
HB56UW1673EJN Series

HB56UW1665EJN Series

16777216-word $\times$ 72-bit High Density Dynamic RAM Module
16777216-word $\times$ 64-bit High Density Dynamic RAM Module

HITACHI

ADE-203-655 (Z)
Preliminary
Rev. 0.0
Sep. 9, 1996

Description

The HB56UW1673EJN Series, HB56UW1665EJN Series belong to 8-byte DIMM (Dual in-line Memory Module) family, and have been developed an optimized main memory solution for 4 and 8-byte processor applications. The HB56UW1673EJN Series is a 16 M $\times$ 72 Dynamic RAM Module, mounted 18 pieces of 64-Mbit DRAM (HM5165405AJ) sealed in SOJ package and 1 piece of serial EEPROM (24C02) for Presence Detect (PD). The HB56UW1665EJN Series is a 16 M $\times$ 64 Dynamic RAM Module, mounted 16 pieces of 64-Mbit DRAM (HM5165405AJ) sealed in SOJ package and 1 piece of serial EEPROM (24C02) for Presence Detect (PD). The HB56UW1673EJN Series, HB56UW1665EJN Series offer Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56UW1673EJN Series, HB56UW1665EJN Series are 168-pin socket type package (dual lead out). Therefore, the HB56UW1673EJN Series, HB56UW1665EJN Series make high density mounting possible without surface mount technology. The HB56UW1673EJN Series, HB56UW1665EJN Series provide common data inputs and outputs. Decoupling capacitors are mounted beside each SOJ on the its module board.

Features

- 168-pin socket type package (Dual lead out)
 - Outline: 133.35 mm (Length) $\times$ 25.40 mm (Height) $\times$ 9.00 mm (Thickness)
 - Lead pitch : 1.27 mm
- Single 3.3 V (± 0.3 V)
- High speed
 - Access time: $t_{RAC} = 60$ ns/70 ns (max)
 - Access time: $t_{CAC} = 15$ ns/18 ns (max)

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

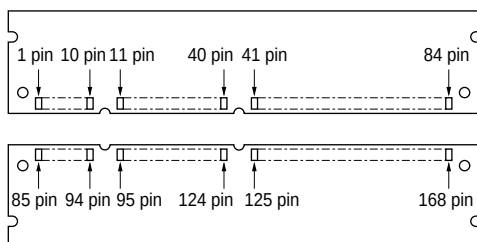
HB56UW1673EJN Series, HB56UW1665EJN Series

- Low power dissipation
 - Active mode: 11.66 W/10.37W (max) (HB56UW1673EJN Series)
 - Active mode: 10.37 W/9.22W (max) (HB56UW1665EJN Series)
 - Standby mode (TTL): 129.6 mW (max) (HB56UW1673EJN Series)
 - Standby mode (TTL): 115.2 mW (max) (HB56UW1665EJN Series)
 - Standby mode (CMOS): 64.8 mW (max) (HB56UW1673EJN Series)
 - Standby mode (CMOS): 57.6 mW (max) (HB56UW1665EJN Series)
- JEDEC standard outline unbuffered 8-byte DIMM
- EDO page mode capability
- 4096 refresh cycles: 64 ms
- 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56UW1673EJN-6A	60 ns	168-pin dual lead out socket type	Gold
HB56UW1673EJN-7A	70 ns		
HB56UW1665EJN-6A	60 ns		
HB56UW1665EJN-7A	70 ns		

Pin Arrangement



Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	$\overline{\text{OE}}2$	86	DQ32	128	NC
3	DQ1	45	$\overline{\text{RAS}}2$	87	DQ33	129	NC
4	DQ2	46	$\overline{\text{CAS}}2$	88	DQ34	130	$\overline{\text{CAS}}6$
5	DQ3	47	$\overline{\text{CAS}}3$	89	DQ35	131	$\overline{\text{CAS}}7$
6	V _{CC}	48	$\overline{\text{WE}}2$	90	V _{CC}	132	NC
7	DQ4	49	V _{CC}	91	DQ36	133	V _{CC}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2 (NC)* ³	94	DQ39	136	CB6 (NC)* ⁷
11	DQ8	53	CB3 (NC)* ⁴	95	DQ40	137	CB7 (NC)* ⁸
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V _{CC}	101	DQ45	143	V _{CC}
18	V _{CC}	60	DQ20	102	V _{CC}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0 (NC)* ¹	63	NC	105	CB4 (NC)* ⁵	147	NC
22	CB1 (NC)* ²	64	V _{SS}	106	CB5 (NC)* ⁶	148	V _{SS}
23	V _{SS}	65	DQ21	107	V _{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55

HB56UW1673EJN Series, HB56UW1665EJN Series

Pin Arrangement (cont)

Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
26	V _{CC}	68	V _{SS}	110	V _{CC}	152	V _{SS}
27	$\overline{WE}0$	69	DQ24	111	NC	153	DQ56
28	$\overline{CAS}0$	70	DQ25	112	$\overline{CAS}4$	154	DQ57
29	$\overline{CAS}1$	71	DQ26	113	$\overline{CAS}5$	155	DQ58
30	$\overline{RAS}0$	72	DQ27	114	NC	156	DQ59
31	$\overline{OE}0$	73	V _{CC}	115	NC	157	V _{CC}
32	V _{SS}	74	DQ28	116	V _{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	A11	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V _{CC}	82	SDA	124	V _{CC}	166	SA1
41	V _{CC}	83	SCL	125	NC	167	SA2
42	NC	84	V _{CC}	126	NC	168	V _{CC}

Notes: 1. CB0: HB56UW1673EJN, NC: HB56UW1665EJN
2. CB1: HB56UW1673EJN, NC: HB56UW1665EJN
3. CB2: HB56UW1673EJN, NC: HB56UW1665EJN
4. CB3: HB56UW1673EJN, NC: HB56UW1665EJN
5. CB4: HB56UW1673EJN, NC: HB56UW1665EJN
6. CB5: HB56UW1673EJN, NC: HB56UW1665EJN
7. CB6: HB56UW1673EJN, NC: HB56UW1665EJN
8. CB7: HB56UW1673EJN, NC: HB56UW1665EJN

Pin Description

Pin name	Function
A0 to A11	Address input — Row addressA0 to A11 — Column addressA0 to A11 — Refresh addressA0 to A11
DQ0 to DQ63	Data input/output
$\overline{\text{RAS}}0, \overline{\text{RAS}}2$	Row address strobe
$\overline{\text{CAS}}0$ to $\overline{\text{CAS}}7$	Column address strobe
$\overline{\text{WE}}0, \overline{\text{WE}}2$	Read/Write enable
$\overline{\text{OE}}0, \overline{\text{OE}}2$	Output enable
SDA	Serial data out (bit0 to bit7)
SCL	Clock for presence detect
SA0 to SA2	Serial address input
CB0 to CB7*1	Check bit
V _{cc}	Power supply
V _{ss}	Ground
NC	No connection

Note: 1. This function is supported only HB56UW1673EJN Series.

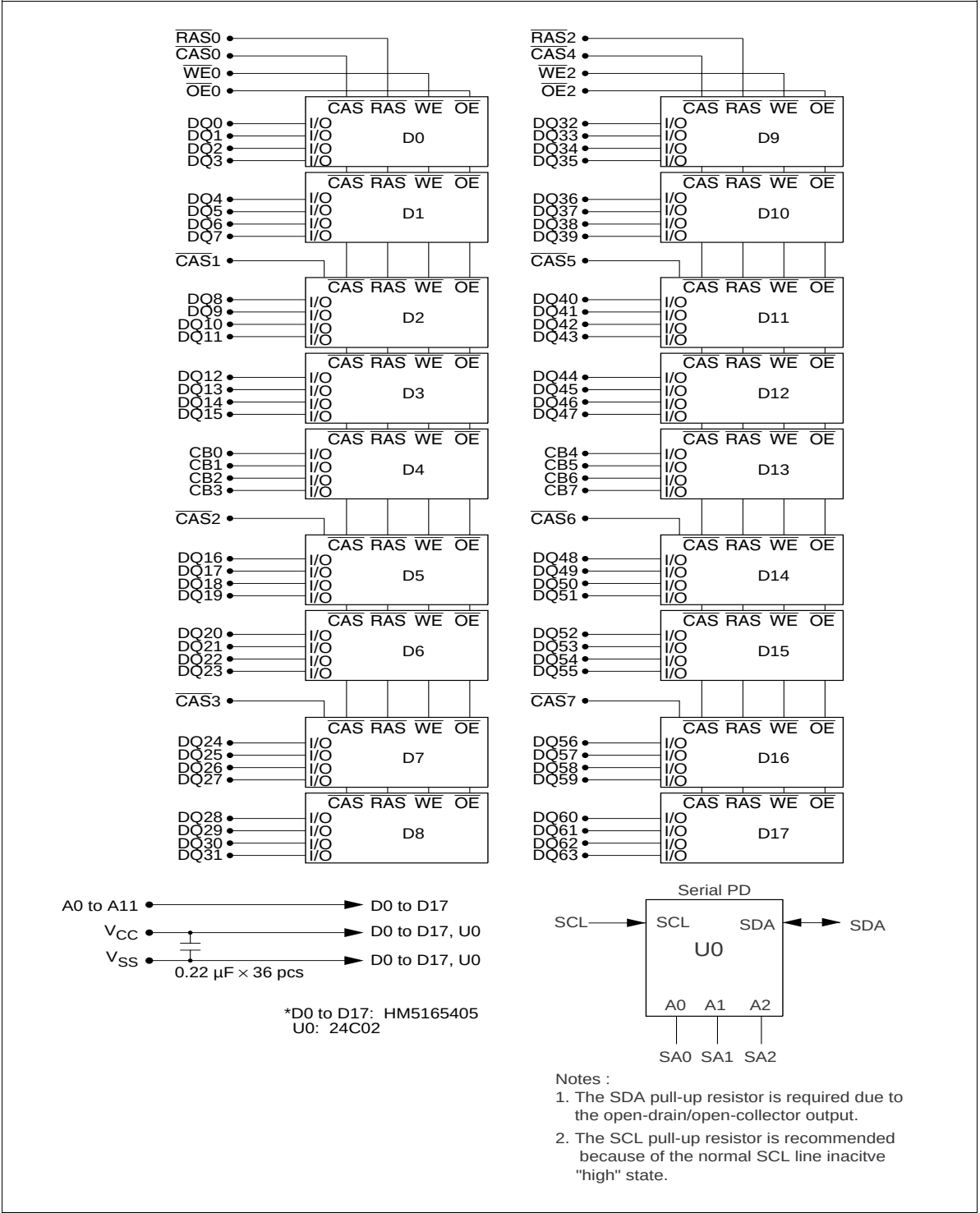
HB56UW1673EJN Series, HB56UW1665EJN Series

Serial PD Matrix*1

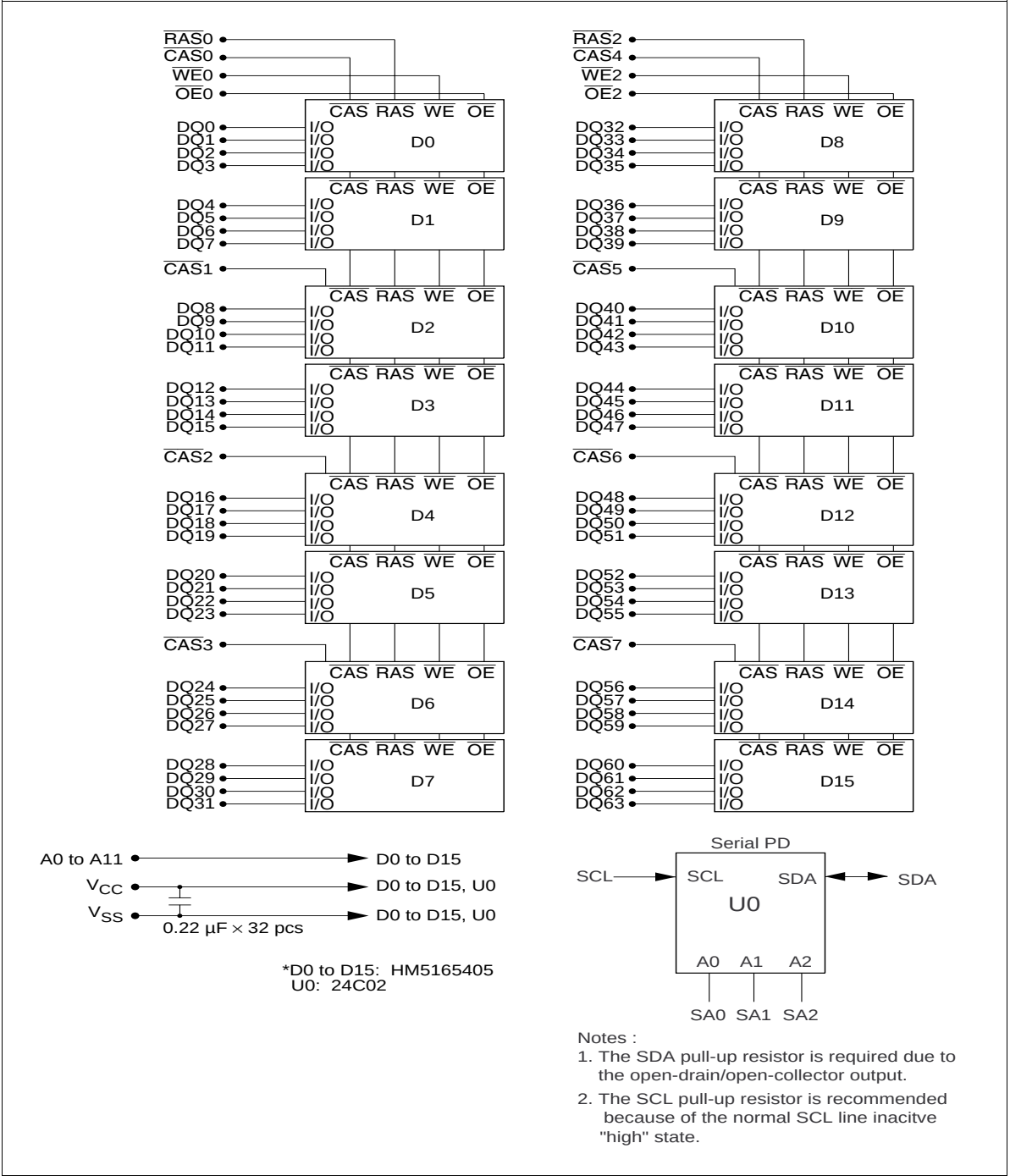
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comments
0	Number serial PD bytes	0	0	0	0	1	1	0	1	13
1	Serial memory	0	0	0	0	1	0	0	0	256byte
2	Fundamental memory type	0	0	0	0	0	0	1	0	EDO
3	Number of row addresses	0	0	0	0	1	1	0	0	12
4	Number of column addresses	0	0	0	0	1	1	0	0	12
5	Number of banks	0	0	0	0	0	0	0	1	1
6	Module data width									
	HB56UW1673EJN	0	1	0	0	1	0	0	0	72
	HB56UW1665EJN	0	1	0	0	0	0	0	0	64
7	Module data width (continued)	0	0	0	0	0	0	0	0	0 (+)
8	Module supply voltage/interface levels	0	0	0	0	0	0	1	0	3.3 V
9	RAS access time									
	60 ns	0	0	1	1	1	1	0	0	
	70 ns	0	1	0	0	0	1	1	0	
10	CAS access time									
	15 ns	0	0	0	0	1	1	1	1	
	18 ns	0	0	0	1	0	0	1	0	
11	Error detection/correction									
	HB56UW1673EJN	0	0	0	0	0	0	1	0	ECC
	HB56UW1665EJN	0	0	0	0	0	0	0	0	None
12	Refresh rate/type	0	0	0	0	0	0	0	0	Normal (15.625 μs)

Note: 1. 0: Serial data, “driven Low”, 1: Serial data, “driven High”
Serial PD data are not protected.

Block Diagram (HB56UW1673EJN)



Block Diagram (HB56UW1665EJN)



Absolute Maximum Ratings (HB56UW1673EJN)

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +4.6	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	18	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Absolute Maximum Ratings (HB56UW1665EJN)

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +4.6	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	16	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.3	3.6	V	1, 2
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	−0.3	—	0.8	V	1

- Note:
1. All voltage referred to V_{SS} .
 2. The supply voltage with all V_{CC} pins must be on the same level. The supply voltage with all V_{SS} pins must be on the same level.

HB56UW1673EJN Series, HB56UW1665EJN Series

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)
(HB56UW1673EJN)

		HB56UW1673EJN					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Operating current* ¹ , * ²	I _{CC1}	—	3240	—	2880	mA	t _{RC} = min
Standby current	I _{CC2}	—	36	—	36	mA	TTL interface R _{AS} , C _{AS} = V _{IH} Dout = High-Z
		—	18	—	18	mA	CMOS interface R _{AS} , C _{AS} ≥ V _{CC} − 0.2 V Dout = High-Z
R _{AS} -only refresh current* ²	I _{CC3}	—	3240	—	2880	mA	t _{RC} = min
Standby current* ¹	I _{CC5}	—	90	—	90	mA	R _{AS} = V _{IH} , C _{AS} = V _{IL} Dout = enable
C _{AS} -before-R _{AS} refresh current	I _{CC6}	—	2700	—	2340	mA	t _{RC} = min
EDO page mode current* ¹ , * ³	I _{CC7}	—	2520	—	2160	mA	t _{HPC} = min
Input leakage current	I _{LI}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 4.6
Output leakage current	I _{LO}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 4.6 Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

- Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while R_{AS} = V_{IL}.
3. Address can be changed once or less within one page mode cycle t_{HPC}.

DC Characteristics ($T_a = 0 \text{ to } +70^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = 0 \text{ V}$)
(HB56UW1665EJN)

HB56UW1665EJN							
Parameter	Symbol	60 ns		70 ns		Unit	Test conditions
		Min	Max	Min	Max		
Operating current* ¹ , * ²	I _{CC1}	—	2880	—	2560	mA	t _{RC} = min
Standby current	I _{CC2}	—	32	—	32	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z
		—	16	—	16	mA	CMOS interface RAS, CAS ≥ V _{CC} – 0.2 V Dout = High-Z
RAS-only refresh current* ²	I _{CC3}	—	2880	—	2560	mA	t _{RC} = min
Standby current* ¹	I _{CC5}	—	80	—	80	mA	RAS = V _{IH} , CAS = V _{IL} Dout = enable
CAS-before-RAS refresh current	I _{CC6}	—	2400	—	2080	mA	t _{RC} = min
EDO page mode current* ¹ , * ³	I _{CC7}	—	2240	—	1920	mA	t _{HPC} = min
Input leakage current	I _{LI}	–10	10	–10	10	μA	0 V ≤ Vin ≤ 4.6 V
Output leakage current	I _{LO}	–10	10	–10	10	μA	0 V ≤ Vin ≤ 4.6 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = –2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

- Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
 2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less within one page mode cycle t_{HPC} .

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V) (HB56UW1673EJN)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	110	pF	1
Input capacitance ($\overline{\text{CAS}}$)	C _{I2}	—	41	pF	1
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{I3}	—	83	pF	1
I/O capacitance (DQ)	C _{I/O}	—	20	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}}$ = V_{IH} to disable Dout.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V) (HB56UW1665EJN)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	100	pF	1
Input capacitance ($\overline{\text{CAS}}$)	C _{I2}	—	34	pF	1
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{I3}	—	76	pF	1
I/O capacitance (DQ)	C _{I/O}	—	20	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}}$ = V_{IH} to disable Dout.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$) *¹, *², *³, *¹⁸

Test Conditions

- Input rise and fall time: 2 ns
- Input levels: $V_{IL} = 0\text{ V}$, $V_{IH} = 3\text{ V}$
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HB56UW1673EJN/HB56UW1665EJN					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t _{RC}	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t _{RP}	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t _{CP}	10	—	13	—	ns	
$\overline{RAS}$ pulse width	t _{RAS}	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t _{CAS}	10	10000	13	10000	ns	
Row address setup time	t _{ASR}	0	—	0	—	ns	
Row address hold time	t _{RAH}	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	ns	
Column address hold time	t _{CAH}	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t _{RCD}	20	45	20	52	ns	3
$\overline{RAS}$ to column address delay time	t _{RAD}	15	30	15	35	ns	4
$\overline{RAS}$ hold time	t _{RSH}	15	—	18	—	ns	
$\overline{CAS}$ hold time	t _{CSH}	48	—	58	—	ns	20
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t _{CRP}	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t _{OED}	15	—	18	—	ns	5
$\overline{OE}$ delay time from Din	t _{DZO}	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t _{DZC}	0	—	0	—	ns	6
Transition time (rise and fall)	t _T	2	50	2	50	ns	7

HB56UW1673EJN Series, HB56UW1665EJN Series

Read Cycle

		HB56UW1673EJN/		HB56UW1665EJN			
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	ns	9, 10, 16
Access time from address	t_{AA}	—	30	—	35	ns	9, 11, 16
Access time from $\overline{\text{OE}}$	t_{OEA}	—	15	—	18	ns	9
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	ns	13, 20
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	ns	
Output buffer turn-off to $\overline{\text{RAS}}$	t_{OFR}	—	15	—	15	ns	20
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	ns	

Write Cycle

		HB56UW1673EJN/ HB56UW1665EJN					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	t _{WCS}	0	—	0	—	ns	14
Write command hold time	t _{WCH}	10	—	13	—	ns	
Write command pulse width	t _{WP}	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	10	—	13	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	10	—	13	—	ns	
Data-in setup time	t _{DS}	0	—	0	—	ns	
Data-in hold time	t _{DH}	10	—	13	—	ns	

Read-Modify-Write Cycle

		HB56UW1673EJN/		HB56UW1665EJN			
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t _{RWC}	149	—	175	—	ns	
RAS to $\overline{WE}$ delay time	t _{RWD}	78	—	91	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t _{CWD}	33	—	39	—	ns	14
Column address to $\overline{WE}$ delay time	t _{AWD}	48	—	56	—	ns	14
$\overline{OE}$ hold time from $\overline{WE}$	t _{OEH}	15	—	18	—	ns	

Refresh Cycle

		HB56UW1673EJN/ HB56UW1665EJN					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
CAS setup time (CBR refresh cycle)	t _{CSR}	5	—	5	—	ns	
CAS hold time (CBR refresh cycle)	t _{CHR}	10	—	10	—	ns	
WE setup time (CBR refresh cycle)	t _{WRP}	0	—	0	—	ns	
WE hold time (CBR refresh cycle)	t _{WRH}	10	—	10	—	ns	
RAS precharge to CAS hold time	t _{RPC}	0	—	0	—	ns	

HB56UW1673EJN Series, HB56UW1665EJN Series

EDO Page Mode Cycle

		HB56UW1673EJN/		HB56UW1665EJN			
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t _{HPC}	25	—	30	—	ns	19
EDO page mode $\overline{\text{RAS}}$ pulse width	t _{RASP}	—	100000	—	100000	ns	15
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	35	—	40	ns	9, 16
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{CPRH}	35	—	40	—	ns	
Output data hold time from $\overline{\text{CAS}}$ low	t _{DOH}	3	—	3	—	ns	9, 16
$\overline{\text{CAS}}$ hold time referred $\overline{\text{OE}}$	t _{COL}	10	—	13	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ setup time	t _{COP}	10	—	10	—	ns	
Read command hold time from $\overline{\text{CAS}}$ precharge	t _{RCHC}	35	—	40	—	ns	
Write pulse width during $\overline{\text{CAS}}$ precharge	t _{WPE}	10	—	10	—	ns	
$\overline{\text{OE}}$ precharge time	t _{OEP}	10	—	10	—	ns	

EDO Page Mode Read-Modify-Write Cycle

		HB56UW1673EJN/ HB56UW1665EJN					
		60 ns		70 ns			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
EDO page mode read- modify-write cycle time	t _{HPRWC}	68	—	79	—	ns	
$\overline{\text{WE}}$ delay time from $\overline{\text{CAS}}$ precharge	t _{CPW}	54	—	62	—	ns	14

Refresh

Parameter	Symbol	Max	Unit	Notes
Refresh period	t _{REF}	64	ms	4096 cycles

- Notes:
1. AC measurements assume $t_r = 2$ ns.
 2. An initial pause of 200 μ s is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS-before-RAS refresh).
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. Either t_{OED} or t_{CDD} must be satisfied.
 6. Either t_{DZO} or t_{DZC} must be satisfied.
 7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
 10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
 11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
 12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 13. t_{OFF} (max), t_{OEZ} (max), t_{WEZ} (max) and t_{OFR} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 15. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
 16. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 17. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
 19. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2 t_r$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
 20. Output is disable after both $\overline{RAS}$ and $\overline{CAS}$ go to high.
 21. t_{CSH} (min) can be achieved when $t_{RCD} \leq t_{CSH}$ (min) - t_{CAS} (min).
 22. XXX: H or L (H: V_{IH} (min) $\leq V_{IN} \leq V_{IH}$ (max), L: V_{IL} (min) $\leq V_{IN} \leq V_{IL}$ (max))
 /////////////// Invalid Dout
 When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

Timing Waveforms*22

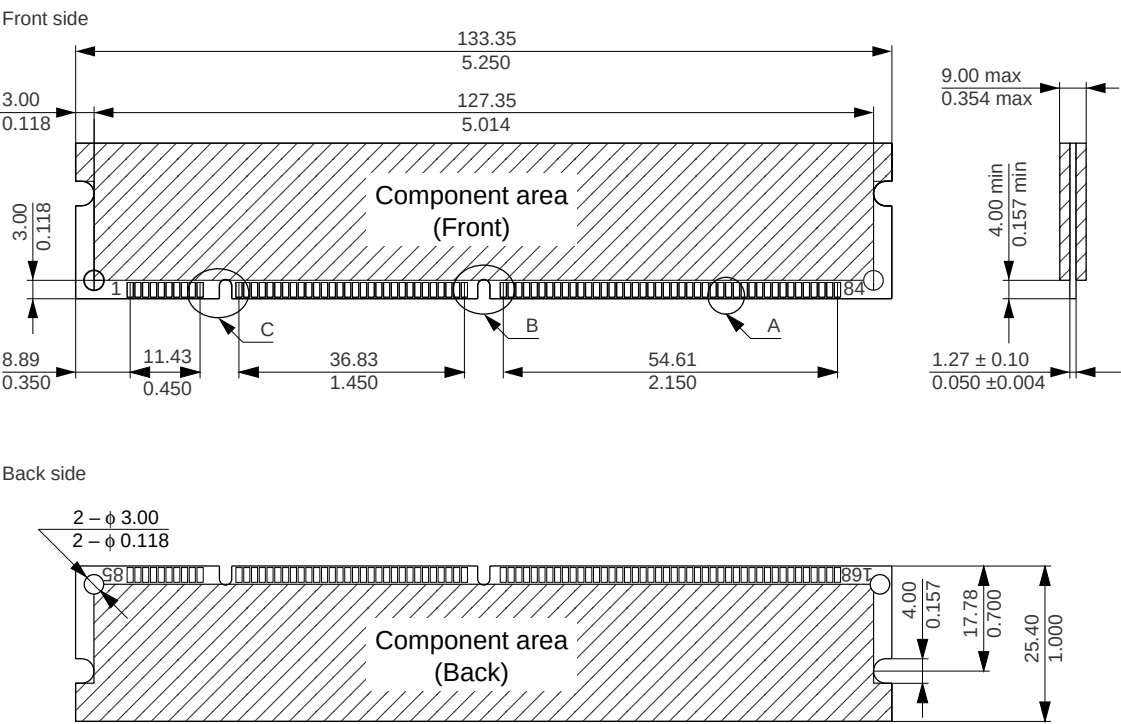
Refer to the HB56UW3273 Series.

HB56UW1673EJN Series, HB56UW1665EJN Series

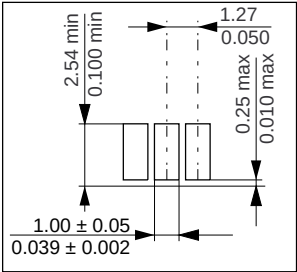
Physical Outline

HB56UW1673EJN Series,
HB56UW1665EJN Series

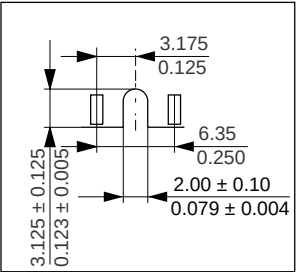
Unit: mm/inch



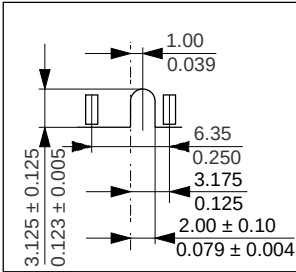
Detail A



Detail B



Detail C



When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. **MEDICAL APPLICATIONS:** Hitachi's products are not authorized for use in **MEDICAL APPLICATIONS** without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in **MEDICAL APPLICATIONS**.

HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

HB56UW1673EJN Series, HB56UW1665EJN Series

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Sep. 9, 1996	Initial issue		