CRYSTAL CLOCK OSCILLATORS

Data Sheet 0208E

Rev. M

LVDS
PJ-A2D00 Series

Description

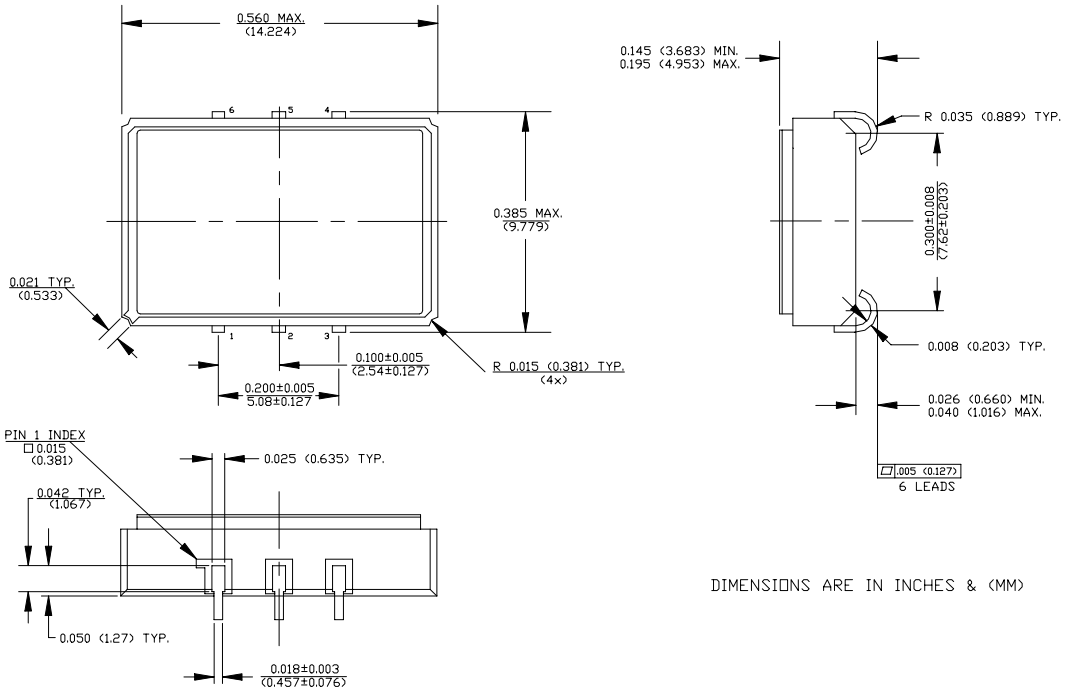
The **PJ-A2D00 Series** of quartz crystal oscillators provide LVDS compatible signals in a ceramic SMD package. Systems designers may now specify space-saving, cost-effective packaged LVDS oscillators to meet their timing requirements.

Features

- Wide frequency range–80.0MHz to 312.5MHz
- User specified tolerance available
- Space-saving alternative to discrete component oscillators
- High shock resistance, to 1000g
- 3.3 volt operation (other voltages available upon request)
- Metal lid electrically connected to ground to reduce EMI
- Enable/Disable
- LVDS output on pin 4, complement on Pin 5
- COTS/Dual use
- Low Jitter - Wavecrest jitter characterization available
- High Reliability - NEL HALT/HASS qualified for crystal oscillator start-up conditions
- Overtone technology
- High Q Crystal actively tuned oscillator circuit
- Power supply decoupling internal
- No internal PLL avoids cascading PLL problems
- High frequencies due to proprietary design
- Gold plated leads
- RoHS Compliant, Lead Free Construction

Electrical Connection

Pin	Connection
1	Enable/Disable
2	N.C.
3	Ground
4	Output
5	Output Complement
6	V_{CC}



NEL FREQUENCY CONTROLS, INC.

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PJ-A2D00 Series Continued
LVDS

Rev. M

Operating Conditions and Output Characteristics

Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max
Frequency	-----	-----	80.0MHz	-----	312.5MHz
Duty Cycle(2)	-----	@ V_O /2	45/55%	-----	55/45%
Logic 0 (2)	V_{OL}	-----	0.80V	-----	1.10V
Logic 1 (2)	V_{OH}	-----	1.25V	-----	1.55V
Differential Voltage (2)	V_{OD}	-----	250 mV	-----	450 mV
Disable Voltage	-----	V_{EE}=0V	-----	-----	0.8V
Enable Voltage(5)	-----	V_{EE}=0V	2.0V	-----	-----
Rise & Fall Time (2)	tr,tf	20-80%V_O	-----	0.8 ns	1.0 ns
Tpd (4)	-----	-----	-0.5 ns	-----	+0.5 ns
Jitter, Integrated	J	Integrated from phase noise, 12kHz to 20MHz, RMS	-----	0.1 ps	-----
Jitter, Wavecrest Characterized (3)	-----	Random Period	-----	2.3ps	-----
		Accum, pk-to-pk	-----	28ps	-----
Phase Noise	£(Δf)	200MHz			
		@ 10Hz	-----	-65 dBc/Hz	-----
		@100Hz	-----	-100 dBc/Hz	-----
		@1kHz	-----	-130 dBc/Hz	-----
		@10kHz	-----	-143 dBc/Hz	-----
		@100kHz	-----	-143 dBc/Hz	-----
		@ >1Mhz	-----	-145 dBc/Hz	-----
Frequency Stability (1)	dF/F	Overall conditions including: voltage, calibration, temp., 10 yr aging, shock, vibration	-100ppm	-----	+100ppm

General Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max
Supply Voltage	V_{CC}	-----	3.135V	3.3V	3.465V
Supply Current	I_{CC}	-----	0.0 mA	-----	80 mA
Output current	I_O	Continuous Output Current	0.0 mA	-----	±50.0 mA
Operating temperature	T_A	------	0°C	-----	70°C
Storage temperature	T_S	-----	-55°C	-----	125°C
Power Dissipation	P_D	-----	-----	-----	277 mW
Load	100 ohms across differential outputs				
Start-up time	t_S	-----	-----	2 ms	10 ms

Environmental and Mechanical Characteristics

Mechanical Shock	Per MIL-STD-202, Method 213, Condition E
Thermal Shock	Per MIL-STD-883, Method 1011, Condition A
Vibration	0.060" double amplitude 10 Hz to 55 Hz, 35g's 55Hz to 2000 Hz
Hermetic Seal	Leak rate less than 1 x 10^{-8} atm.cc/sec of helium

Footnotes:
1) Standard frequency stability (±20,±25,±50ppm & others available)
2) With Load of 100 ohms across differential outputs.
3) Jitter performance is frequency dependent. Please contact factory for full Wavecrest characterization.
) Tpd is phase shift between the falling edge of pin 4 and the rising edge of pin 5.
5) Open to enable pin also enables the output

Creating a Part Number

PJ - A2D0X - FREQ

Package Code
PJ 6 J Lead SMD

Input Voltage

Code	Specification
A	3.3V
B	2. 5V
	5V

Tolerance/Performance

0	±100ppm 0-70°C
1	±50ppm 0-70°C
7	±25ppm 0-70°C
9	Customer Specific
A	±20ppm 0-70°C
B	±50ppm -40 to +85°C
C	±100ppm -40 to +85°C

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PJ-A2D00 Series Continued

Max Reflow Profile