

Features

- Read Access Time - 100 ns
- Word-wide or Byte-wide Configurable
- 8-Megabit Flash and Mask ROM Compatible
- Low Power CMOS Operation
 - 100 μ A Maximum Standby
 - 50 mA Maximum Active at 5 MHz
- Wide Selection of JEDEC Standard Packages
 - 42-Lead 600 mil Cerdip and PDIP
 - 44-Lead SOIC (SOP)
 - 48-Lead TSOP (12 mm x 20 mm)
- 5V \pm 10% Power Supply
- High Reliability CMOS Technology
 - 2,000 ESD Protection
 - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 50 μ s/word (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

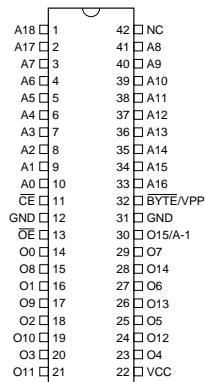
The AT27C800 is a low-power, high performance 8,388,608-bit UV erasable programmable read only memory (EPROM) organized as either 512K by 16 or 1024K by 8 bits. It requires a single 5V power supply in normal read mode operation. Any word can be accessed in less than 100 ns, eliminating the need for speed-reducing WAIT states. The x16 organization makes this part ideal for high-performance 16- and 32-bit microprocessor systems.

(continued)

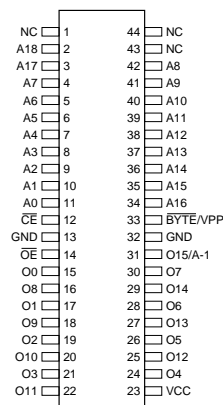
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
O0 - O15	Outputs
O15/A-1	Output/Address
BYTE/VPP	Byte Mode/ Program Supply
CE	Chip Enable
OE	Output Enable
NC	No Connect

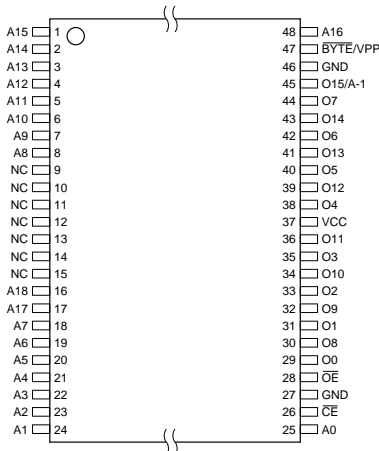
CDIP, PDIP Top View



SOIC (SOP)



TSOP
Type 1



**8-Megabit
(512K x 16 or
1024K x 8)
UV Erasable
EPROM**

**AT27C800
Preliminary**

The AT27C800 can be organized as either word-wide or byte-wide. The organization is selected via the $\overline{\text{BYTE/V}}_{\text{PP}}$ pin. When $\overline{\text{BYTE/V}}_{\text{PP}}$ is asserted high (V_{IH}), the word-wide organization is selected and the O15/A-1 pin is used for O15 data output. When $\overline{\text{BYTE/V}}_{\text{PP}}$ is asserted low (V_{IL}), the byte wide organization is selected and the O15/A-1 pin is used for the address pin A-1. When the AT27C800 is logically regarded as x16 (word-wide), but read in the byte-wide mode, then with $A-1 = V_{\text{IL}}$ the lower eight bits of the 16 bit word are selected with $A-1 = V_{\text{IH}}$ the upper 8 bits of the 16-bit word are selected.

In read mode, the AT27C800 typically consumes 15 mA. Standby mode supply current is typically less than 10 μA .

The AT27C800 is available in industry standard JEDEC-approved one-time programmable (OTP) PDIP, SOIC (SOP), and TSOP as well as UV erasable windowed Cerdip packages. The device features two-line control ($\overline{\text{CE}}$, $\overline{\text{OE}}$) to eliminate bus contention in high-speed systems.

With high density 512K word or 1024K-bit storage capability, the AT27C800 allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's AT27C800 has additional features that ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 50 μs /word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming equipment and voltages.

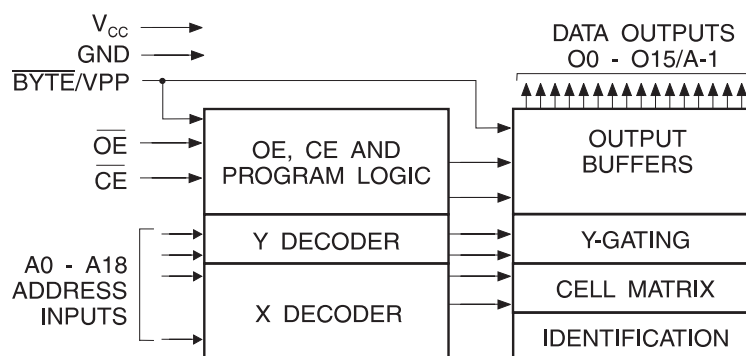
Erase Characteristics

The entire memory array of the AT27C800 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2,537 \AA . Complete erasure is assured after a minimum of 20 minutes of exposure using 12,000 $\mu\text{W}/\text{cm}^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 $\text{W}\cdot\text{sec}/\text{cm}^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM that will be subjected to continuous fluorescent indoor lighting or sunlight.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 μF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with with Respect to Ground.....	-2.0V to +7.0V ⁽¹⁾
Voltage on A9 with Respect to Ground	-2.0V to +14.0V ⁽¹⁾
V _{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V ⁽¹⁾
Integrated UV Erase Dose.....	7258 W •sec/cm ²

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC which may overshoot to + 7.0V for pulses of less than 20 ns.

Operating Modes

Mode\Pin	CE	OE	Ai	BYTE/V _{PP}	Outputs		
					O ₀ -O ₇	O ₈ -O ₁₄	O ₁₅ /A-1
Read Word-wide	V _{IL}	V _{IL}	X ⁽¹⁾	V _{IH}	D _{OUT}	D _{OUT}	D _{OUT}
Read Byte-wide Upper	V _{IL}	V _{IL}	X ⁽¹⁾	V _{IL}	D _{OUT}	High Z	V _{IH}
Read Byte-wide Lower	V _{IL}	V _{IL}	X ⁽¹⁾	V _{IL}	D _{OUT}	High Z	V _{IL}
Output Disable	X ⁽¹⁾	V _{IH}	X ⁽¹⁾	X		High Z	
Standby	V _{IH}	X ⁽¹⁾	X ⁽¹⁾	X ⁽⁵⁾		High Z	
Rapid Program ⁽²⁾	V _{IL}	V _{IH}	Ai	V _{PP}		D _{IN}	
PGM Verify	X	V _{IL}	Ai	V _{PP}		D _{OUT}	
PGM Inhibit	V _{IH}	V _{IH}	X ⁽¹⁾	V _{PP}		High Z	
Product Identification ⁽⁴⁾	V _{IL}	V _{IL}	A9 = V _H ⁽³⁾ A0 = V _{IH} or V _{IL} A1 - A18 = V _{IL}	V _{IH}	Identification Code		

- Notes:
1. X can be V_{IL} or V_{IH}.
 2. Refer to the programming characteristics tables in this data sheet.
 3. V_H = 12.0 ± 0.5V.
 4. Two identifier words may be selected. All Ai inputs are held low (V_{IL}) except A9, which is set to V_H, and A0, which is toggled low (V_{IL}) to select the Manufacturer's Identification word and high (V_{IH}) to select the Device Code word.
 5. Standby V_{CC} current (I_{SB}) is specified with V_{PP} = V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.



DC and AC Operating Conditions for Read Operation

		AT27C800		
		-10	-12	-15
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V _{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC}		±1.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0V to V _{CC}		±5.0	μA
I _{PP1} ⁽²⁾	V _{PP} ⁽¹⁾ Read/Standby Current	V _{PP} = V _{CC}		±10	μA
I _{SB}	V _{CC} ⁽¹⁾ Standby Current	I _{SB1} (CMOS) CE = V _{CC} ± 0.3V		100	μA
		I _{SB2} (TTL) CE = 2.0 to V _{CC} + 0.5V		1.0	mA
	V _{CC} Active Current	f = 5MHz, I _{OUT} = 0 mA, CE = V _{IL}		50	mA
V _{IL}	Input Low Voltage		-0.6	0.8	V
V _{IH}	Input High Voltage		2.0	V _{CC} + 0.5	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -400 mA	2.4		V

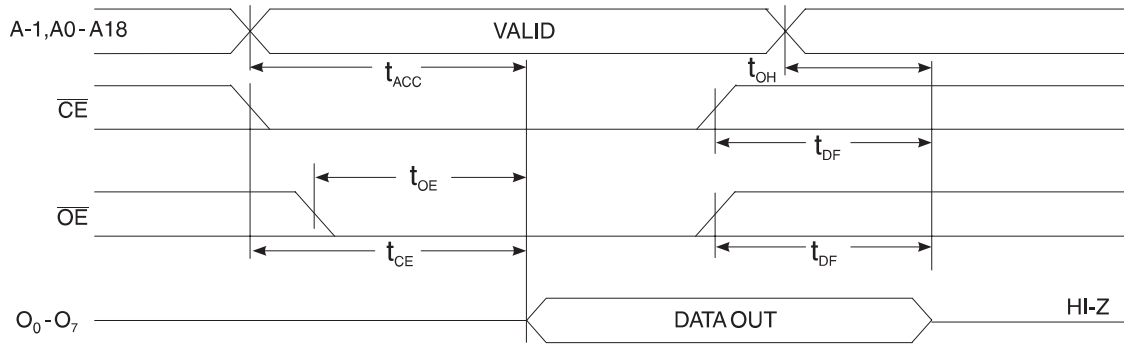
- Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
 2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

Symbol	Parameter	Condition	AT27C800						Units
			-10		-12		-15		
			Min	Max	Min	Max	Min	Max	
t _{ACC} ⁽³⁾	Address to Output Delay	CE = OE = V _{IL}		100		120		150	ns
t _{CE} ⁽²⁾	CE to Output Delay	OE = V _{IL}		100		120		150	ns
t _{OE} ^(2,3)	OE to Output Delay	CE = V _{IL}		40		40		50	ns
t _{DF} ^(4,5)	OE or CE High to Output Float, whichever occurred first			30		35		40	ns
t _{OH} ⁽⁴⁾	Output Hold from Address CE or OE, whichever occurred first		5.0		5.0		5.0		ns
t _{ST}	BYTE High to Output Valid			100		120		150	ns
t _{STD}	BYTE Low to Output Transition			40		50		60	ns

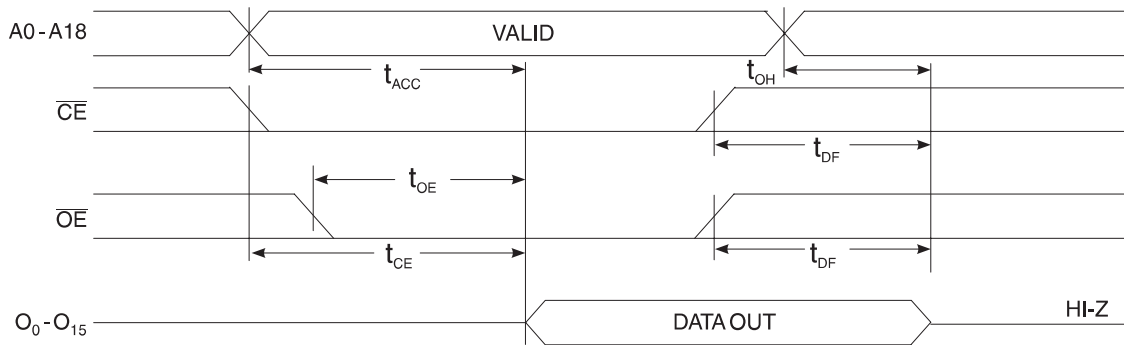
- Notes: 2,3,4,5. See the AC Waveforms for Read Operation diagram.

Byte-Wide Read Mode AC Waveforms⁽¹⁾



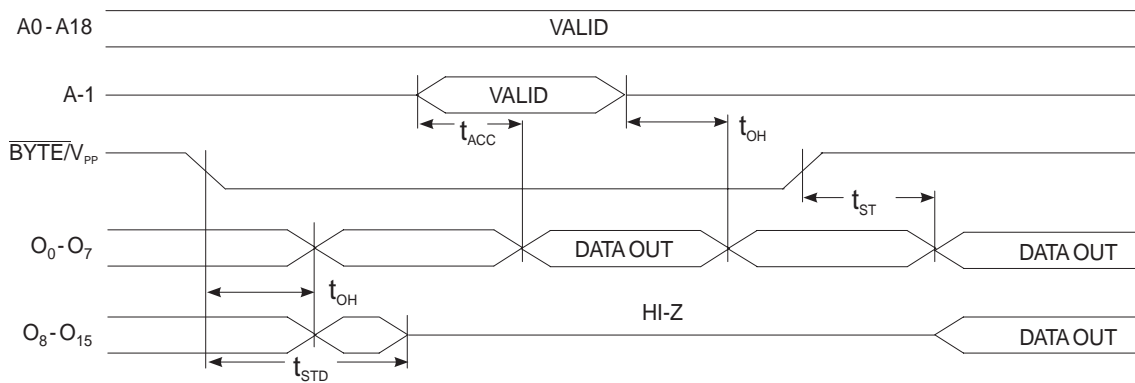
Note: 1. BYTE/V_{PP} = V_{IL}

Byte-Wide Read Mode AC Waveforms⁽¹⁾



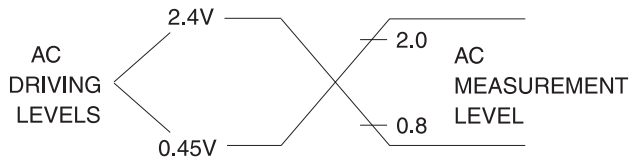
Note: 1. BYTE/V_{PP} = V_{IH}

BYTE Transition AC Waveforms



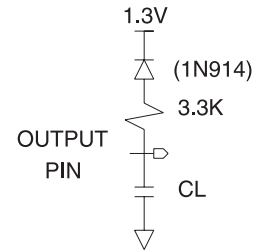
- Notes: 1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
- 2. OE may be delayed up to t_{CE} - t_{OE} after the falling edge of CE without impact on t_{CE}.
- 3. OE may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
- 4. This parameter is only sampled and is not 100% tested.
- 5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



$t_R, t_F < 20$ ns (10% to 90%)

Output Test Load



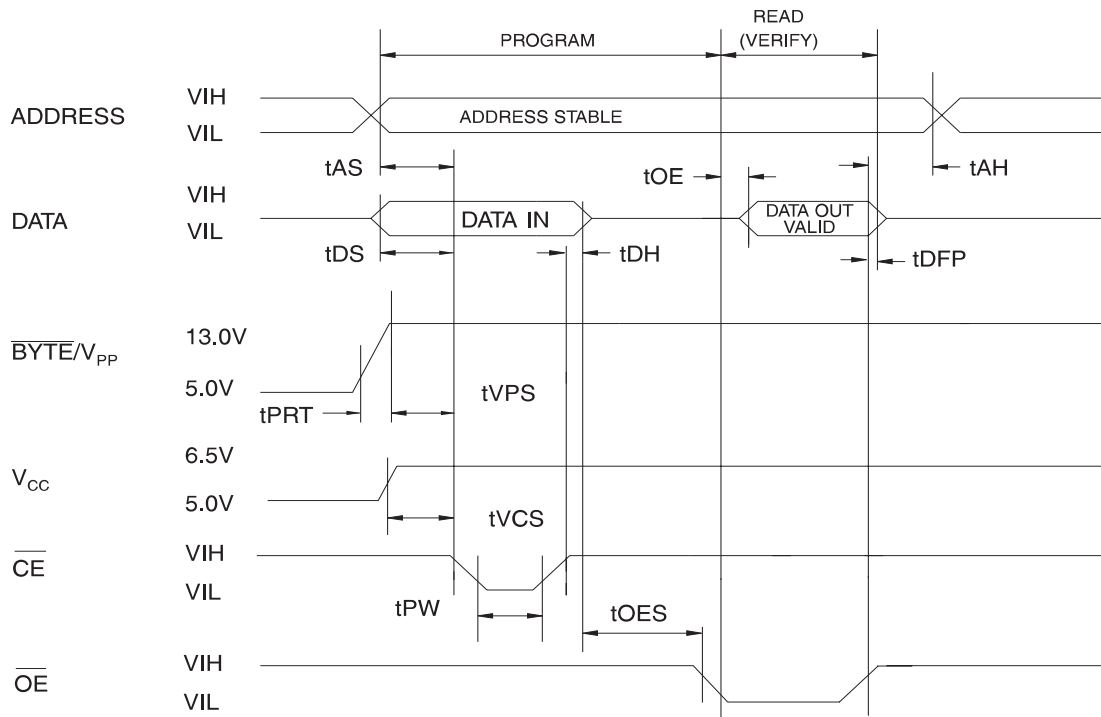
Note: 1. CL = 100 pF including jig capacitance.

Pin Capacitance ($f = 1$ MHz, $T = 25^\circ\text{C}$)⁽¹⁾

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms⁽¹⁾



- Notes:
1. The Input Timing reference is 0.8V for V_{IL} and 2.0V for V_{IH} .
 2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
 3. When programming the AT27C800, a 0.1 μF capacitor is required across V_{PP} and ground to suppress voltage transients.

DC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		± 10	μA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1 \text{ mA}$		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400 \mu\text{A}$	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{\text{CE}} = V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V



AC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions ⁽¹⁾	Limits		Units
			Min	Max	
t_{AS}	Address Setup Time	Input Rise and Fall Times: (10% to 90%) 20 ns.	2		μs
t_{OES}	\overline{OE} Setup Time		2		μs
t_{DS}	Data Setup Time		2		μs
t_{AH}	Address Hold Time	Input Pulse Levels: 45V to 2.4V	0		μs
t_{DH}	Data Hold Time		2		μs
t_{DFP}	\overline{OE} High to Output Float Delay ⁽²⁾	Input Pulse Levels: 0.8V to 2.0V	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		μs
t_{VCS}	V_{CC} Setup Time	Input Timing Reference Level: 0.8V to 2.0V	2		μs
t_{PW}	\overline{CE} Program Pulse Width ⁽³⁾		47.5	52.5	μs
t_{OE}	Data Valid from \overline{OE}	Output Timing Reference Level: 0.8V to 2.0V		150	ns
t_{PRT}	BYTE / V_{PP} Pulse Rise Time During Programming		50		ns

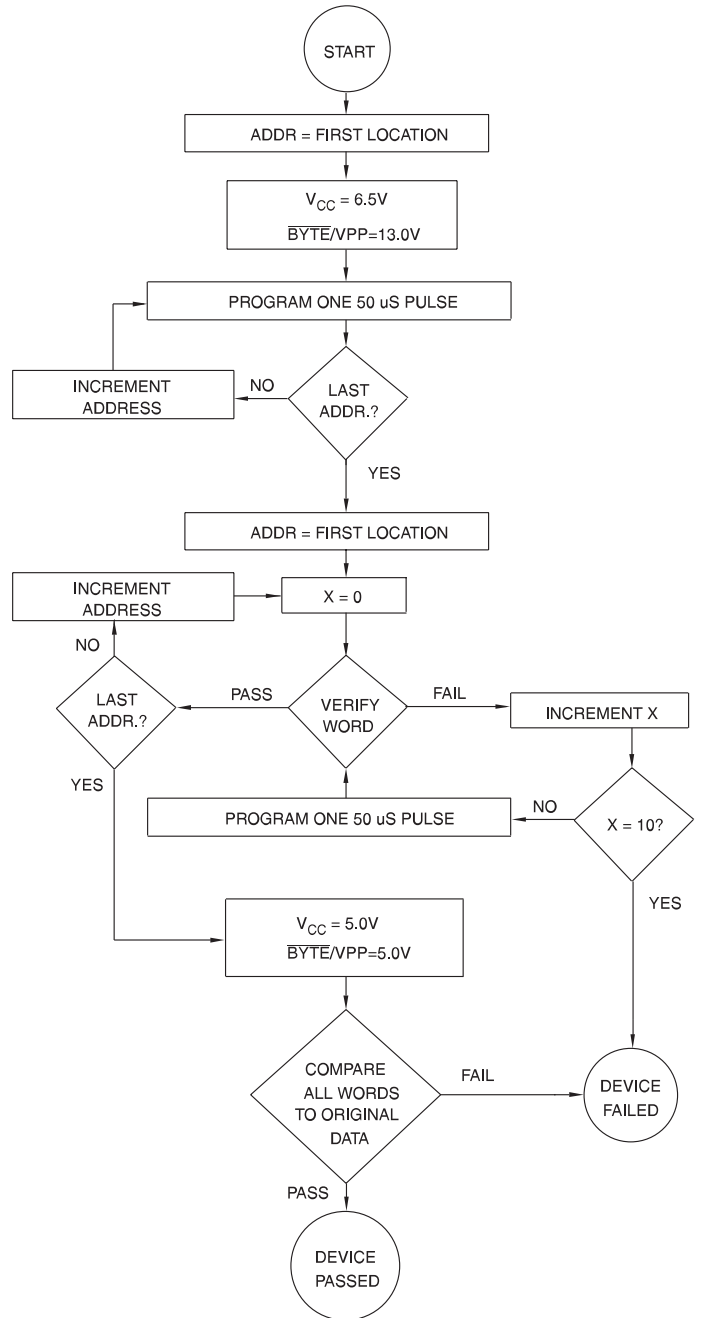
- Notes:
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP} .
 - This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven— see timing diagram.
 - Program Pulse width tolerance is $50 \mu\text{s} \pm 5\%$.

Atmel's 27C800 Integrated Product Identification Code

Codes	Pins									Hex Data
	A0	015	014	013	012	011	010	09	08	
Manufacturer	0	0	0	0	1	1	1	1	0	1E1E
Device Type	1	1	1	1	1	1	0	0	0	F8F8

Rapid Programming Algorithm

A 50 μs $\overline{\text{CE}}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and $\overline{\text{BYTE}}/V_{\text{PP}}$ is raised to 13.0V. Each address is first programmed with one 50 μs $\overline{\text{CE}}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 50 μs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All words are read again and compared with the original data to determine if the device passes or fails.





Ordering Information

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	50	0.1	AT27C800-10DC AT27C800-10PC AT27C800-10RC AT27C800-10TC	42DW6 42P6 44R 48T	Commercial (0°C to 70°C)
	50	0.1	AT27C800-10DI AT27C800-10PI AT27C800-10RI AT27C800-10TI	42DW6 42P6 44R 48T	Industrial (-40°C to 85°C)
120	50	0.1	AT27C800-12DC AT27C800-12PC AT27C800-12RC AT27C800-12TC	42DW6 42P6 44R 48T	Commercial (0°C to 70°C)
	50	0.1	AT27C800-12DI AT27C800-12PI AT27C800-12RI AT27C800-12TI	42DW6 42P6 44R 48T	Industrial (-40°C to 85°C)
150	50	0.1	AT27C800-15DC AT27C800-15PC AT27C800-15RC AT27C800-15TC	42DW6 42P6 44R 48T	Commercial (0°C to 70°C)
	50	0.1	AT27C800-15DI AT27C800-15PI AT27C800-15RI AT27C800-15TI	42DW6 42P6 44R 48T	Industrial (-40°C to 85°C)

Package Type	
42DW6	42 Lead, 0.600" Wide, Ceramic Dual Inline Package (CDIP)
42P6	42 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44R	44 Lead, 0.525" Wide, Plastic Gull Wing Small Outline Package (SOIC/SOP)
48T	48 Lead, Plastic Thin Small Outline Package (TSOP) 12 x 20 mm