

Hex Inverter Gate Logic IC in bare die form

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Description

The 54HC04 hex inverter gate is fabricated on a .35µm advanced CMOS process combining high speed LSTTL performance with CMOS low power. The device contains six independent inverters with standard push-pull outputs which perform the Boolean function $Y = \bar{A}$ in positive logic. Internal circuitry comprises of three stages and includes buffered output for high noise immunity and stability. Inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs. The product die size is significantly smaller than industry peers due to its re-design and production using a more advanced CMOS process.

Ordering Information

The following part suffixes apply:

- No suffix MIL-STD-883 /2010B Visual Inspection
- "H" MIL-STD-883 /2010B Visual Inspection+ MIL-PRF-38534 Class H LAT
- "K" MIL-STD-883 /2010A Visual Inspection (Space)
 + MIL-PRF-38534 Class K LAT

LAT = Lot Acceptance Test.

For further information on LAT process flows see below.

www.siliconsupplies.com\quality\bare-die-lot-qualification

Supply Formats:

- Default Die in Waffle Pack (400 per tray capacity)
- Sawn Wafer on Tape On request
- Unsawn Wafer On request
- Die Thickness <> 350µm(14 Mils) On request
- Assembled into Ceramic Package On request

Features:

Output Drive Capability: 10 LSTTL Loads

■ Low Input Current: 1µA

Outputs directly interface CMOS, NMOS and TTL

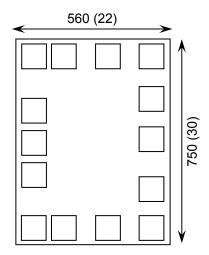
Operating Voltage Range: 2V to 6V

Function compatible with 54LS04

High Noise Immunity CMOS process

Full Military Temperature Range.

Die Dimensions in µm (mils)



Mechanical Specification

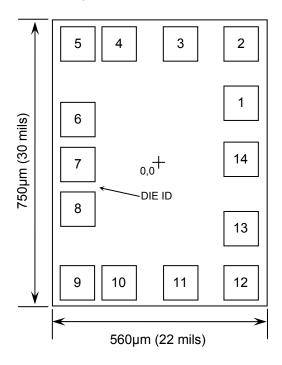
Die Size (Unsawn)	560 x 750 22 x 30	μm mils
Minimum Bond Pad Size	90 x 90 3.54 x 3.54	μm mils
Die Thickness	350 (±20) 13.78 (±0.79)	μm mils
Top Metal Composition	Al 1%Si 1.1μ	m
Back Metal Composition	N/A – Bare S	Si



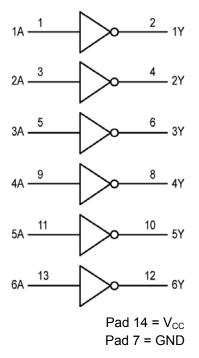


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Pad Layout and Functions



Logic Diagram



PAD	FUNCTION	COORDIN	ATES (µm)
PAD	FUNCTION	X	Y
1	1A	210	155
2	1Y	210	320
3	2A	60	320
4	2Y	-103	320
5 6	3A	-210	320
	3Y	-210	117
7	GND	-210	0
8	4Y	-210	-117
9	4A	-210	-320
10	5Y	-103	-320
11	5A	60	-320
12	6Y	210	-320
13	6A 210		-178
14	V _{CC}	210	9
CON	NECT CHIP BA	CK TO V _{CC} C	R FLOAT

Truth Table

INPUTS	OUTPUT				
Α	Υ				
Н	L				
L	Н				
H = High level (steady state)					
L = Low level	(steady state)				





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Absolute Maximum Ratings¹

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V _{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V _{IN}	-0.5 to V _{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V _{OUT}	-0.5 to V _{CC} +0.5	V
DC Input Current	I _{IN}	±20	mA
DC Output Current, per pad	I _{OUT}	±25	mA
DC Supply Current, V _{CC} or GND	I _{CC}	±50	mA
Power Dissipation in Still Air ²	P _D	750	mW
Storage Temperature Range	T _{STG}	-65 to 150	°C

^{1.} Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. 2. Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions³ (Voltages referenced to GND)

PARAMETER	SYMBOL		MIN	MAX	UNITS
Supply Voltage	V _{CC}		2	6	V
DC Input or Output Voltage	V _{IN} ,V _{OUT}		0	V _{CC}	V
Operating Temperature Range	TJ		-55	+125	°C
Input Rise or Fall Times		V _{CC} = 2V	0	1000	
	t _r , t _f	$V_{CC} = 4.5V$	0	500	ns
		V _{CC} = 6.0V	0	400	

^{3.} This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \le (V_{IN} \text{ or } V_{OUT}) \le V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC Electrical Characteristics (Voltages Referenced to GND)

PARAMETER	SYMBOL	L V _{cc}	CONDITIONS		UNITS		
	OTHIBOL		CONDITIONS	25°C	85°C	FULL RANGE⁴	Julio
Minimum High-Level Input Voltage		2.0V	.,	1.5	1.5	1.5	
	V _{IH}	3.0V	$V_{OUT} = 0.1V \text{ or}$ $V_{CC} - 0.1V$ $\left I_{OUT} \right \le 20\mu\text{A}$	2.1	2.1	2.1	V
		4.5V		3.15	3.15	3.15	
		6.0V		4.2	4.2	4.2	
Maximum Low-Level Input Voltage		2.0V		0.5	0.5	0.5	
	V _{IL}	3.0V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	0.9	0.9	0.9	V
	VIL	4.5V	V _{CC} -0.1V I _{OUT} ≤ 20μA	1.35	1.35	1.35	V
		6.0V	1.0011	1.8	1.8	1.8	

^{4.} $-55^{\circ}C \le T_{J} \le +125^{\circ}C$





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DC Electrical Characteristics Continued (Voltages Referenced to GND)

PARAMETER	SYMBOL	V _{cc}	CONDITIONS		LIM	ITS	UNITS
TATOWNETER	STINIDOL	▼ CC	CONDITIONS	25°C	5°C 85°C	FULL RANGE⁴	Julia
		2.0V	\/ =\/ or\/	1.9	1.9	1.9	V
		4.5V	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 20 \mu A$	4.4	4.4	4.4	
		6.0V	1.0011 = 1	5.9	5.9	5.9	
Minimum High-Level Output Voltage	V _{OH}	3.0V	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 2.4 \text{mA}$	2.48	2.34	2.20	
		4.5V	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 4.0 \text{mA}$	3.98	3.84	3.70	V
		6.0V	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 5.2 \text{mA}$	5.48	5.34	5.20	
		2.0V	$V_{IN} = V_{IL} \text{ or } V_{IL}$ $ I_{OUT} \le 20\mu\text{A}$	0.1	0.1	0.1	V
		4.5V		0.1	0.1	0.1	
		6.0V	1.0011	0.1	0.1	0.1	
Maximum Low-Level Output Voltage	V _{OL}	3.0V	$V_{IN} = V_{IL} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 2.4 \text{mA}$	0.26	0.33	0.40	
, -		4.5V	$V_{IN} = V_{IL} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 4.0 \text{mA}$	0.26	0.33	0.40	V
	6.0V		$V_{IN} = V_{IL} \text{ or } V_{IL}$ $\left I_{OUT} \right \le 5.2 \text{mA}$	0.26	0.33	0.40	
Maximum Input Leakage Current	I _{IN}	6.0V	$V_{IN} = V_{CC}$ or GND	±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Leakage Current	I _{CC}	6.0V	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\mu A$	1	10	40	μА

AC Electrical Characteristics⁵

PARAMETER	SYMBOL	V _{cc}	CONDITIONS	LIMITS			
	OTHIBOL	- VCC CONDITION	CONDITIONS	25°C	85°C	FULL RANGE⁴	UNITS
Maximum Propagation Delay, Input A or B to Output Y		2.0V	$\begin{array}{c c} 2.0V \\ \hline 3.0V \\ \hline 4.5V \\ \end{array}$ $\begin{array}{c c} C_L = 50 pF, \\ \hline t_r = t_f = 6 ns \\ \end{array}$	75	95	110	
	II tың tын 🗀	3.0V		30	40	55	ns
		4.5V		15	19	22	
(Figure 1,2)		6.0V	13	16	19		
Maximum Output Rise	e, t _{TLH,} t _{THL} 3.0V	2.0V	C _L = 50pF,	75	95	110	ns
and Fall Time, Any Output (Figure 1,2)		3.0V		27	32	36	
		4.5V	$t_r = t_f = 6$ ns	15	19	22	113
		6.0V		13	16	19	

 $[\]textbf{5.} \ \ \text{Not production tested in die form, characterized by chip design and tested in package}.$





AC Electrical Characteristics Continued⁵

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PARAMETER	SYMBOL	Voc	V _{cc} CONDITIONS		LIM	ITS	UNITS
	01111202	• 66	CONDITIONS	25°C	85°C	FULL RANGE⁴	Julio
Maximum Input Capacitance	C _{IN}	-	-	10	10	10	pF
Power Dissipation Capacitance Per Gate ⁶	C _{PD}	-	$T_A = 25^{\circ}C,$ $V_{CC} = 5.0V$		TYPI		pF

^{6.} Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

Switching Waveform

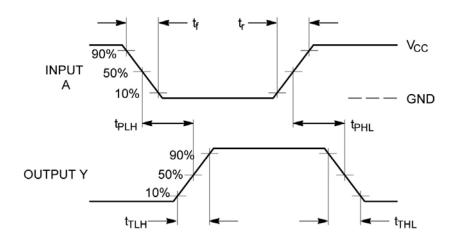
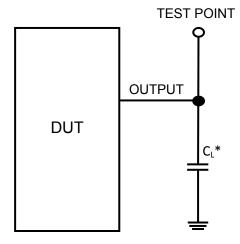


Figure 1 – Propagation Delay & Output Transition Time

Test Circuit



^{*} Includes all probe and jig capacitance

Figure 2

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