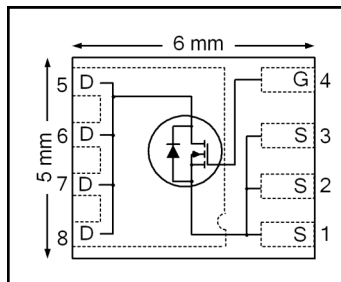


**Application**

- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- DC/DC converters
- DC/AC Inverters

HEXFET® Power MOSFET



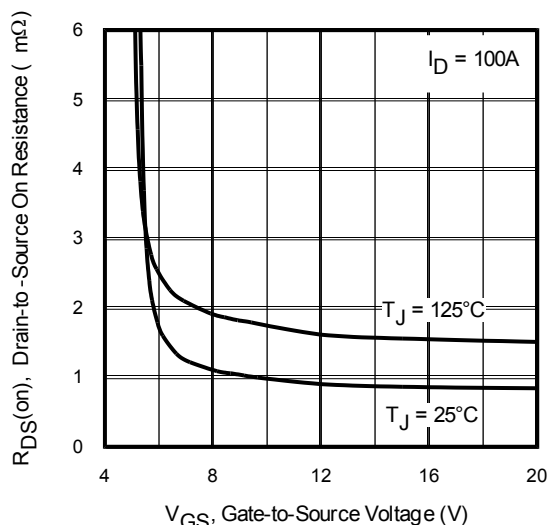
<b>V<sub>DSS</sub></b>	<b>40V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>0.95mΩ</b>
<b>max</b>	<b>1.25mΩ</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>265A①</b>
<b>I<sub>D</sub> (Package Limited)</b>	<b>100A①</b>

**Benefits**

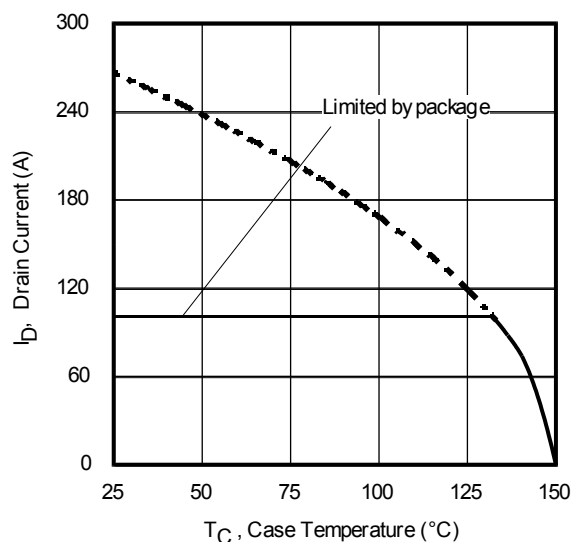
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant



Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH7084PbF	PQFN 5mm x 6mm	Tape and Reel	4000	IRFH7084TRPbF



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	40	A
$I_D @ T_{C(\text{Bottom})} = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	265 <sup>①</sup>	
$I_D @ T_{C(\text{Bottom})} = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	170 <sup>①</sup>	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	100 <sup>①</sup>	
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	400	A
	Linear Derating Factor	1.25	W/°C
$P_D @ T_C = 25^\circ\text{C}$	Max Power Dissipation <sup>⑧</sup>	156	
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>③</sup>	185	mJ
$E_{AS}$ (tested)	Single Pulse Avalanche Energy Tested Value <sup>⑨</sup>	370	
$I_{AR}$	Avalanche Current <sup>②</sup>	See Fig 14, 15, 23a,	A
$E_{AR}$	Repetitive Avalanche Energy <sup>②</sup>		mJ

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case <sup>⑧</sup>	0.5	0.8	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case <sup>⑧</sup>	—	21	
$R_{\theta JA}$	Junction-to-Ambient <sup>⑩</sup>	—	35	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient <sup>⑩</sup>	—	20	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.034	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.95	1.25	m $\Omega$	$V_{GS} = 10\text{V}, I_D = 100\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.2	—	3.9	V	$V_{DS} = V_{GS}, I_D = 150\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	$\mu\text{A}$	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Gate Resistance	—	1.4	—	$\Omega$	

**Notes:**

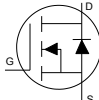
- ① Calculated continuous current based on maximum allowable junction temperature. Package is limited to 100A by production test capability.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.037\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 100\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ④  $I_{SD} \leq 100\text{A}$ ,  $di/dt \leq 994\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150^\circ\text{C}$ .
- ⑤ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑥  $C_{OSS}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $C_{OSS}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑧  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑨ This value determined from sample failure population, starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.037\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 100\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ⑩ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:

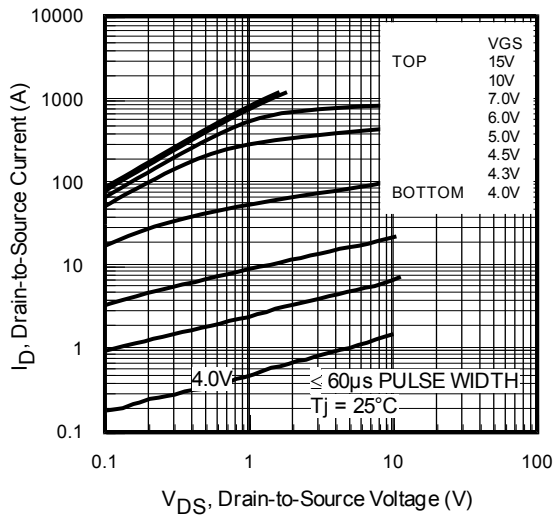
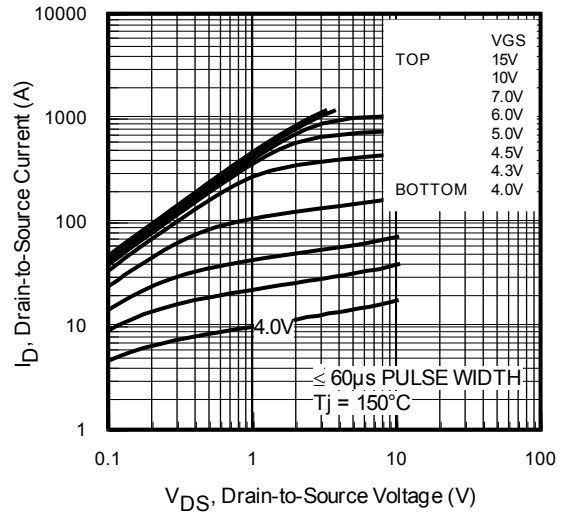
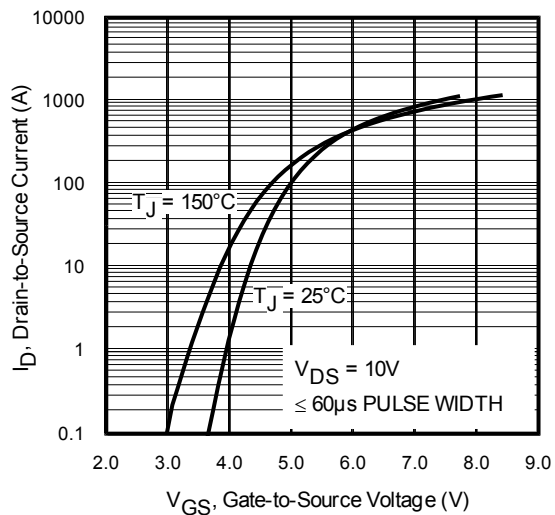
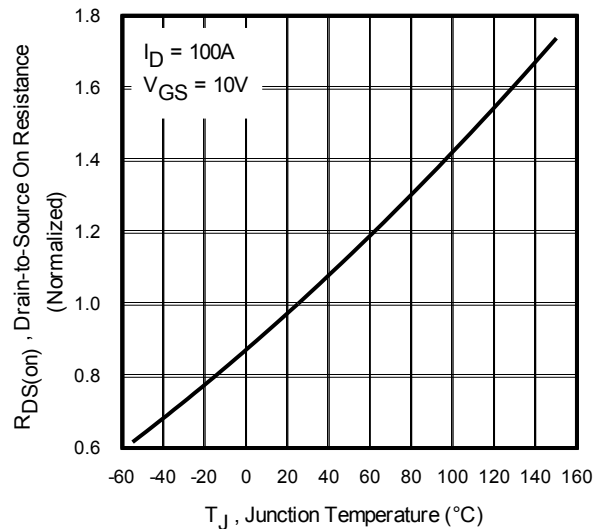
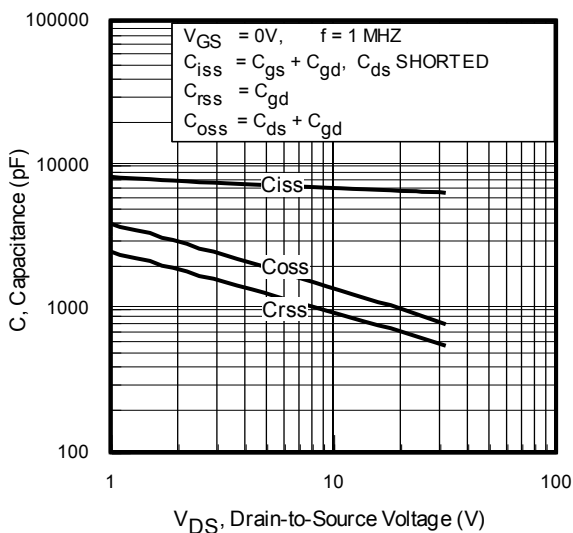
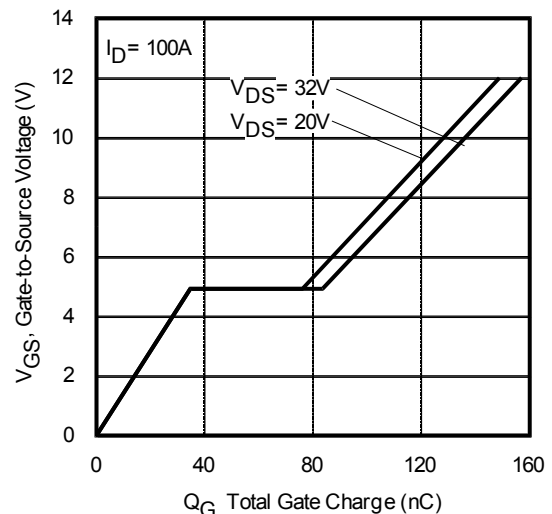
<http://www.irf.com/technical-info/appnotes/an-994.pdf>

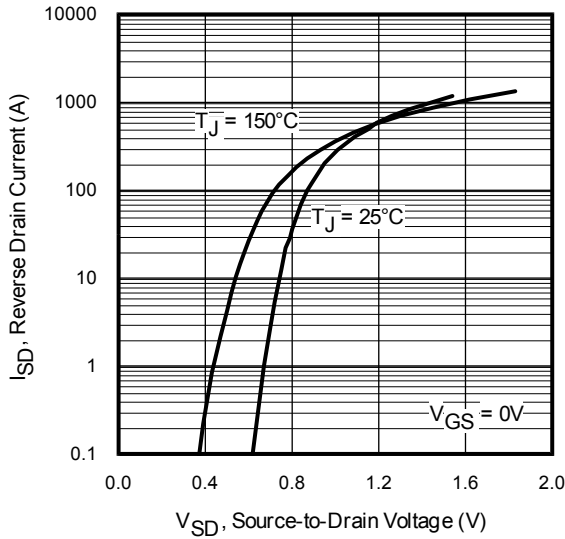
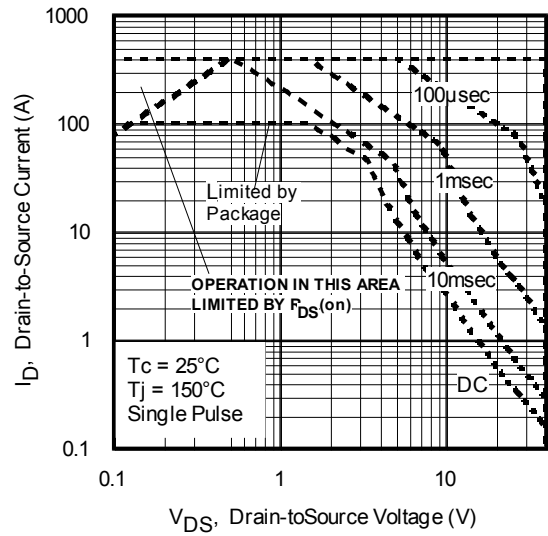
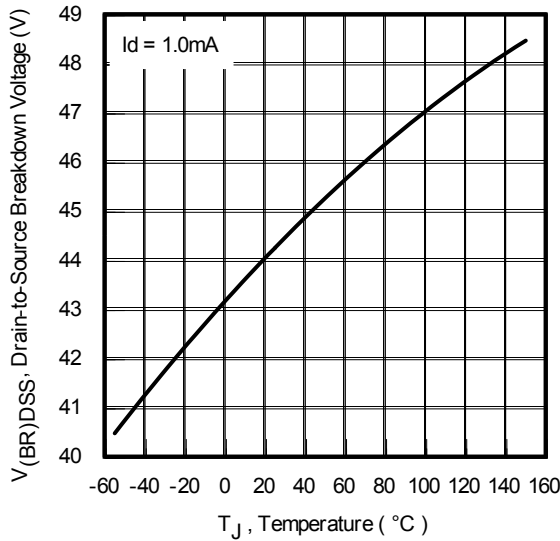
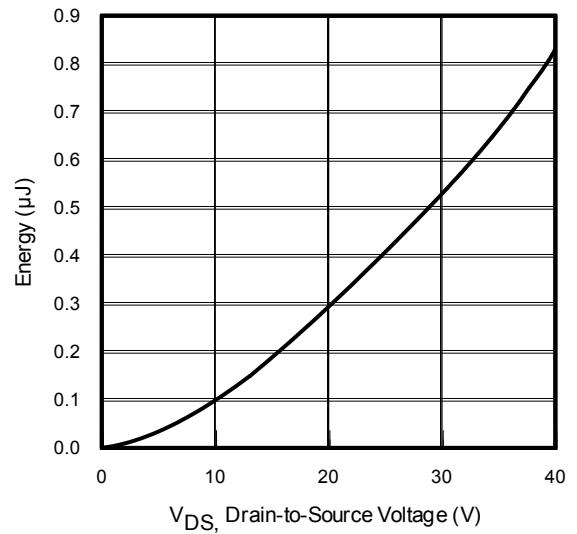
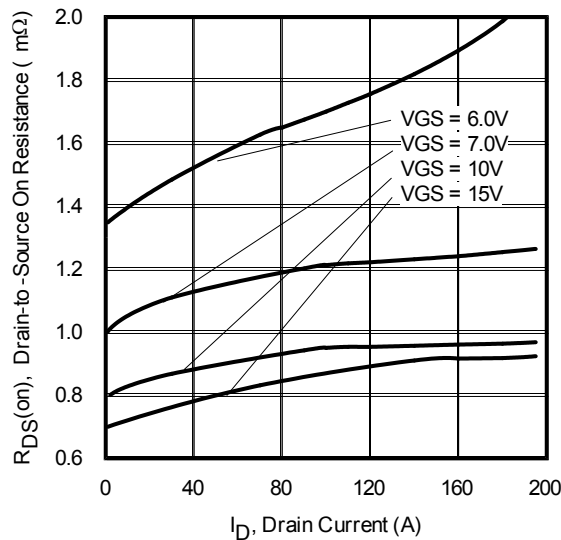
**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

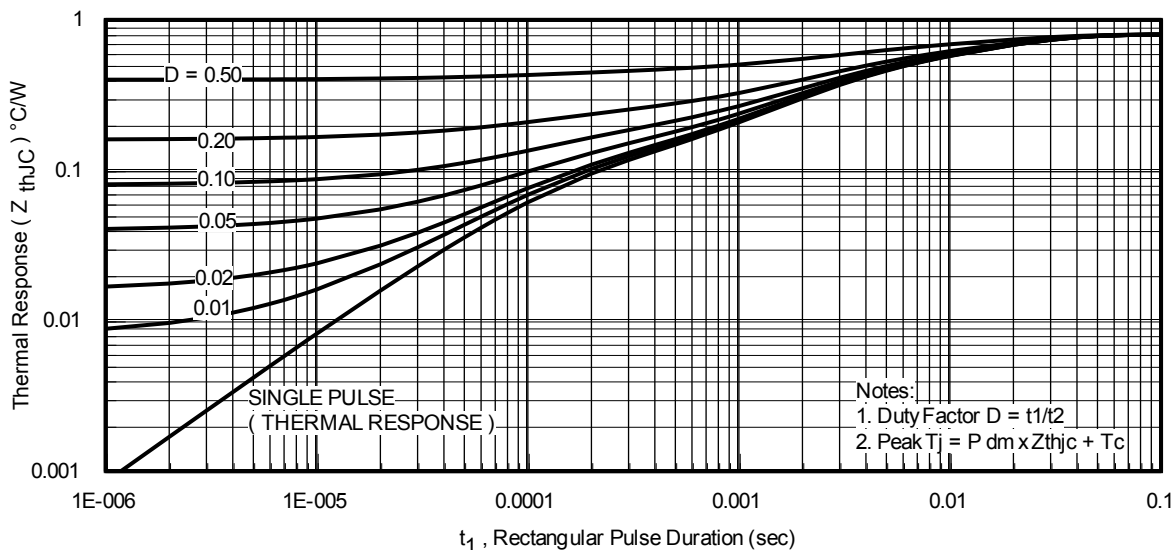
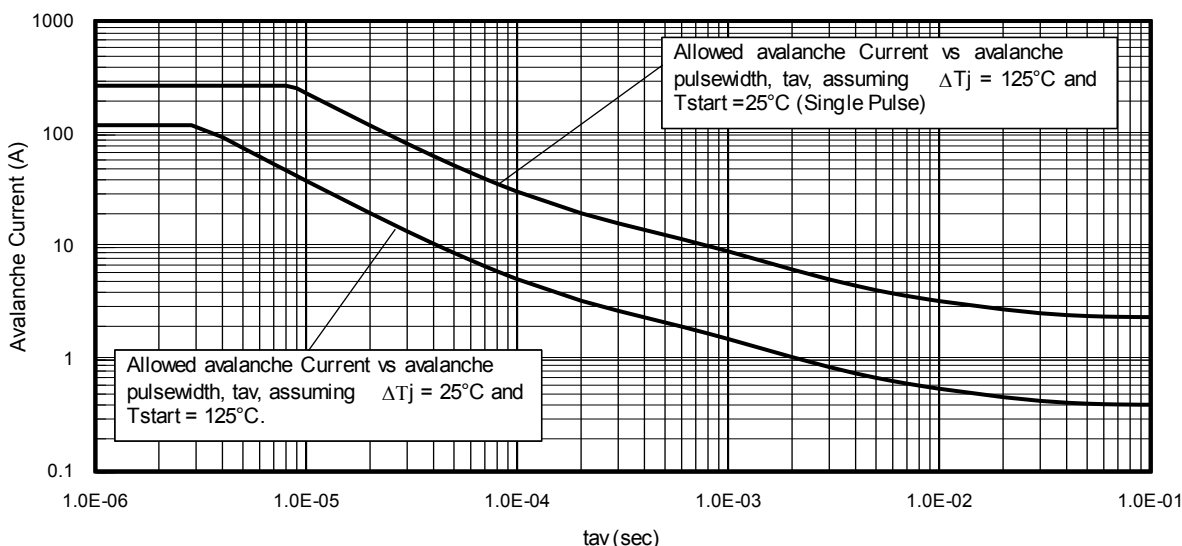
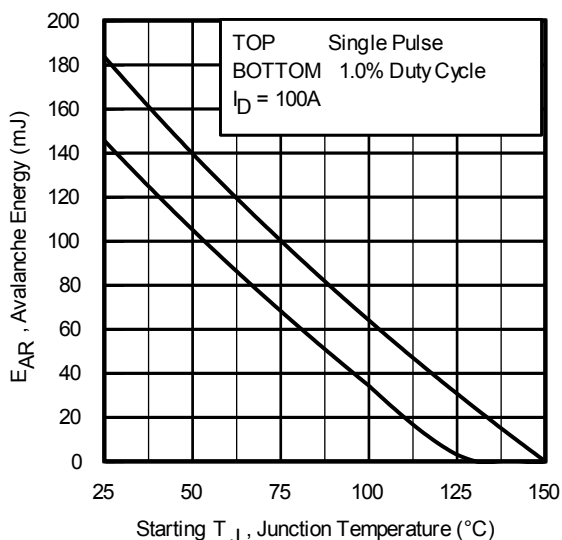
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	120	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 100A
Q <sub>g</sub>	Total Gate Charge	—	127	190	nC	I <sub>D</sub> = 100A V <sub>DS</sub> = 20V V <sub>GS</sub> = 10V
Q <sub>gs</sub>	Gate-to-Source Charge	—	35	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	41	—		
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> – Q <sub>gd</sub> )	—	195	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	16	—	ns	V <sub>DD</sub> = 20V I <sub>D</sub> = 30A R <sub>G</sub> = 2.7Ω V <sub>GS</sub> = 10V <sup>⑤</sup>
t <sub>r</sub>	Rise Time	—	31	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	64	—		
t <sub>f</sub>	Fall Time	—	34	—		
C <sub>iss</sub>	Input Capacitance	—	6560	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz, See Fig.5 V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 32V <sup>⑦</sup> See Fig.11 V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 32V <sup>⑥</sup>
C <sub>oss</sub>	Output Capacitance	—	940	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	650	—		
C <sub>oss eff.(ER)</sub>	Effective Output Capacitance (Energy Related)	—	1120	—		
C <sub>oss eff.(TR)</sub>	Output Capacitance (Time Related)	—	1300	—		

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode) <sup>①</sup>	—	—	100 <sup>①</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①</sup>	—	—	400		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 100A, V <sub>GS</sub> = 0V <sup>⑤</sup>
dv/dt	Peak Diode Recovery dv/dt <sup>④</sup>	—	4.5	—	V/ns	T <sub>J</sub> = 150°C, I <sub>S</sub> = 100A, V <sub>DS</sub> = 40V <sup>⑤</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	36 37	—	ns	V <sub>DD</sub> = 34V I <sub>F</sub> = 100A, di/dt = 100A/μs <sup>⑤</sup>
Q <sub>rr</sub>	Reverse Recovery Charge	—	38 40	—		
I <sub>RRM</sub>	Reverse Recovery Current	—	1.7	—	A	T <sub>J</sub> = 25°C


**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 11.** Drain-to-Source Breakdown Voltage

**Fig 12.** Typical  $C_{oss}$  Stored Energy

**Fig 13.** Typical On-Resistance vs. Drain Current


**Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 15. Typical Avalanche Current vs. Pulse width**

**Fig 16. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 14, 15:  
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)  
 $P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{thJC} ]$   
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$

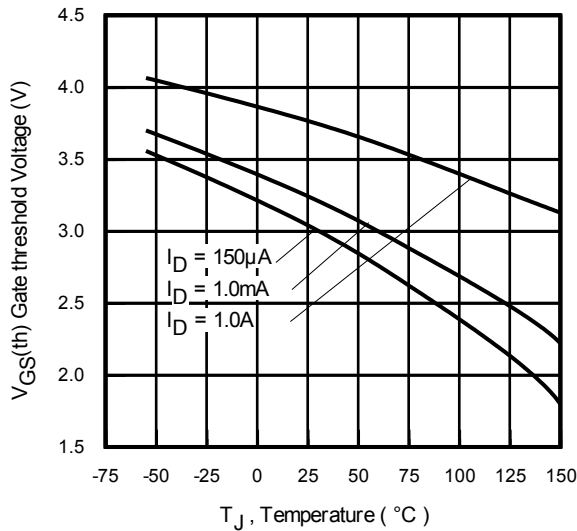


Fig 17. Threshold Voltage vs. Temperature

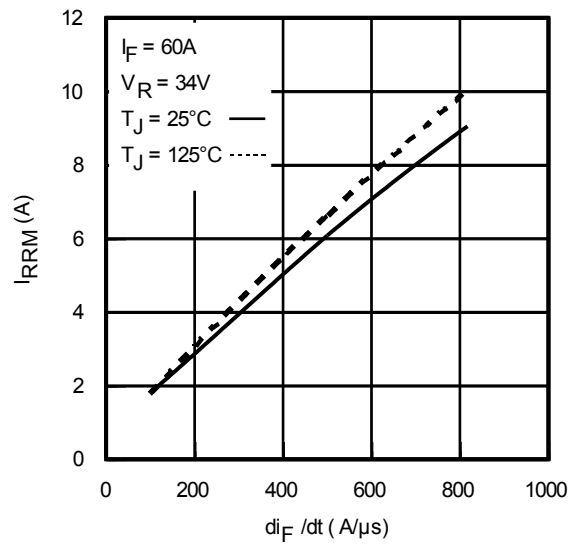


Fig 18. Typical Recovery Current vs. dif/dt

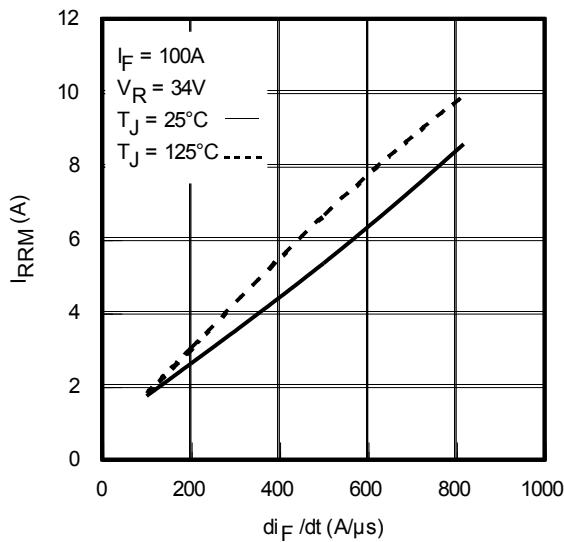


Fig 19. Typical Recovery Current vs. dif/dt

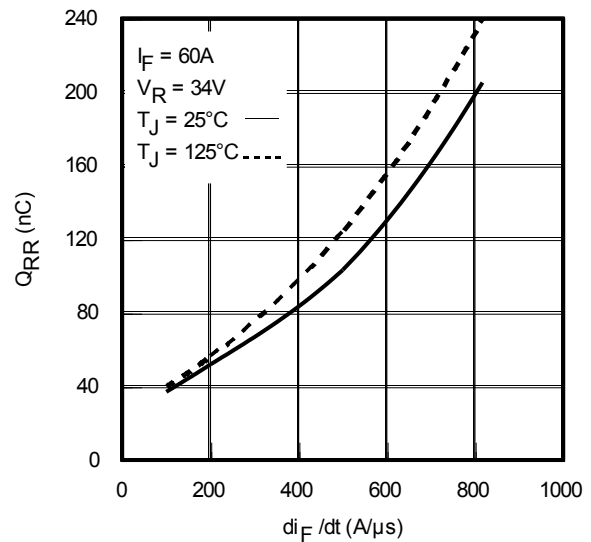


Fig 20. Typical Stored Charge vs. dif/dt

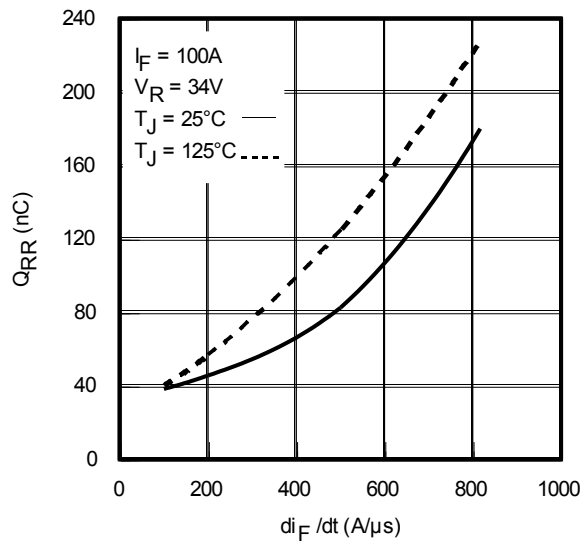
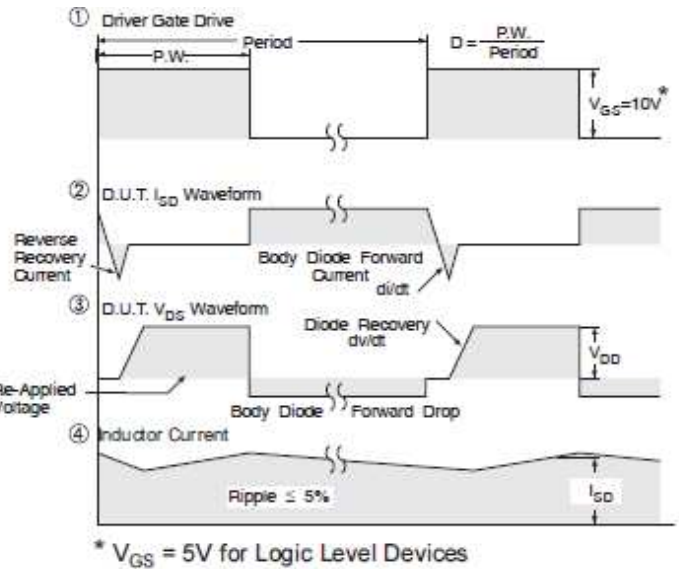
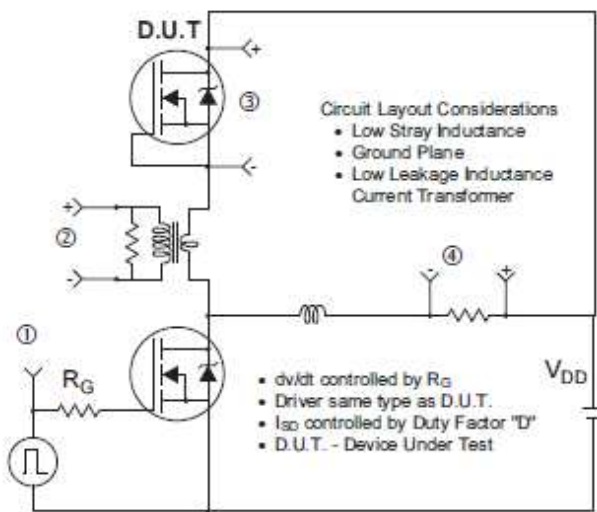
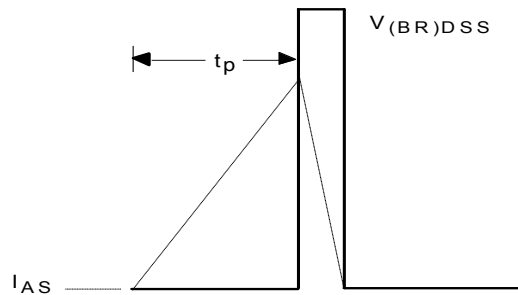
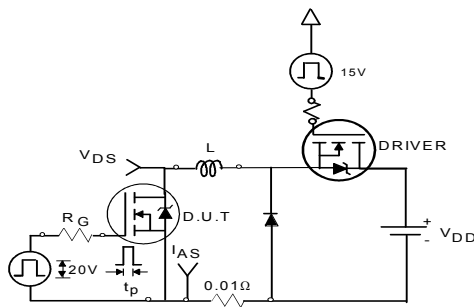


Fig 21. Typical Stored Charge vs. dif/dt

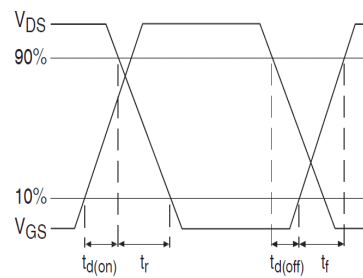
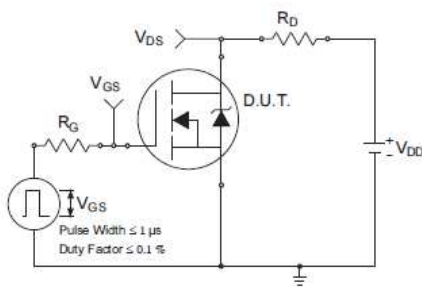


**Fig 22.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



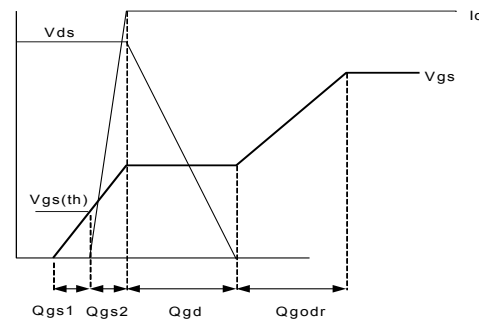
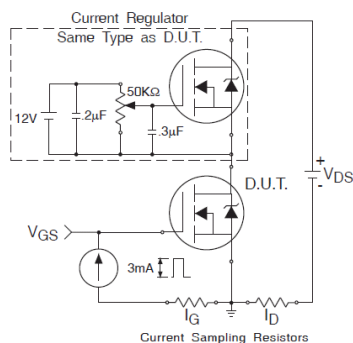
**Fig 23a.** Unclamped Inductive Test Circuit

**Fig 23b.** Unclamped Inductive Waveforms



**Fig 24a.** Switching Time Test Circuit

**Fig 24b.** Switching Time Waveforms

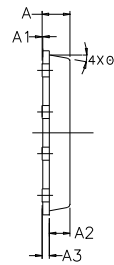


**Fig 25a.** Gate Charge Test Circuit

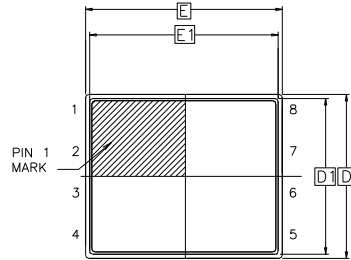
**Fig 25b.** Gate Charge Waveform



PQFN 5x6 Outline "B" Package Details

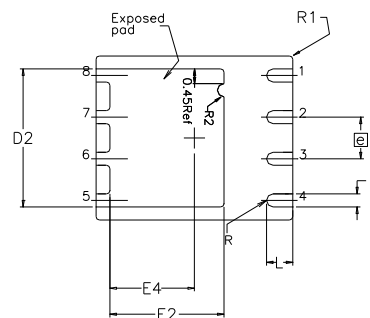


SIDE VIEW



TOP VIEW

DIM SYMBOL	MIN	NOM	MAX
A	0.800	0.830	1.05
A1	0.000	0.020	0.050
A2	0.580	0.630	0.680
A3	0.254 REF		
Ø	0"	10"	12"
b	0.350	0.400	0.470
D	4.850	5.000	5.150
D1	4.675	4.750	5.000
D2	3.700	4.210	4.300
e	1.270 BSC		
E	5.850	6.000	6.150
E1	5.675	5.750	6.000
E2	3.380	3.480	3.760
E4	2.480	2.580	2.680
L	0.550	0.800	0.900
R	0.200 REF		
R1	0.100 REF		
R2	0.150	0.200	0.250

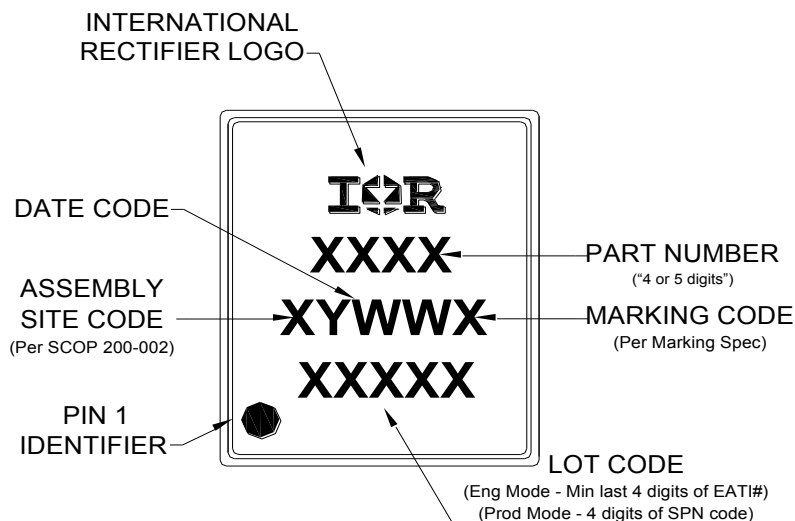


BOTTOM VIEW

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

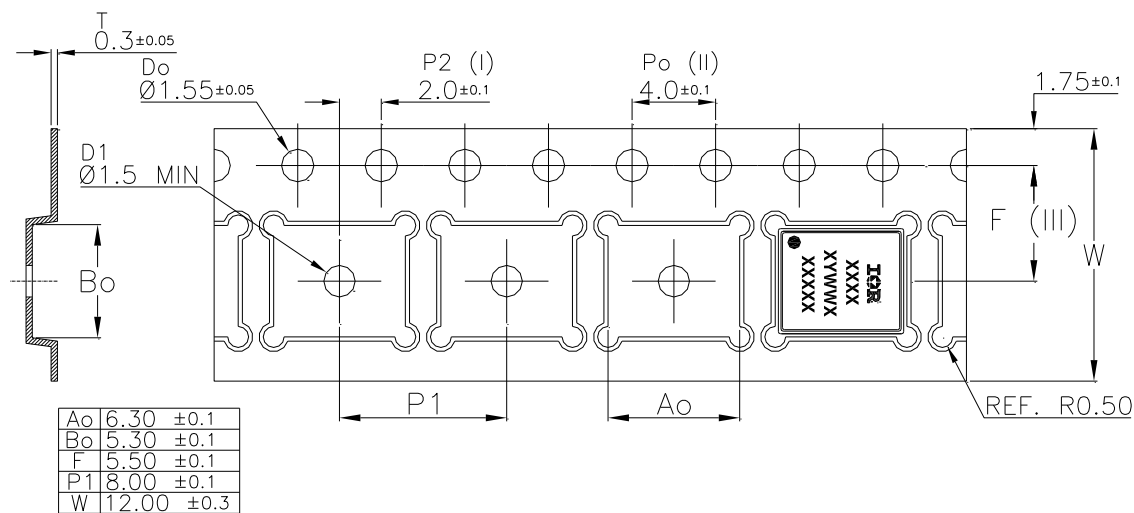
For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN 5x6 Outline "B" Part Marking



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**PQFN 5x6 Outline "B" Tape and Reel**



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification information<sup>†</sup>**

Qualification level	Industrial <sup>††</sup>	
	(per JEDEC JESD47F <sup>†††</sup> guidelines )	
Moisture Sensitivity Level	PQFN 5mmx 6mm	MSL1
		(per JEDEC J-STD-020D <sup>†††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: <http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
10/16/14	• Add Pd at tc=25C on page 1