HM514260DI Serie

262,144-word × 16-bit Dynamic RAM

HITACHI

ADE-203-710A (Z)
Rev. 1.0
Feb. 13, 1997

Description

The Hitachi HM514260DI is a CMOS dynamic RAM organized as 262,144 words × 16 bits. The HM514260DI realizes higher density, higher performance, and various functions by employing 0.8 µm CMOS process technology and new CMOS circuit design technologies. The HM514260DI offers fast pag mode as a high-speed access mode. It is packaged in a standard 400-mil 40-pin plastic SOJ.

Features

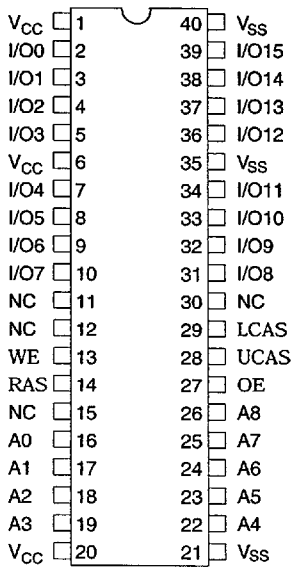
- Single 5-V supply: 5V ± 10%
- Access time: 70 ns/80 ns (max)
- Power dissipation:
  - — Active mode: 770 mW/688 mW (max)
  - — Standby mode:
    - 11 mW (max)
    - 1.1 mW (max) (L-version)
- Fast page mode capability
- 512 refresh cycles:
  - — 8 ms
  - — 128 ms (L-version)
- Two CAS byte control
- Two variations of refresh:
  - — RAS-only refresh
  - — CAS-before-RAS refresh
- Battery back up operation (L-version)
- Operating temperature range: –40 to 85°C

Ordering Information

Type No.	Access Time	Package
HM514260DJI-7 HM514260DJI-8	70 ns 80 ns	400-mill 40-pin plastic SOJ (CP-40D)
HM514260DLJI-7 HM514260DLJI-8	70 ns 80 ns	400-mill 40-pin plastic SOJ (CP-40D)

Pin Arrangement

HM514260DJI/DLJI Series

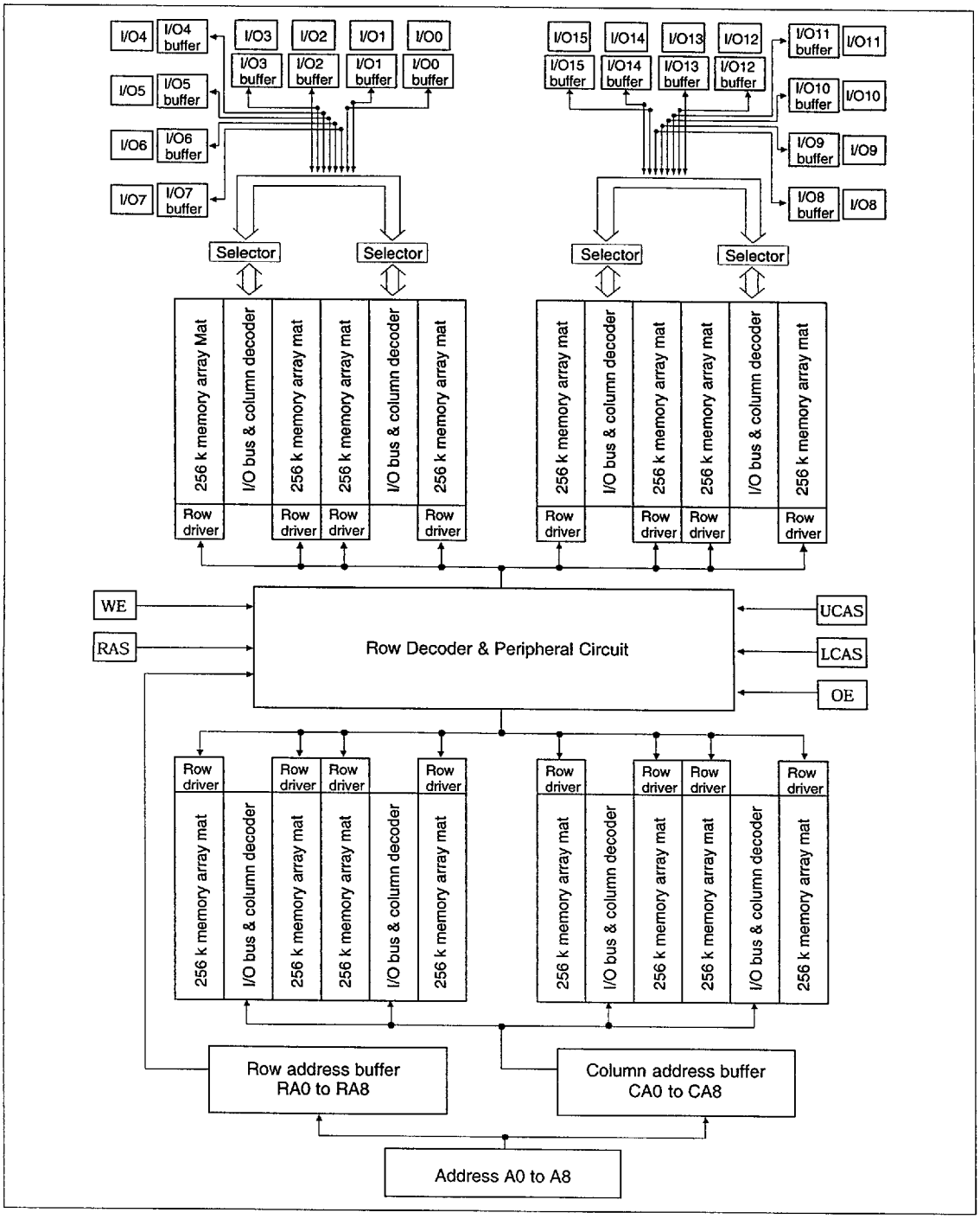


(Top view)

Pin Description

Pin Name	Function
A0 to A8	Address input: • Row address: A0 to A8 • Column address: A0 to A8 • Refresh address: A0 to A8
I/O0 to I/O15	Data input/output
RAS	Row address strobe
UCAS, LCAS	Column address strobe
WE	Read/write enable
OE	Output enable
V_{cc}	Power supply
V_{ss}	Ground
NC	No connection

Block Diagram



Operation Mode

The HM514260DI series has the following ten operation modes.

1. Read cycle
2. Early write cycle
3. Delayed write cycle
4. Read-modify-write cycle
5. RAS-only refresh cycle
6. CAS-before-RAS refresh cycle
7. Fast page mode read cycle
8. Fast page mode early write cycle
9. Fast page mode delayed write cycle
10. Fast page mode read-modify-write cycle

	Inputs					
RAS	**LCAS**	**UCAS**	**WE**	**OE**	**Output**	**Operation**
H	H	H	D	D	Open	Standby
H	L	L	H	L	Valid	Standby
L	L	L	H	L	Valid	Read cycle
L	L	L	L*2	D	Open	Early write cycle
L	L	L	L*2	H	Undefined	Delayed write cycle
L	L	L	H to L	L to H	Valid	Read-modify-write cycle
L	H	H	D	D	Open	RAS-only refresh cycle
H to L	H	L	D	D	Open	CAS-before-RAS refresh cycle or
	L	H				
	L	L				
L	H to L	H to L	H	L	Valid	Fast page mode read cycle
L	H to L	H to L	L*2	D	Open	Fast page mode early write cycle
L	H to L	H to L	L*2	H	Undefined	Fast page mode delayed write cycle
L	H to L	H to L	H to L	L to H	Valid	Fast page mode read-modify-write cycle
L	L	L	H	H	Open	Read cycle (Output disabled)

Notes: 1. H: High (inactive), L: Low (active), D: H or L

2. $t_{WCS} \geq 0$ ns Early write cycle
   $t_{WCS} < 0$ ns Delayed write cycle
3. Mode is determined by the OR function of the UCAS and LCAS. (Mode is set by the earliest of UCAS and LCAS active edge and reset by the latest of UCAS and LCAS inactive edge.) However, write operation and output High-Z control are done independently by each UCAS, LCAS.
   ex. if RAS = H to L, LCAS = L, UCAS = H, then CAS-before-RAS refresh cycle is selected.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	−40 to +85	°C
Storage temperature range	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = −40 to +85° C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	2
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1, 2
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Notes: 1. All voltage referred to V_{SS}
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics (Ta = –40 to +85°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM514260DI					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current*1, *2	I_{CC1}	—	140	—	125	mA	RAS, UCAS or LCAS cycling t_{RC} = min
Standby current	I_{CC2}	—	2	—	2	mA	TTL interface RAS, UCAS, LCAS = V_{IH} Dout = High-Z
Standby current		—	1	—	1	mA	CMOS interface RAS, UCAS, LCAS, WE, OE ≥ V_{CC} – 0.2 V Dout = High-Z
Standby current (L-version)	I_{CC2}	—	200	—	200	µA	CMOS interface RAS, UCAS, LCAS, OE, WE ≥ V_{CC} – 0.2 V Dout = High-Z
RAS-only refresh current*2	I_{CC3}	—	130	—	110	mA	t_{RC} = min
CAS-before-RAS refresh current*2	I_{CC6}	—	130	—	120	mA	t_{RC} = min
Fast page mode current*1, *3	I_{CC7}	—	130	—	120	mA	t_{PC} = min
Battery backup current*4 (Standby with CBR refresh) (L-version)	I_{CC10}	—	300	—	300	µA	Standby: CMOS interface Dout = High-Z CBR refresh: t_{RC} = 250 µs t_{RAS} ≤ 1 µs, UCAS, LCAS = V_{IL} WE, OE = V_{IH}
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 6.5 V
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 6.5 V, Dout = disable
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5.0 mA
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified as the output open condition.
2. Address can be changed once (or not at all) while RAS = V_{IL}.
3. Address can be changed once (or not at all) while UCAS and LCAS = V_{IH}.
4. V_{IH} ≥ V_{CC} – 0.2 V, 0 ≤ V_{IL} ≤ 0.2 V; address can be changed once (or not at all) while RAS = V_{IL}
5. All the V_{CC} pins must be supplied with the same voltage, and all the V_{SS} pins must be supplied with the same voltage.

Capacitance (Ta = +25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton meter or other effective capacitance measuring method.
2. UCAS and LCAS = V_{IH} to disable Dout

AC Characteristics (Ta = –40 to +85°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *14, *15, *17, *18

Test Conditions

- Input rise and fall time: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Input levels: 0 V, 3 V
- Output load: 2 TTL gate + C_L (100 pF), including scope and jig

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

		HM514260DI					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	130	—	150	—	ns	
RAS precharge time	t_{RP}	50	—	60	—	ns	
RAS pulse width	t_{RAS}	70	10000	80	10000	ns	
CAS pulse width	t_{CAS}	20	10000	20	10000	ns	23
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	19
Column address hold time	t_{CAH}	15	—	15	—	ns	19
RAS to CAS delay time	t_{RCD}	20	50	20	60	ns	8
RAS to column address delay time	t_{RAD}	15	35	15	40	ns	9
RAS hold time	t_{RSH}	20	—	20	—	ns	
CAS hold time	t_{CSH}	70	—	80	—	ns	
CAS to RAS precharge time	t_{CRP}	15	—	15	—	ns	20
OE to Din delay time	t_{ODD}	20	—	20	—	ns	
OE delay time from Din	t_{DZO}	0	—	0	—	ns	
CAS setup time from Din	t_{DZC}	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	7
Refresh period	t_{REF}	—	8	—	8	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	ms	

Read Cycle

		HM514260DI					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Access time from RAS	t_{RAC}	—	70	—	80	ns	2, 3
Access time from CAS	t_{CAC}	—	20	—	20	ns	3, 4, 13
Access time from address	t_{AA}	—	35	—	40	ns	3, 5, 13
Access time from OE	t_{OAC}	—	20	—	20	ns	23
Read command setup time	t_{RCS}	0	—	0	—	ns	19
Read command hold time to CAS	t_{RCH}	0	—	0	—	ns	16, 20
Read command hold time to RAS	t_{RRH}	0	—	0	—	ns	16
Column address to RAS lead time	t_{RAL}	35	—	40	—	ns	
Output buffer turn-off time	t_{OFF1}	0	15	0	15	ns	6
Output buffer turn-off to OE	t_{OFF2}	0	15	0	15	ns	6
CAS to Din delay time	t_{CDD}	15	—	15	—	ns	

Write Cycle

		HM514260DI					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	ns	10, 19
Write command hold time	t_{WCH}	15	—	15	—	ns	19
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to RAS lead time	t_{RWL}	20	—	20	—	ns	
Write command to CAS lead time	t_{CWL}	20	—	20	—	ns	21
Data-in setup time	t_{DS}	0	—	0	—	ns	11, 21
Data-in hold time	t_{DH}	15	—	15	—	ns	11, 21
CAS to OE delay time	t_{COD}	—	0	—	0	ns	19, 23

Read-Modify-Write Cycle

		HM514260DI					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	180	—	200	—	ns	
RAS to WE delay time	t_{RWD}	95	—	105	—	ns	10
CAS to WE delay time	t_{CWD}	45	—	45	—	ns	10
Column address to WE delay time	t_{AWD}	60	—	65	—	ns	10
OE hold time from WE	t_{OEH}	20	—	20	—	ns	

Refresh Cycle

		HM514260DI					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
CAS setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	ns	19
CAS hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	20
RAS precharge to CAS hold time	t_{RPC}	10	—	10	—	ns	19
CAS precharge time in normal mode	t_{CPN}	10	—	10	—	ns	22

Fast Page Mode Cycle

		HM514260DI					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	45	—	50	—	ns	
Fast page mode CAS precharge time	t_{CP}	10	—	10	—	ns	22
Fast page mode RAS pulse width	t_{RASC}	—	100000	—	100000	ns	12
Access time from CAS precharge	t_{ACP}	—	40	—	45	ns	3, 13, 20
RAS hold time from CAS precharge	t_{RHCP}	40	—	45	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514260DI -7 Min	HM514260DI -7 Max	HM514260DI -8 Min	HM514260DI -8 Max	Unit	Notes
Fast page mode read-modify-write cycle CAS precharge to WE delay time	t_{CPW}	65	—	70	—	ns	
Fast page mode read-modify-write cycle time	t_{PCM}	95	—	100	—	ns	

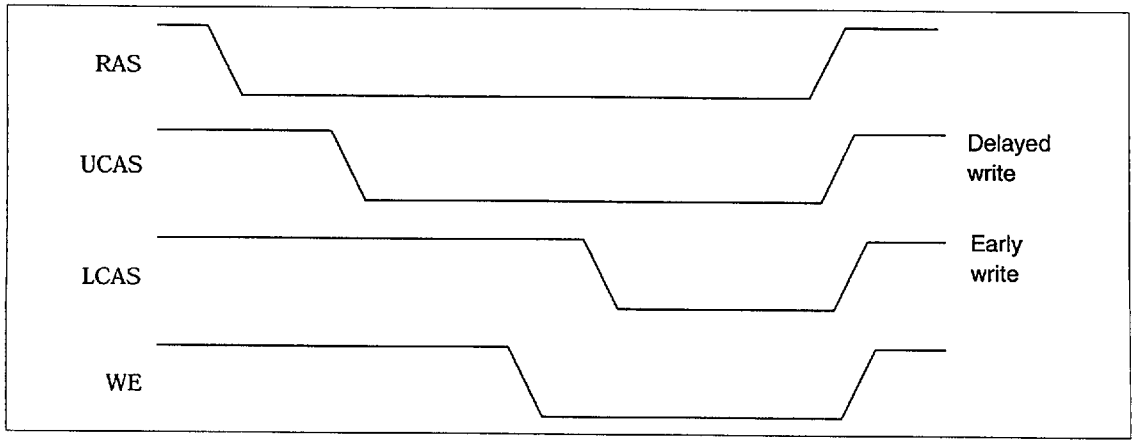
Notes:
1. AC measurements assume t_T = 5 ns, V_{IH} = 3.0 V, V_{IL} = 0.0 V.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in this data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referred to CAS leading edge in an early write cycle and to WE leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines RAS pulse width in fast page mode cycles.
13. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{ACP}.
14. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles (RAS-only refresh cycle or CAS-before-RAS refresh cycle). If the internal refresh counter is used, a minimum of eight CAS-before-RAS refresh cycles is required.
15. In delayed write or read-modify-write cycles, OE must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
17. When both UCAS and LCAS go low at the same time, all 16-bits data are written into the device. UCAS and LCAS cannot be staggered within the same write/read cycles.
18. All the V_{CC} and V_{SS} pins must be supplied with the same voltages.
19. t_{COD}, t_{ASC}, t_{CAH}, t_{RCS}, t_{WCS}, t_{WCH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of UCAS or LCAS.
20. t_{CRP}, t_{CHR}, t_{ACP} t_{RCH} and t_{CPW} are determined by the later rising edge of UCAS or LCAS.
21. t_{CWL}, t_{DH} and t_{DS} should be satisfied by both UCAS and LCAS.
22. t_{CPN} and t_{CP} are determined by the time that both UCAS and LCAS are high.

23. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When the output buffer is turned on and off within a very short time, it generally cause large V_{CC}/V_{SS} line noise, which degrades the V_{IH} min/V_{IL} max level.
24. XXX: H or L (H: V_{IH} (Min) ≤ V_{IN} ≤ V_{IH} (Max), L: V_{IL} (Min) ≤ V_{IN} ≤ V_{IL} (Max))
    ///////: Invalid Dout
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL}.

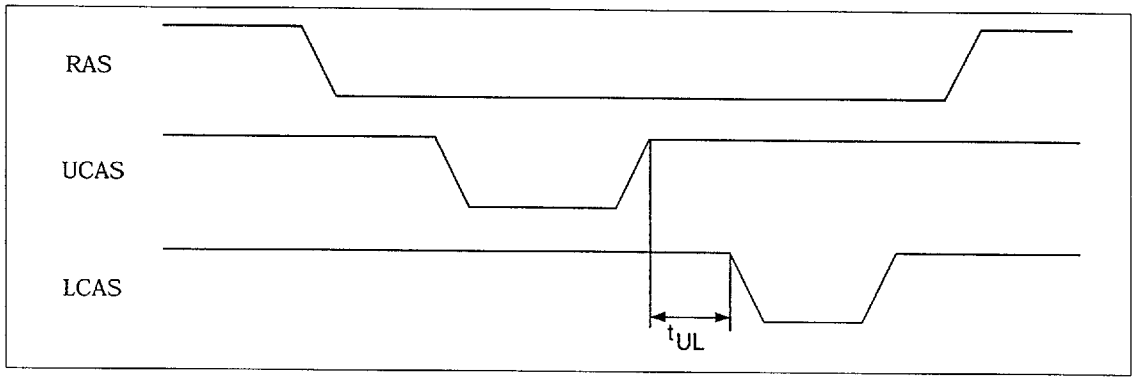
Notes Concerning 2CAS Control

Please do not intentionally separate the UCAS/LCAS operation timing. However, skew between UCAS/LCAS is allowed under the following conditions:

1. Each of the UCAS/LCAS should satisfy the timing specifications individually.
2. Different operation modes for upper and lower bytes, such as shown in the figure below, are not allowed:



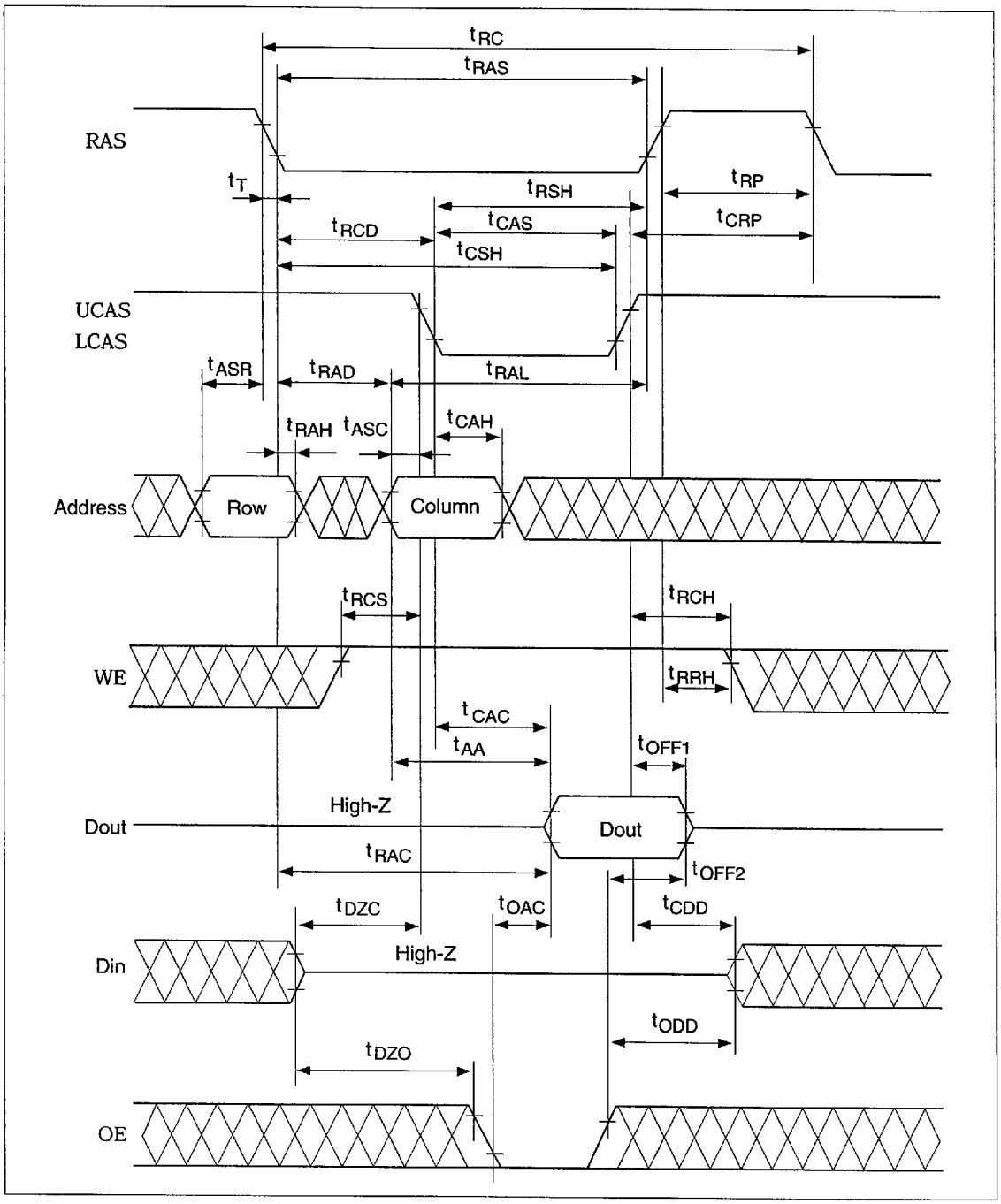
3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, fast page mode can be performed:



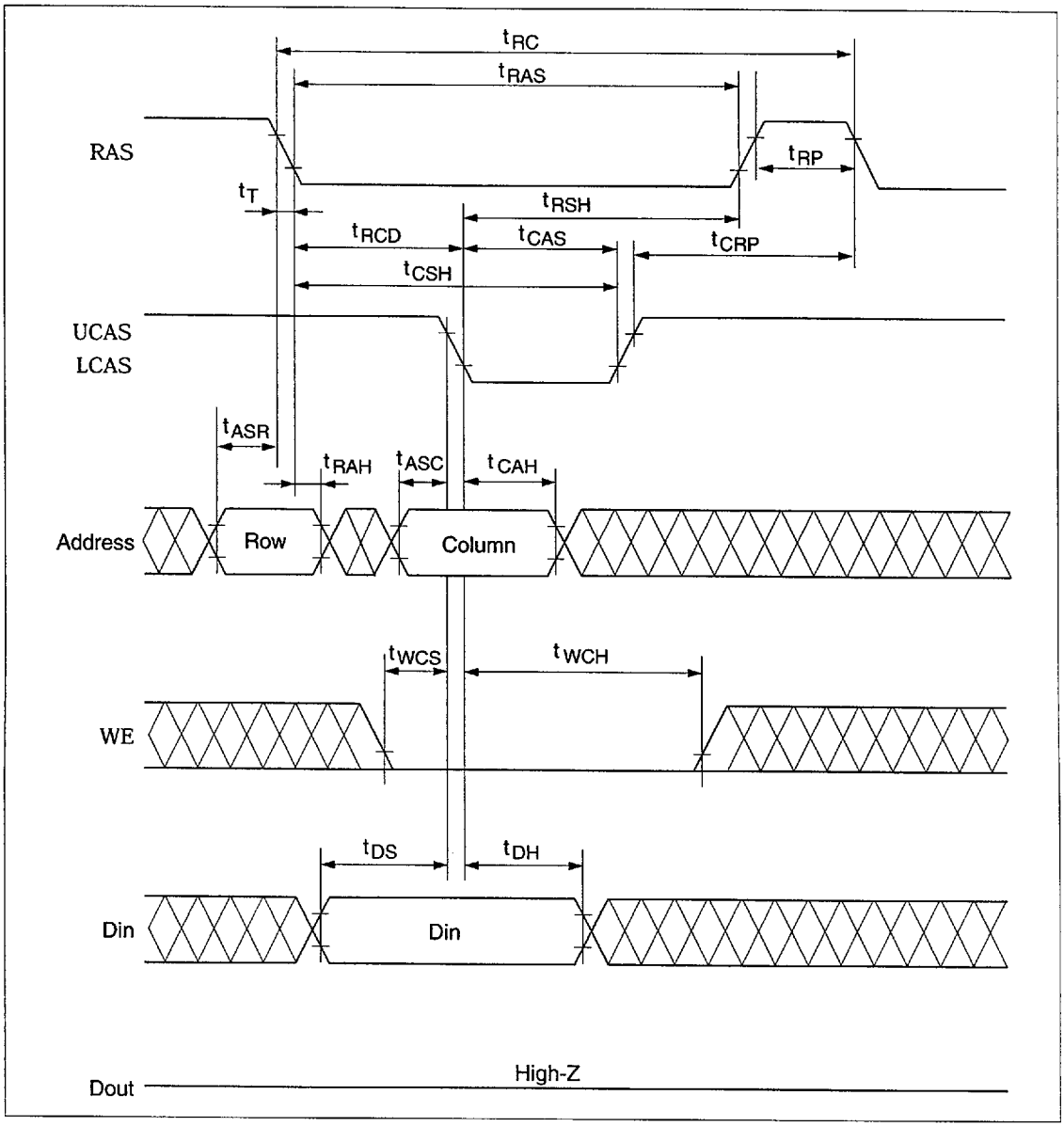
4. Byte control operation by remaining UCAS or LCAS high is guaranteed.

Timing Waveforms*[24]

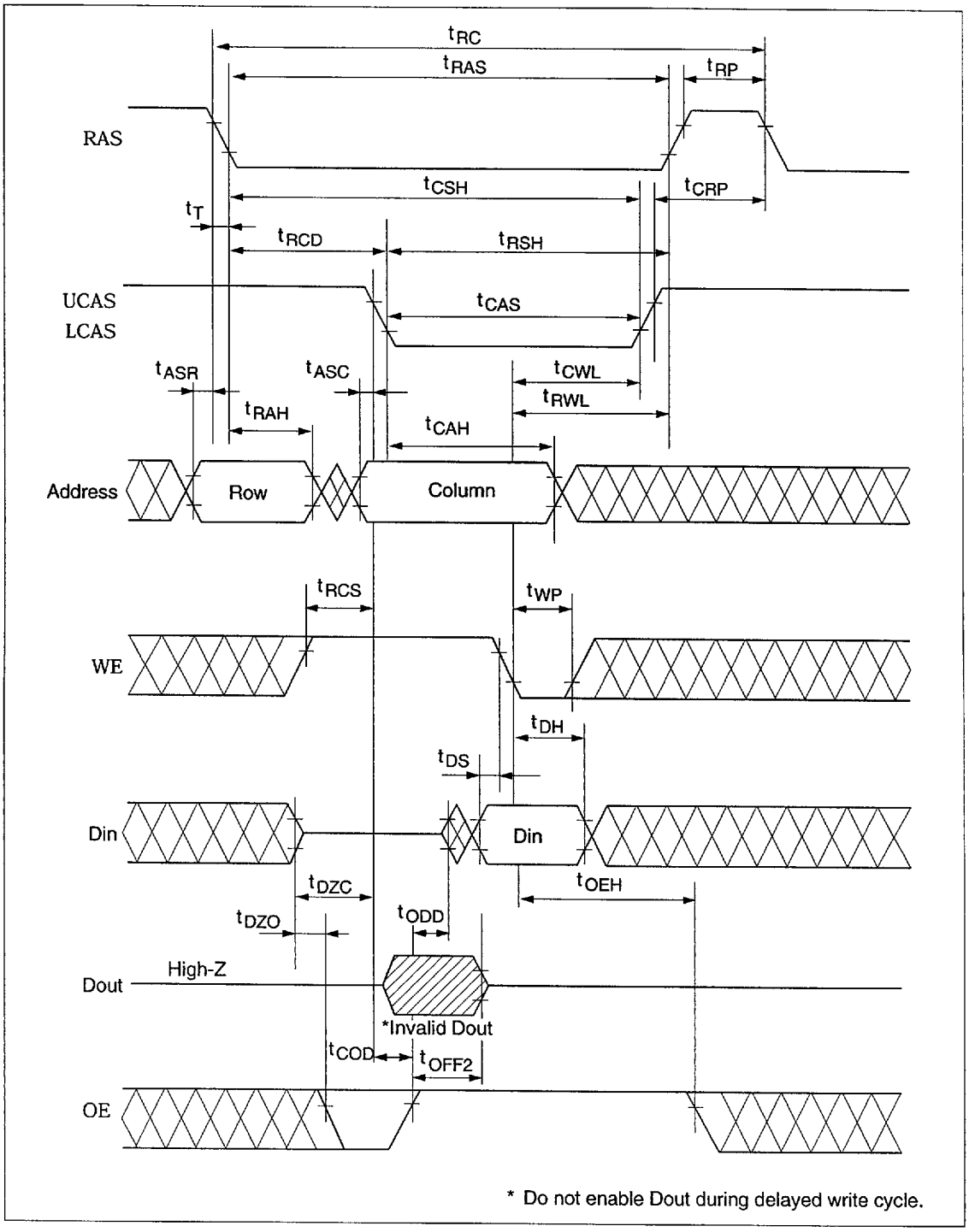
Read Cycle



Early Write Cycle

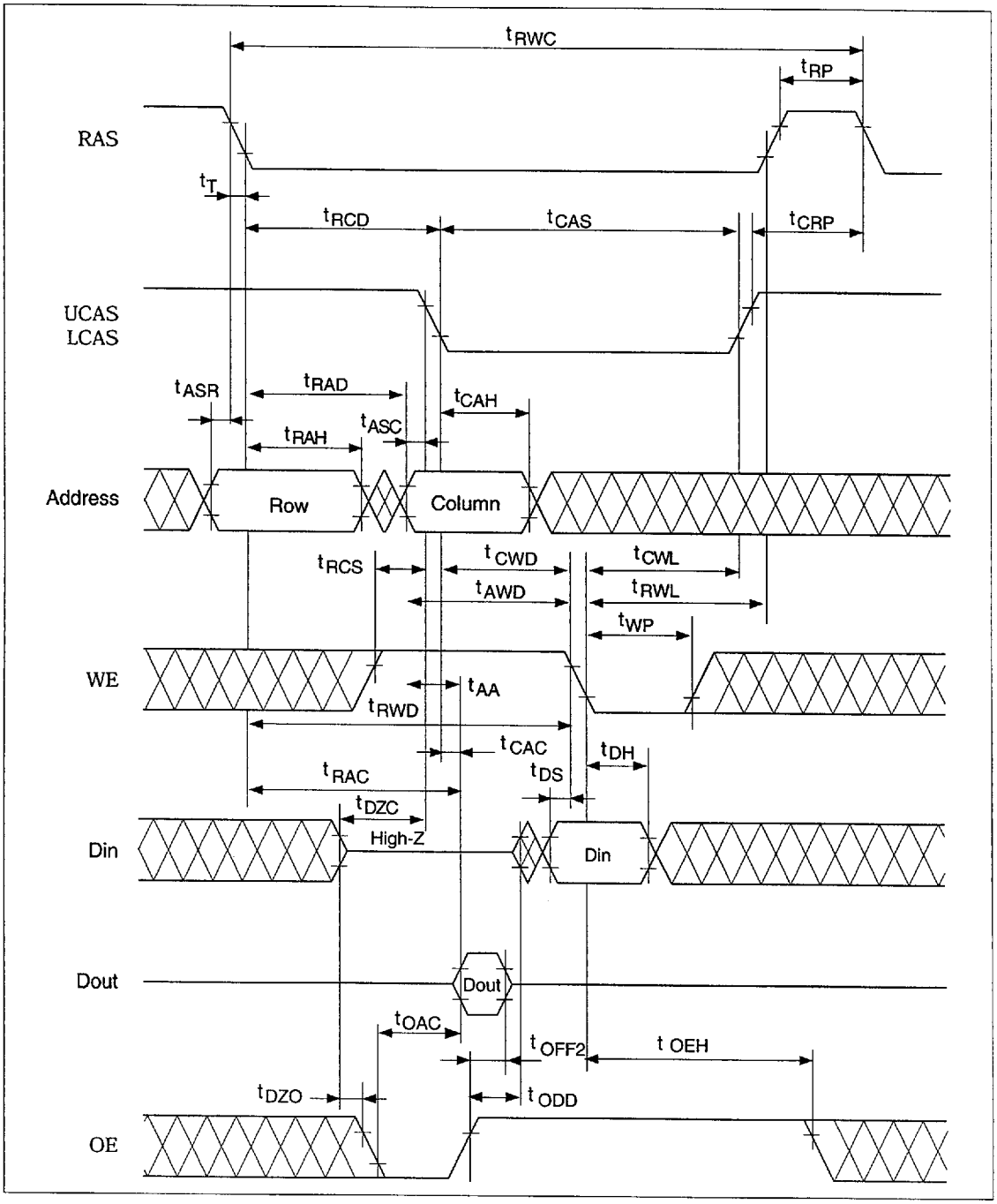


Delayed Write Cycle

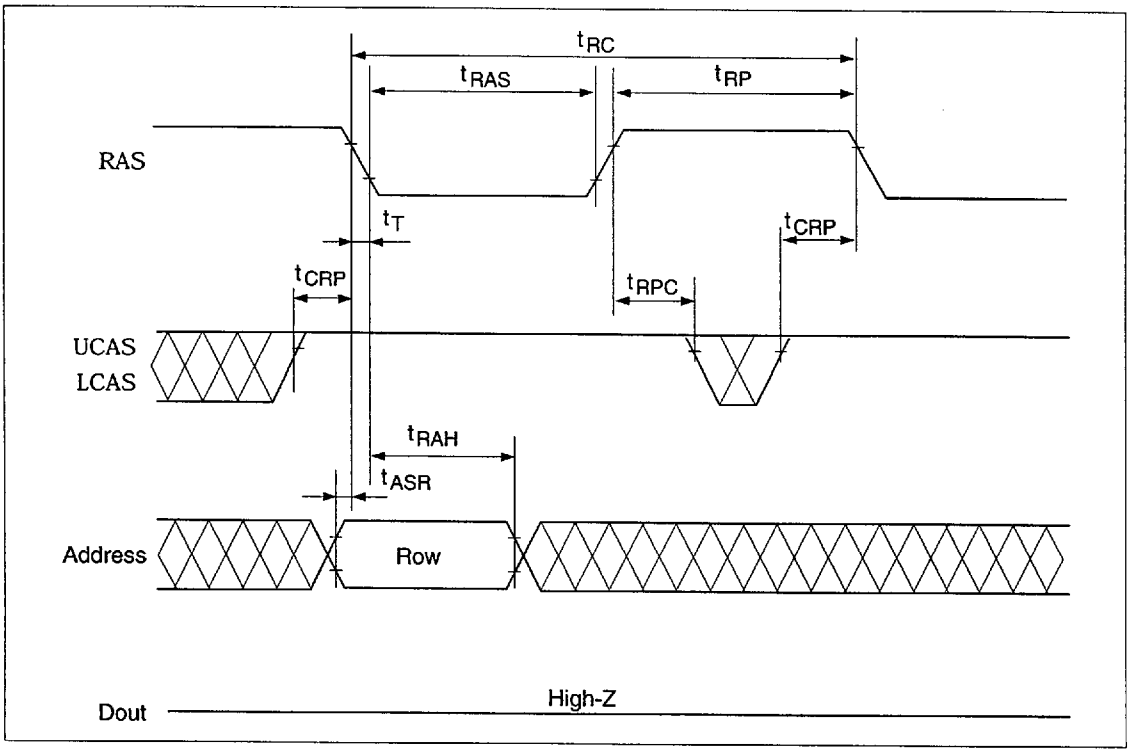


* Do not enable Dout during delayed write cycle.

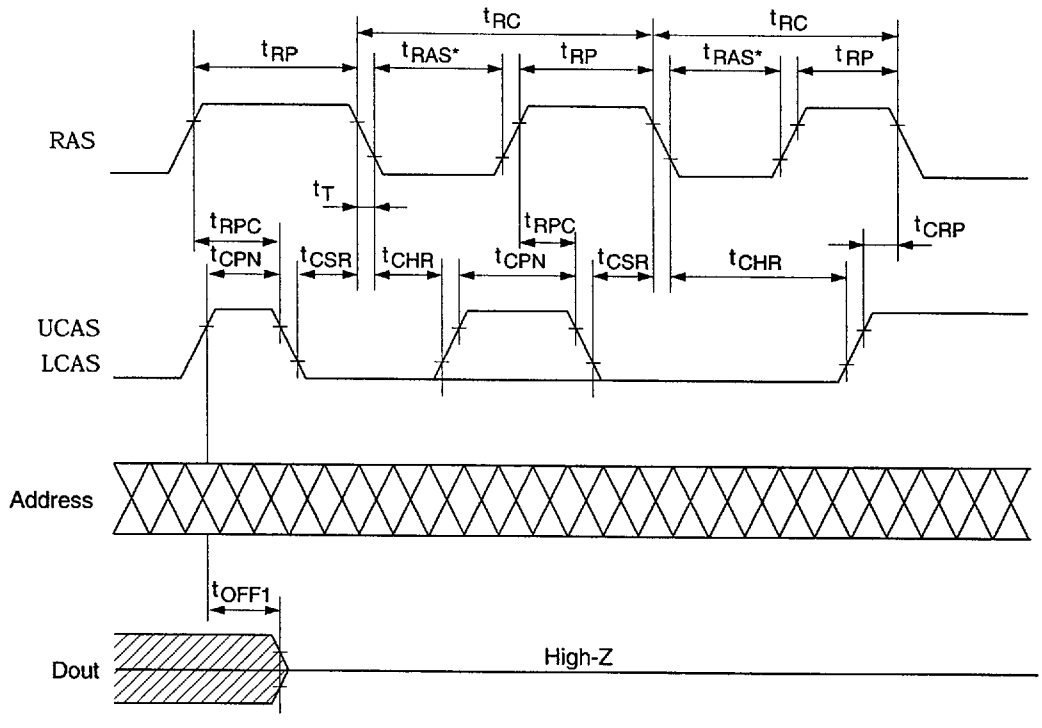
Read-Modify-Write Cycle



RAS-Only Refresh Cycle

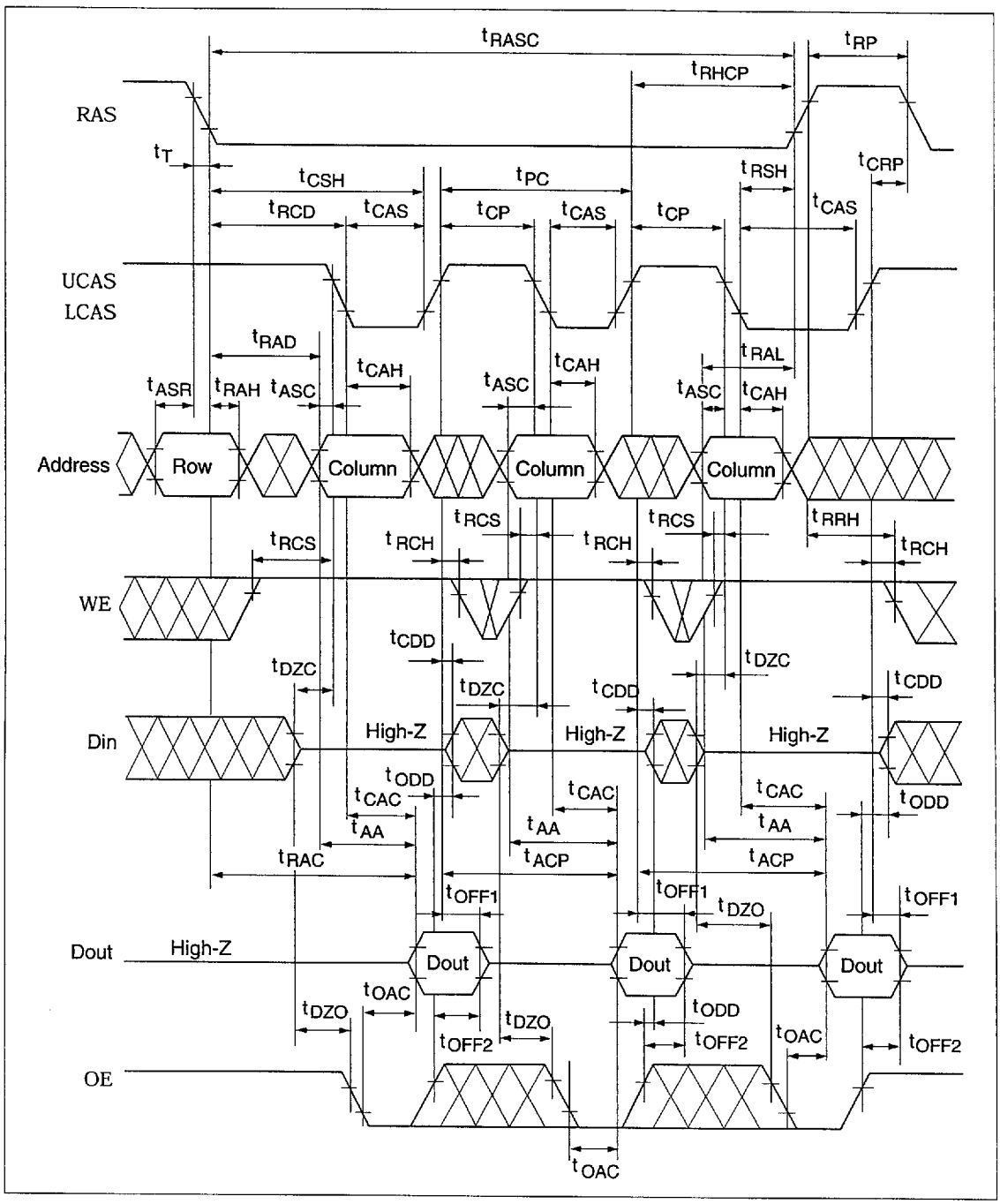


CAS-Before-RAS Refresh Cycle

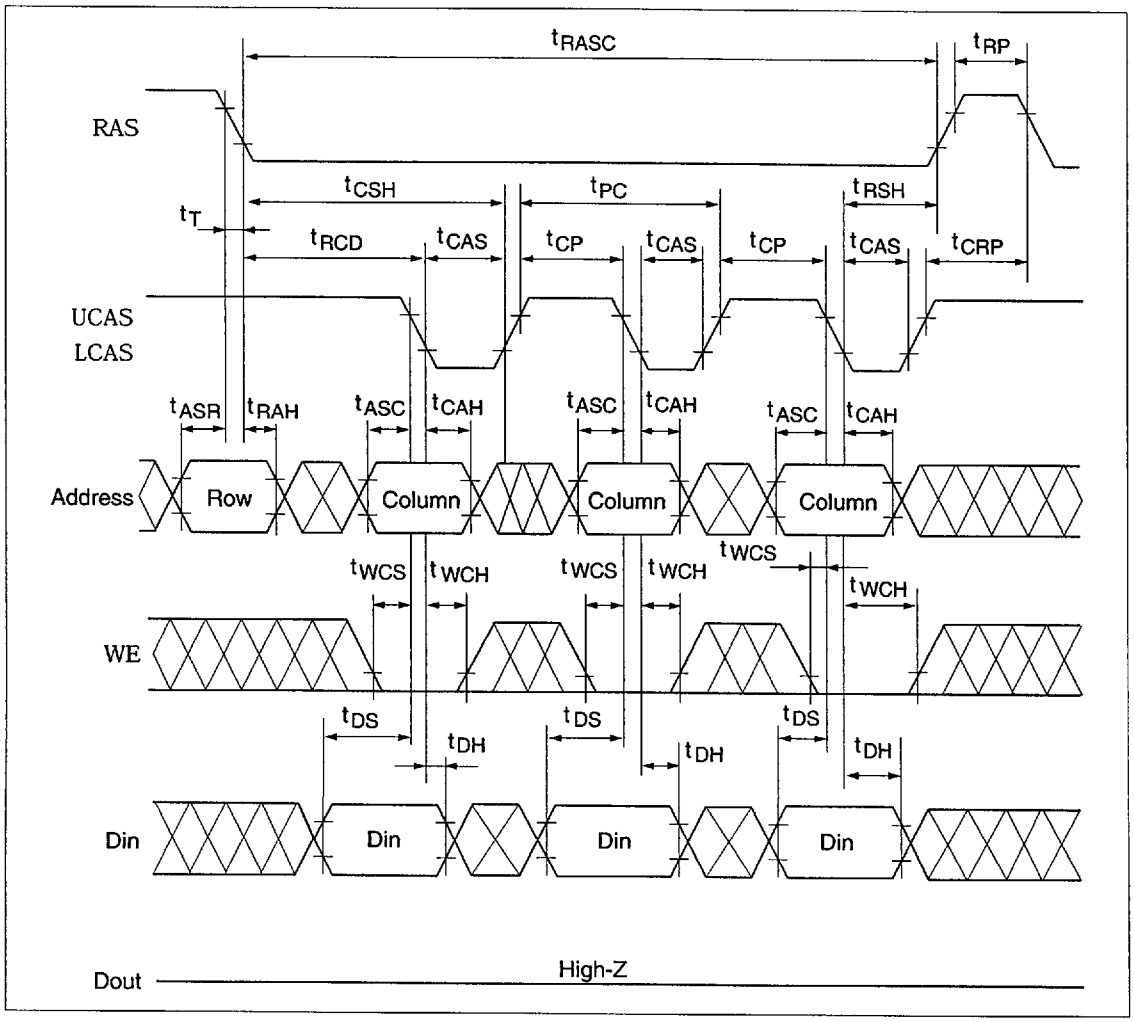


Note: Do not extend $t_{RAS} \geq t_{RAS}$ (max). Untested self refresh mode may be activated and data loss may result (HM514260D/DL).

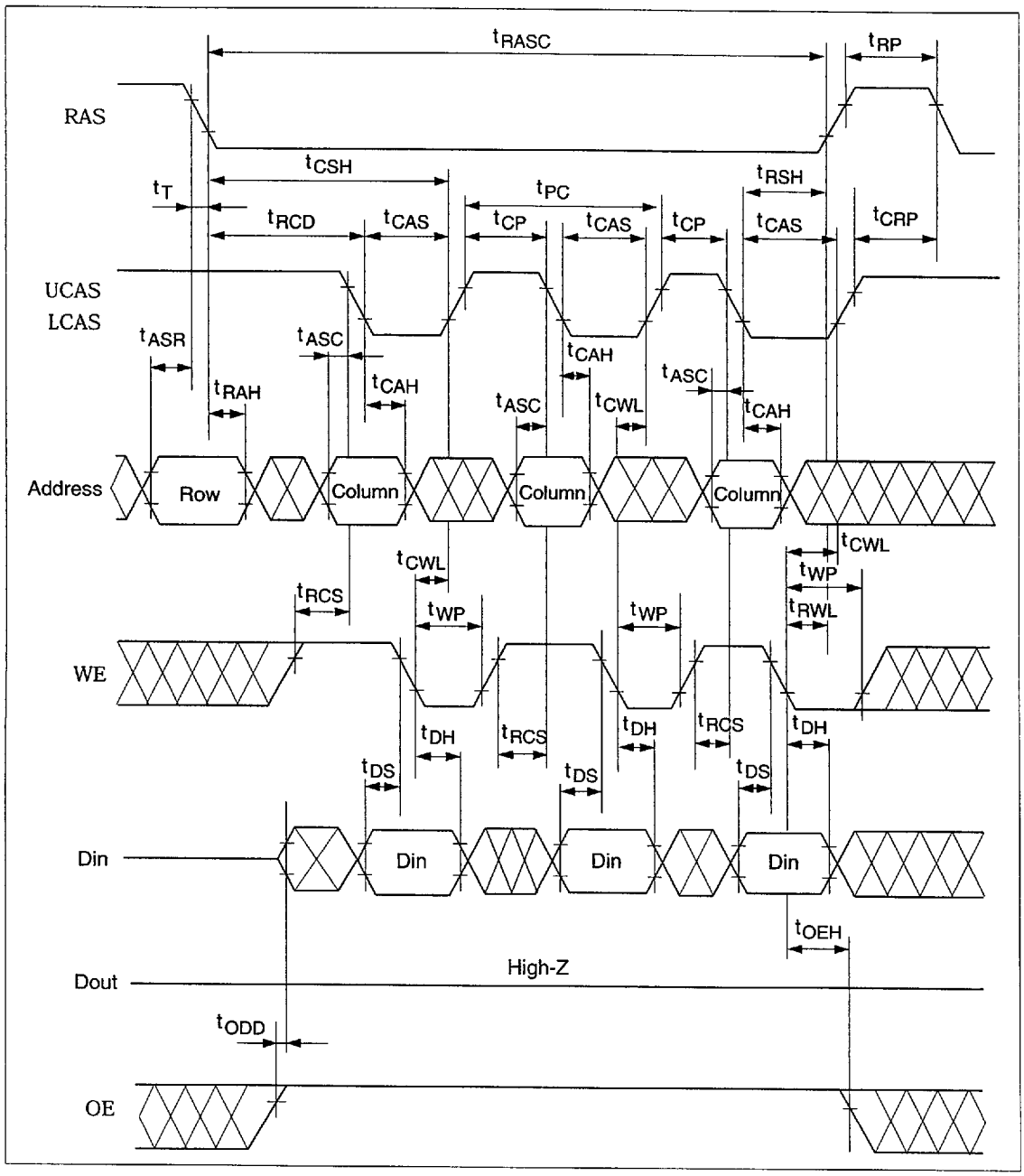
Fast Page Mode Read Cycle



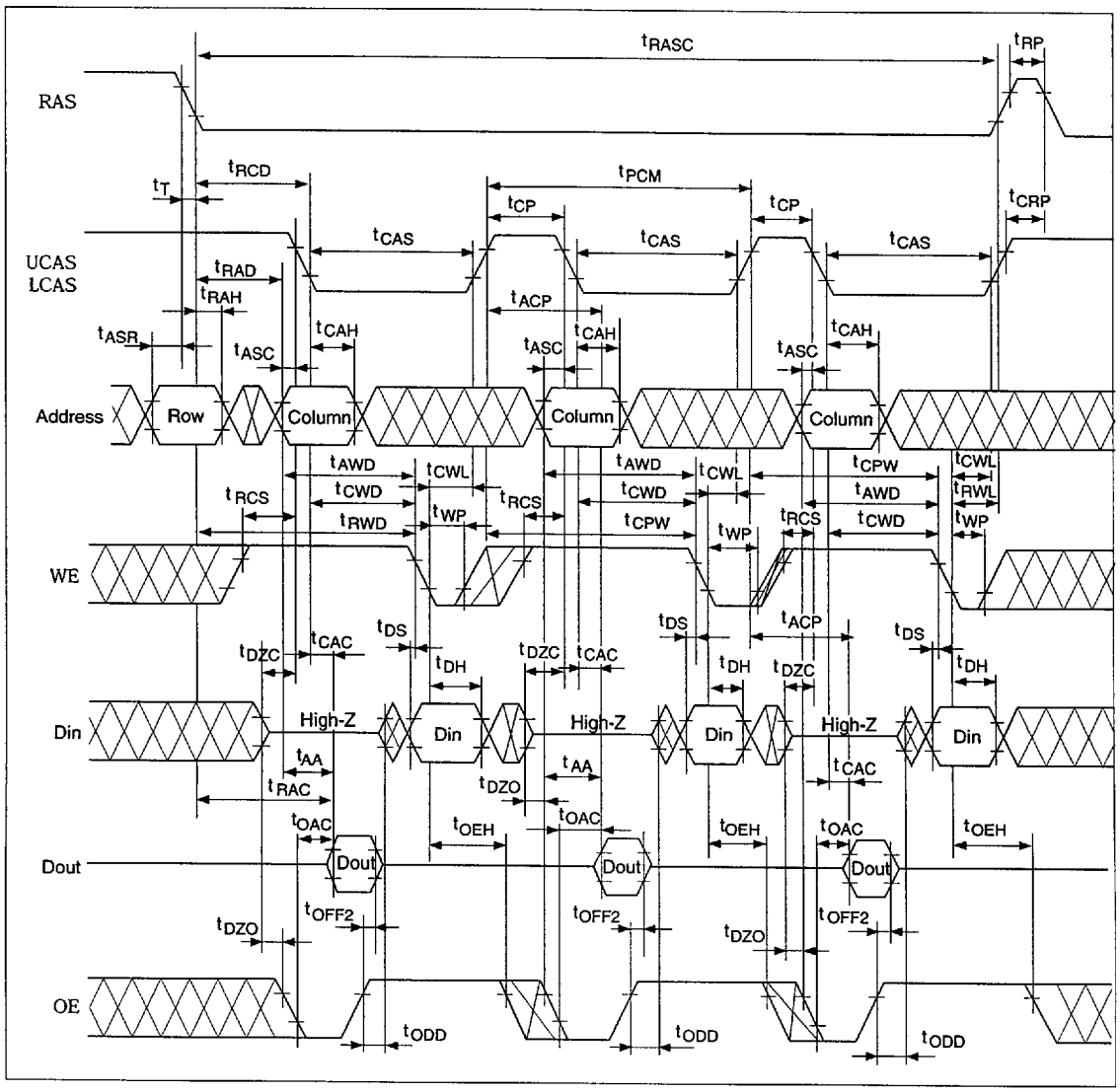
Fast Page Mode Early Write Cycle



Fast Page Mode Delayed Write Cycle



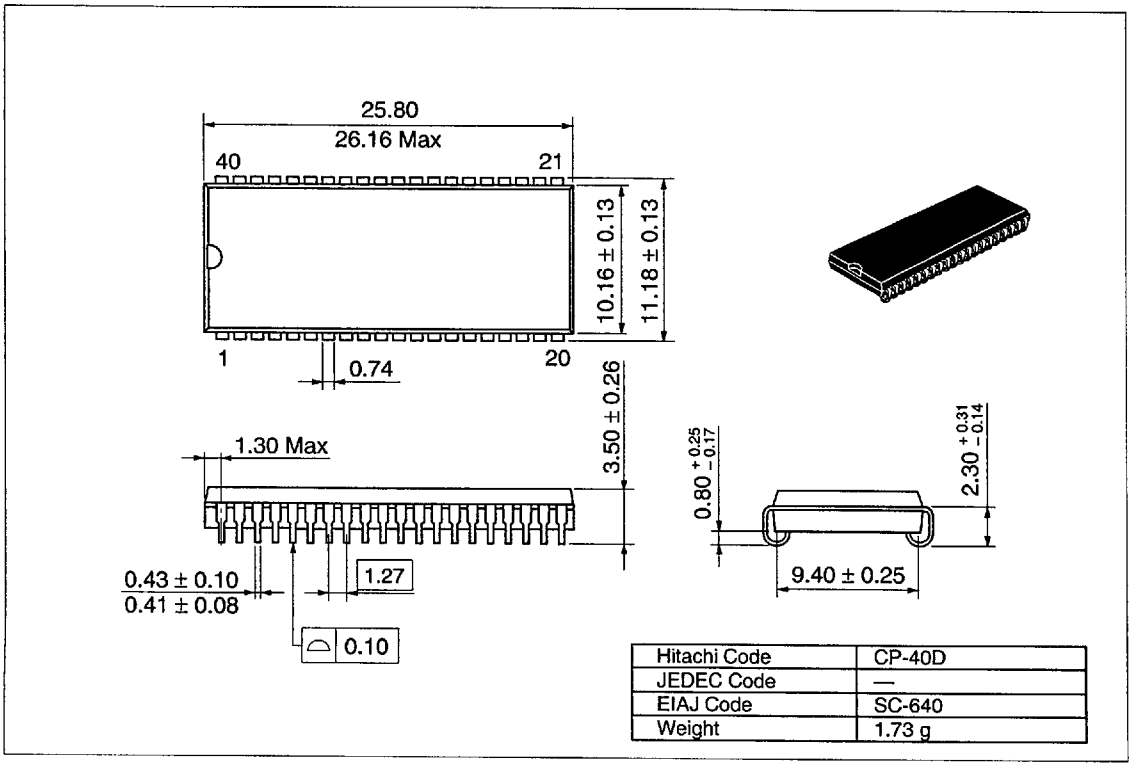
Fast Page Mode Read-Modify-Write Cycle



Package Dimensions

Unit: mm

HM514260DJI/DLJI Series (CP-40D)



Hitachi Code	CP-40D
JEDEC Code	—
EIAJ Code	SC-640
Weight	1.73 g