

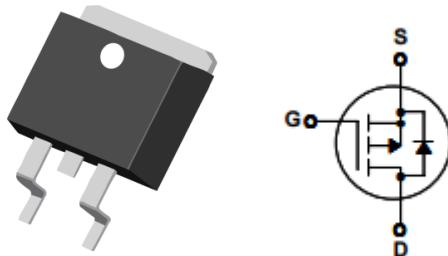
Description

This P-channel MOSFETs use advanced trench technology and design to provide excellent RDS(on) with low gate charge. It can be used in a wide variety of applications.

Features

BVDSS	RDS(on)	ID
-60V	0.07Ω	-27A

- 1) Low gate charge.
- 2) Green device available.
- 3) Advanced high cell density trench technology for ultra RDS(ON)
- 4) Excellent package for good heat dissipation.



TO-263

Absolute Maximum Ratings $T_c=25^\circ\text{C}$,unless otherwise noted

Symbol	Parameter	Ratings	Units
VDS	Drain-Source Voltage	-60	V
VGS	Gate-Source Voltage	± 20	V
ID	Continuous Drain Current-1	-27	A
	Continuous Drain Current-T=100°C	-19.1	
	Pulsed Drain Current2	-108	
EAS	Single Pulse Avalanche Energy3	560	mJ
PD	Power Dissipation4	120	W
TJ, TSTG	Operating and Storage Junction Temperature Range	-55 to +175	°C

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance ,Junction to Case1	1.25	°C/W
	Thermal Resistance, Junction to Ambient1	62.5	

Package Marking and Ordering Information

Part NO.	Marking	Package
KSMB27P06	KSMB27P06	TO-263

Electrical Characteristics $T_c=25^\circ\text{C}$ unless otherwise noted

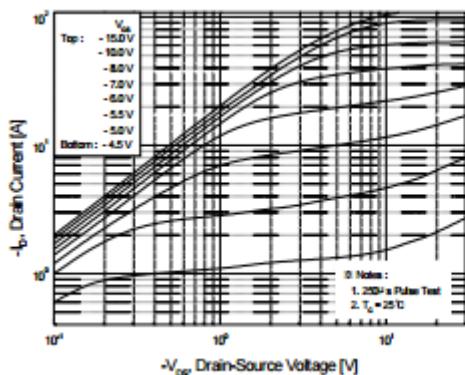
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$\text{V}_{\text{DS}}=0\text{V}, \text{I}_D=250\mu\text{A}$	-60	—	—	V
I_{DSS}	Zero Gate Voltage Drain Current	$\text{V}_{\text{DS}}=0\text{V}, \text{V}_{\text{GS}}=32\text{V}$	—	—	-1	μA
I_{GSS}	Gate-Source Leakage Current	$\text{V}_{\text{DS}}=\pm 20\text{V}, \text{V}_{\text{GS}}=0\text{A}$	—	—	± 100	nA
On Characteristics						
$\text{V}_{\text{GS}(\text{th})}$	GATE-Source Threshold Voltage	$\text{V}_{\text{DS}}=\text{V}_{\text{DS}}, \text{I}_D=250\mu\text{A}$	-2.0	—	-4.0	V
$\text{R}_{\text{DS}(\text{ON})}$	Drain-Source On Resistance ²	$\text{V}_{\text{DS}}=10\text{V}, \text{I}_D=6\text{A}$	—	0.055	0.07	Ω
		$\text{V}_{\text{DS}}=2.5\text{V}, \text{I}_D=5\text{A}$	—	—	—	---
G_{FS}	Forward Transconductance	$\text{V}_{\text{DS}}=5\text{V}, \text{I}_D=12\text{A}$	—	12.4	—	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$\text{V}_{\text{DS}}=15\text{V}, \text{V}_{\text{GS}}=0\text{V},$ $f=1\text{MHz}$	—	1100	1400	pF
C_{oss}	Output Capacitance		—	510	660	
C_{rss}	Reverse Transfer Capacitance		—	120	155	
Switching Characteristics						
$\text{t}_{\text{d}(\text{on})}$	Turn-On Delay Time	$\text{V}_{\text{DS}}=20\text{V},$ $\text{V}_{\text{GS}}=10\text{V}, \text{R}_{\text{GEN}}=3.3\Omega$	—	18	45	ns
t_r	Rise Time		—	185	380	ns
$\text{t}_{\text{d}(\text{off})}$	Turn-Off Delay Time		—	30	70	ns
t_f	Fall Time		—	90	190	ns
Q_g	Total Gate Charge	$\text{V}_{\text{GS}}=4.5\text{V}, \text{V}_{\text{DS}}=20\text{V},$ $\text{I}_D=6\text{A}$	—	33	43	nC
Q_{gs}	Gate-Source Charge		—	6.8	—	nC
Q_{gd}	Gate-Drain "Miller" Charge		—	18	—	nC
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage ²	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_S=1\text{A}$	—	—	-4.0	V
t_{rr}	Reverse Recovery Time	$\text{I}_r=7\text{A}, \text{di}/\text{dt}=100\text{A}/\mu\text{s}$	—	105	—	ns
Q_{rr}	Reverse Recovery Charge		—	0.41	—	nC

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board 2OZ copper.

2. The data tested by pulse width≤300us,duty cycle≤2%
3. The EAS data shows Max.rating.The test condition is $V_{DD}=25V$, $V_{GS}=10V$, $L=0.1mH$, $i_{AS}=17.8A$
4. The power dissipation is limited by 150°C junction temperature.

Typical Characteristics $T_J=25^{\circ}\text{C}$ unless otherwise noted



**Fig. 1 Typical Output Characteristics,
TC = 25 °**

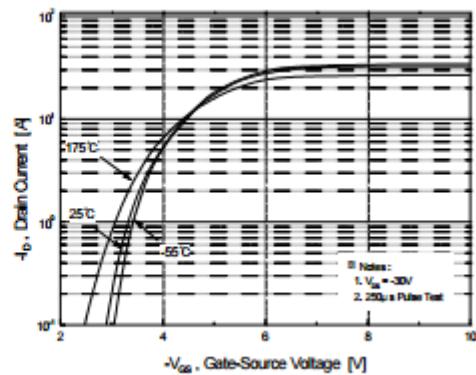
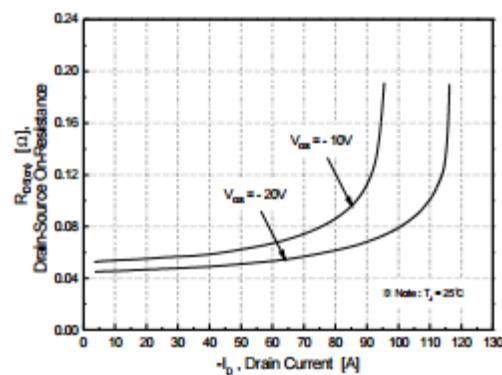
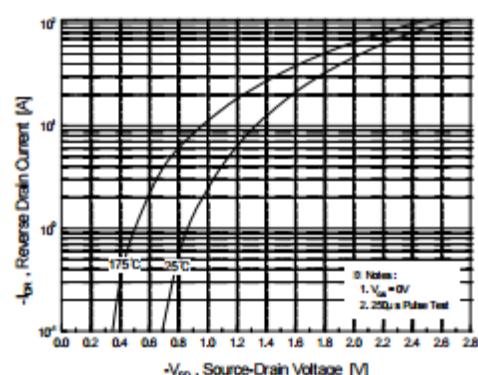


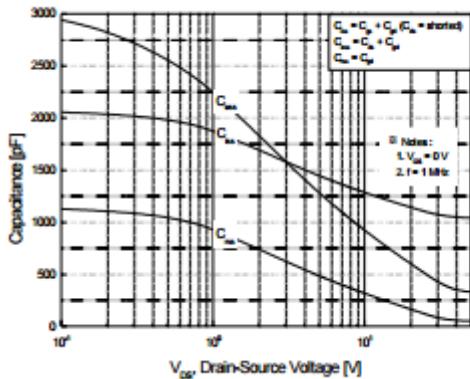
Fig. 2 Typical Transfer Characteristics



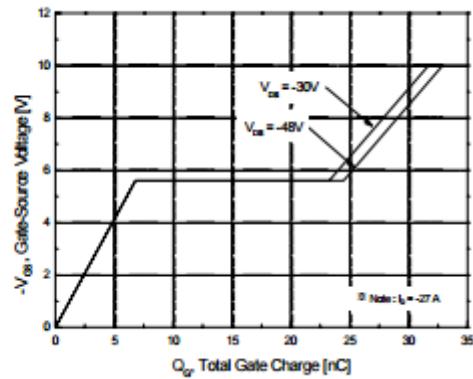
**Fig. 3 Typical Output Characteristics,
TC = 150 °C**



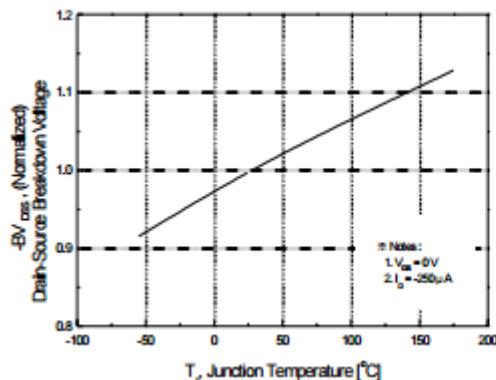
**Fig. 4 - Normalized On-Resistance vs.
Temperature**



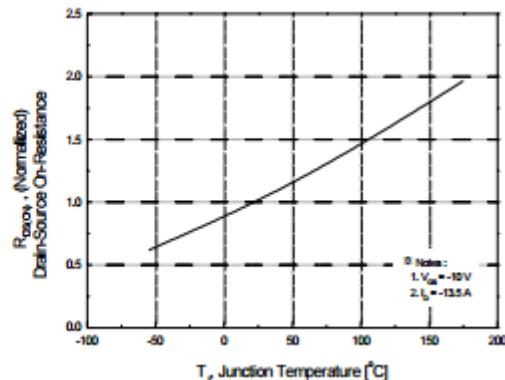
**Fig. 5 - Typical Capacitance vs.
Drain-to-Source Voltage**



**Fig. 6 - Typical Source-Drain
Diode Forward Voltage**



**Fig. 7 - Typical Gate Charge vs.
Gate-to-Source Voltage**



**Fig. 8 - Maximum Safe
Operating Area**

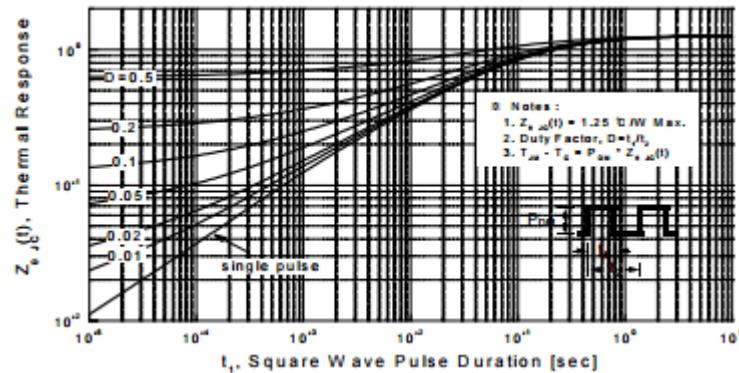


Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Case