M610x-SYNCE Series TCXO
IEEE 1588 & Synchronous Ethernet

Features:
- Available in Clipped Sine Wave or CMOS output
- Available in 10 pad or 4/5 pad options
- Low phase noise and excellent g-sensitivity performance 1.5 ppb/g

Applications:
- Synchronous Ethernet slave clocks ITU-T G.8262 EEC options 1 & 2
- Compliant to Stratum 3 GR-1244-CORE & GR-253-CORE
- SONET/SDH Network Timing
- Wireless Communications

Designed to Support 1588 & SyncE Device Suppliers Like:
- Microsemi
- IDT
- Semtech

Ordering Information

M610x-SYNCE	2	2	T	S	N	00.0000 MHz

Product Series
M6100 = 5.0 V
M6101 = 3.3 V
M6102 = 3.0 V

Temperature Range
2: -40 °C to +85 °C **6:** -20 °C to +70 °C

Holdover Stability
1: EEC Option 1 (±2.0 ppm)
2: EEC Option 2 (±0.34 ppm)

Output Type
T: Voltage Controlled With Tristate
F: No Voltage Control With Tristate

Output Waveform
C: HCMOS
S: Clipped Sine Wave

Package/Lead Configurations
N: 10 pad Leadless Ceramic
T: 4/5 pad Leadless Ceramic

Frequency (customer specified)

Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency Range	F	10.000		38.880	MHz	
Initial Accuracy	F_I	-1.0		+1.0	ppm	@ 25˚C @ time of shipment
Frequency Stabilities						
Operating Temperature	T_A	See Ordering Information				
vs Temperature	$\Delta F_T/F$			0.3	ppm	T_A = -40 °C to +85 °C Ref GR1244CORE
vs Drift				40	ppb	After 24 hours at constant temperature
Free-Run Accuracy		-4.6		+4.6	ppm	Includes initial calibration @ +25 °C, deviation over temperature, supply voltage and load variations, reflow soldering, and 20 year aging.
vs. Supply Voltage	$\Delta F_{VDD}/F$		±0.02	±0.1	ppm	±5% change in voltage
vs. Load	$\Delta F_{LOAD}/F$		±0.02	±0.1	ppm	±5% change in load
RF Output						
Output Type	See Ordering Information					
Output Load			15 10/10		pF kΩ / pF	HCMOS Output Clipped Sine Wave Output
Symmetry (duty cycle)	T_{DC}	40	50	60	%	Ref to ½ V_S, HCMOS
Rise/Fall Time	T_R/T_F			8	ns	Ref. 10% to 90% V_{OUT}, HCMOS
Output Logic Level (HCMOS)	V_{OH}	80			% V_{DD}	I_{OH}/ I_{OL} = ±4 mA, V_S = +3.0 V
	V_{OH}			20	% V_{DD}	I_{OH}/ I_{OL} = ±4 mA, V_S = +3.0 V
Output Level (Clipped Sinewave)		1.0			V_{pk-pk}	
Frequency Adjustment		±9.2			ppm	Over Control Voltage Range
Control Voltage Range		0.3 0.3 0.5		2.7 3.0 4.5	V	For V_S = 3.0 V For V_S = 3.3 V For V_S = 5.0 V
Input Resistance		100			kΩ	
Linearity				3	%	
Other Parameters						
SSB Phase Noise (under static conditions, 10MHz)			-100		dBc/Hz	@ 10 Hz Offset
			-128			@ 100 Hz Offset
			-148			@ 1 kHz Offset
			-155			@ 10 kHz Offset
			-156			@ 100 kHz Offset
Wander Generation	MTIE & TDEV per ITU-T G.8262 EEC option 2, GR-1244 & ITU-T G.812 (See Figure A)					@ 0.1 Hz bandwidth
Supply Voltage & Current						
Supply Voltage	V_{DD}	See Ordering Information			V_{DC}	
Supply Current	I_D		2.2	3.3	mA	HCMOS @ 13 MHz
			1.5	2.2	mA	Clipped Sine Wave @ 13 MHz

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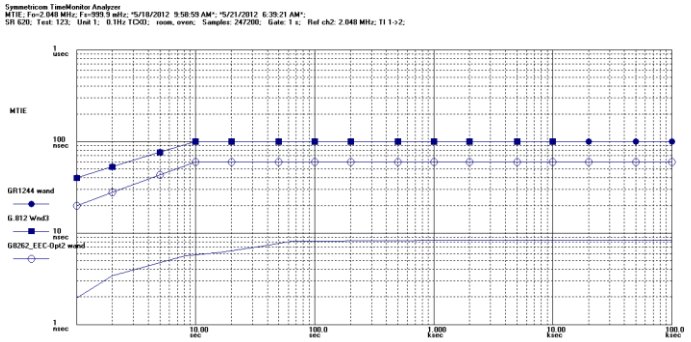
Wander Generation Plots: Loop BW 0.1Hz

MTIE Performance



TDEV Performance

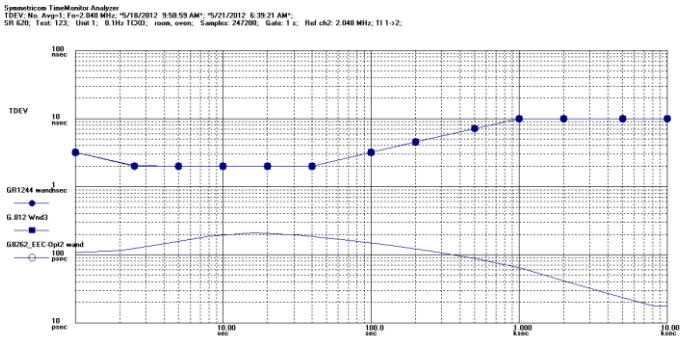
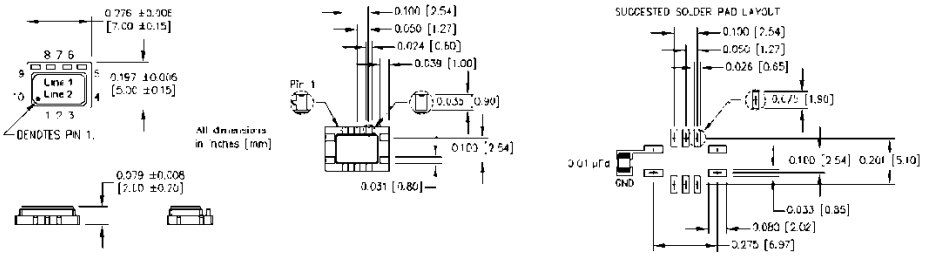
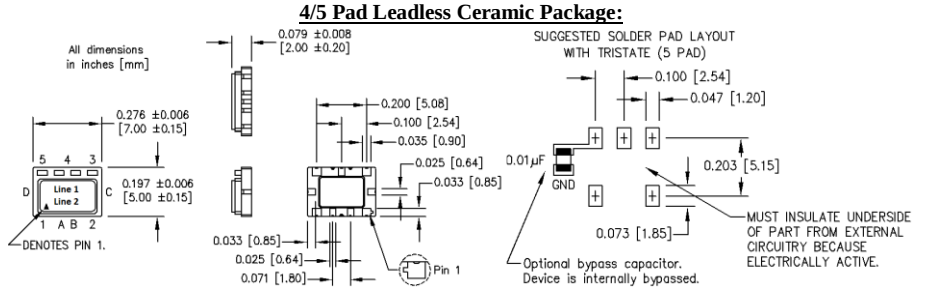


Figure A

10 Pad Leadless Ceramic Package:



4/5 Pad Leadless Ceramic Package:



Marking and Pin Assignments

Marking:

Line 1: M610xyw
Line 2: Frequency

Pin Assignments:

M610x 10 Pad	M610x 4/5 Pad
Pin/Pad 1: Vref or N/C	Pin/Pad 1: Vcontrol
Pin/Pad 2: N/C	Pin/Pad A: N/C
Pin/Pad 3: N/C	Pin/Pad B: N/C
Pin/Pad 4: Ground	Pin/Pad 2: Ground
Pin/Pad 5: Output	Pin/Pad C: N/C
Pin/Pad 6: N/C	Pin/Pad 3: Output
Pin/Pad 7: N/C	Pin/Pad 4: Tristate or N/C
Pin/Pad 8: Tristate	Pin/Pad 5: Supply
Pin/Pad 9: Supply	Pin/Pad D: N/C
Pin/Pad 10: Vcontrol	

Recommended Reflow Profile: