

AN-7730

FL7730 Design Tool Flow

Overview

This document is intended to provide in-depth guidance to using the Fairchild Design Tool for FL7730. Use the Design Tool with the product datasheet.

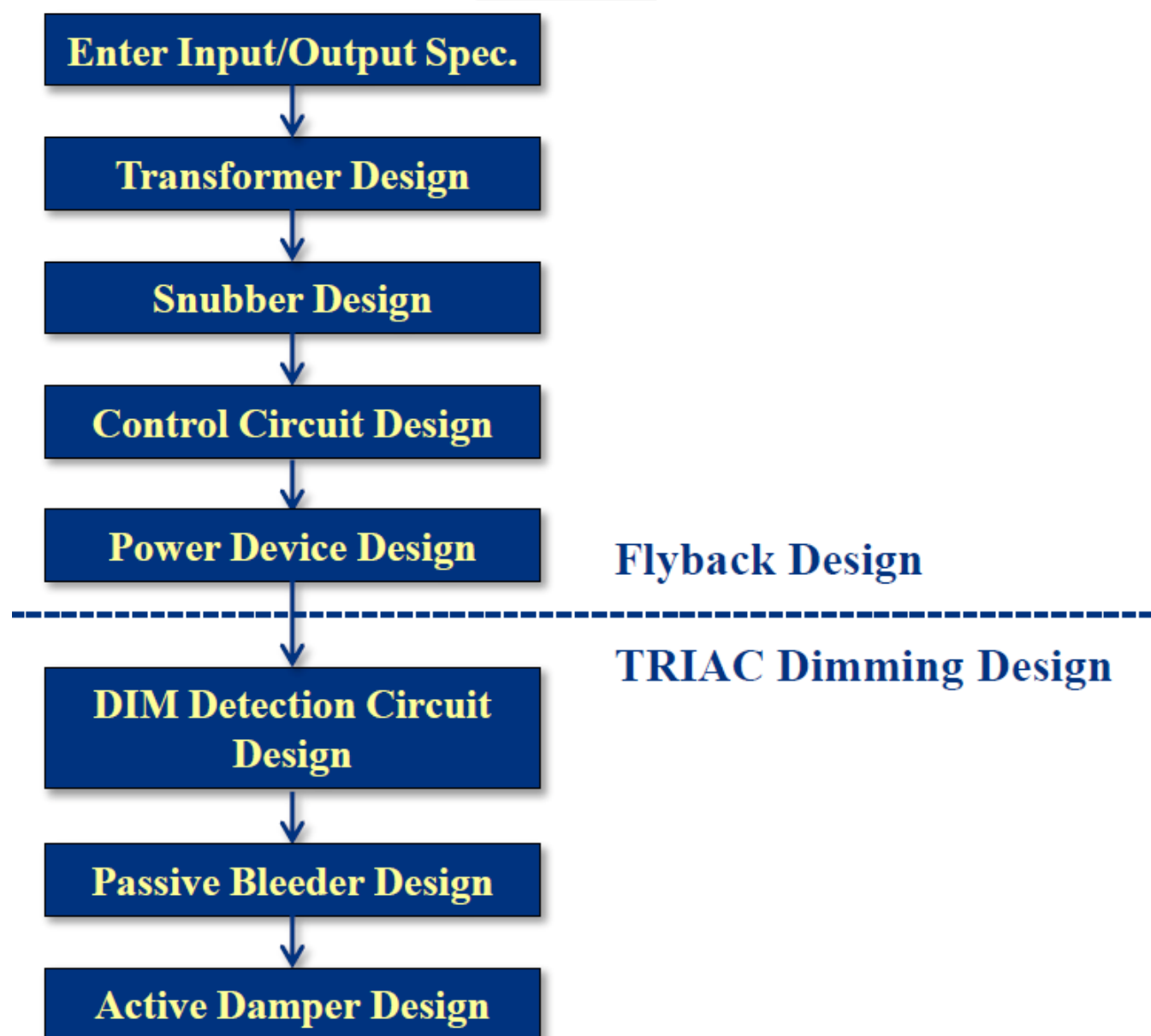


Figure 1. Design Flow

Step 1 — Enter Input Output Specification

Input
Output

Blue box is input from user.
Red box is calculated output.

Input Spec			
Min. Vin	90	Vac	
Max. Vin	140	Vac	
Output Spec			
Vout	22	V	
Max. Vout	28	V	
Iout	380	mA	
Pout	8.36	W	

Max. Vout is OVP level.

Step 2 — Transformer Design

Transformer Design		
Max. Duty	39	%
Max. Ton	6.500	us
Switching freq.	60	kHz
Max. Vcs	0.5	V
Efficiency	80	%
Ae	36.6	mm ²
Bmax	0.3	
Lm	0.982	mH
Nps	3.223	
Nas	0.821	
Nap	0.255	
Np.min	75.347	T
Np	76	T
Ns	23.578	T
Na	19.368	T
Llk	10	uH

Max. duty is generally between 20 ~ 50%.

High max. duty = · Low conduction loss. Suitable for low-line

Low max. duty = · More Bmax margin. Suitable for high-line

Max. Ton should be less than 10us.

This switching frequency is the operating frequency at the rated Vout condition.

The switching frequency should be less than 65kHz.

Max. Vcs is max. peak CS voltage.

Enter Max. Vcs less than 0.67V because pulse by pulse CS voltage limit is 0.67V.

Higher Nps makes higher max. Vcs in the primary side CC regulation.

So, when max. Vcs is highly set, Nps becomes higher.

Enter Np over Np.min.

If Np is too big to fit in transformer window, reduce Max. Duty.

Make transformer according to the above spec.

Then, enter Llk (Leakage inductance) after measuring.

Step 3 — Snubber Design

Snubber Design		
Vsn	200	V
ΔVsn	5	V
Rsn	242.7247	kohm
Csn	2.746596	nF

Vsn is snubber voltage.

Vsn is generally set as 2~2.5 times Nps · Vo.

ΔVsn is generally set as 5% ripple of Vsn.

Step 4 — Control Circuit Design

Control Circuit Design		
R _{sense}	0.593767	ohm
R _{cc}	100	ohm
V _{in.bnk}	50	V
V _f	0.5	V
R _{vs1}	165.2367	kohm
R _{vs2}	19.75502	kohm
C _{vs}	10	pF
C _{comi}	1	uF
C _{vdd}	33	uF
D _{vdd Vmax}	73.95584	V
R _{str}	155.8442	kohm

R_{cc} is line CC compensation resistor.
When I_{out} becomes higher at higher input voltage, increase R_{cc}.
R_{cc} should be limited less than 500ohm.
Large R_{cc} can make CS noise, inducing V_{cs} peak detection error.

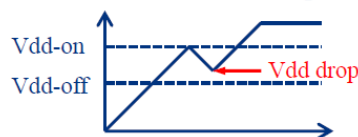
V_{in.bnk} is COMI/VS blanking level.
COMI blanking : Error amp. input is fixed, working as open loop.
VS blanking : VS voltage detection is disabled.
V_{in.bnk} is generally set as 30~70V.

V_f is secondary diode forward voltage.

C_{vs} is VS filter capacitor, generally set as 10~30pF.

C_{comi} is generally 0.68~3.3uF.
Check output voltage overshoot at startup in max. V_{in} condition.
If output voltage overshoot is too big, increase C_{comi}.

V_{dd} capacitor is generally in 10~47uF.
If V_{dd} drops too close to V_{dd-off} at startup, increase C_{vdd}.



Step 5 — Power Device Design

Power Device Design		
MOSFET V _{max}	397.9899	V
MOSFET I _{pk}	0.842082	A
Diode V _{max}	89.4245	V
Diode I _{pk}	2.714286	A

V_{max} is MOSFET drain-source maximum voltage.
I_{pk} is MOSFET peak current.

V_{max} is maximum reverse voltage of secondary diode.
I_{pk} is peak current of secondary diode.

Step 6 — DIM Detection Circuit Design

DIM Detection Circuit Design		
ZDdim	11	V
Rdim1	1	Mohm
Rdim2	75	kohm
Rdim3	62	kohm
Cdim	3.3	uF

Zener voltage of ZDdim is generally in 10~40V.

Rdim1 is generally around 1Mohm.

If Rdim1 is too small,

- efficiency is reduced.
- Dim pin voltage is changed a lot when line voltage changes.

If Rdim1 is too big,

- ZDdim biasing current becomes too small, inducing error in dimming angle detection.

TRIAC dimmers have different max. dimming angle.

So, Rdim2/3 can not be calculated and found by testing with dimmers.

Rdim2/3 are tens to hundreds kohm.

Rdim2/3 determine dimming control range.

For wider dimming control range, reduce Rdim2 and Rdim3.

(But, wider dimming control makes higher flicker possibility specially in high-line and low output power condition.).

Cdim is 0.1~5uF as a filter to supply DC voltage to Dim pin.

If Cdim is too big, Dim pin voltage rises slowly at startup and it can affect powering speed.

Step 7 — Passive Bleeder Design

Passive Bleeder Design		
Cbleeder	330	nF
Rbleeder	0.5	kohm

Cbleeder is generally 47~470nF.

If Cbleeder is increased,

- Flicker is relieved.
- Efficiency and PF become worse.

Rbleeder is determined after selecting Cbleeder.

Rbleeder is generally 0.1~10kohm.

Too big Rbleeder limits bleeder current, which makes flicker.

Too small Rbleeder induces input current ringing at dimmer firing, which also can make flicker.

So, change Rbleeder by checking input current at firing.

Find the min. Rbleeder to satisfy below.

- input current at firing is higher enough than dimmer holding current.
- there is no mis-fire right after firing.

The min. Rbleeder is proper value for no flicker and high efficiency.

Step 8 — Active Damper Design

Active Damper Design		
Rdamp	100	ohm
SWdamp Vmax	300	V
Ddelay Vmax	300	V
Cdelay	100	nF
Rdelay	20	kohm

Rdamp is generally 10~1kohm.

Rdamp is to limit input spike current at fire and remove flicker.

Large Rdamp can considerably reduce spike current and remove flicker, but it will reduce efficiency.

So, find min. Rdamp to satisfy below without active damping circuit.

- Input spike current at 90° dimming angle is less than customer spec.
- There is no flicker caused by Rdamp current ringing.
(Check input current and Rdamp current at the same time. Then, you can find if input current ringing is affected by Rdamp current.)

Check the Rdamp temperature after finding the min. Rdamp.

If the temperature is too high and efficiency is too low, active damper is necessary and go to **active damper design**.

Active Damper Design		
Rdamp	100	ohm
SWdamp Vmax	300	V
Ddelay Vmax	300	V
Cdelay	100	nF
Rdelay	20	kohm

Check Rdamp voltage at 90° dimming angle firing.
That is SWdamp max voltage .

Tip! SWdamp with low threshold voltage can reduce power loss.
(Because Rdamp voltage is regulated as threshold voltage.)

Ddelay max. voltage is same as SWdamp max. voltage.

Cdelay is generally around 100nF.

Rdelay is tens to hundreds kohm.

Large Rdelay lengthens delay time between dimmer fire and SWdamp turn-on.

Find the min. Rdelay to satisfy below.

- At 90° dimming angle, SWdamp should be turned on after input current is dampened by Rdamp.
(Check if input current ringing is finished before SWdamp turns on.)
- The min. Rdelay is proper value for high efficiency.

Related Resources

Locate the Design Tool at:

http://www.fairchildsemi.com/design_tools/led-driver-design-tool/

Consult the product datasheet at:

[*FL7730 — Dimmable Single-Stage PFC PSR Offline LED Driver*](#)

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