AKD4317

Evaluation board for AK4317 Rev.A

General description

The AKD4317 is an evaluation board for the AK4317 of a 1bit stereo D/A converter with individually controllable channel volume for multimedia audio system which includes 18bit digital filter and also analog LPF. The AKD4317 has interface with a digital signal generator using ROM-Board, AKM's A/D converter and serial control circuit, therefore enables easier evaluation of the AK4317.

■ **Ordering guide**

AKD4317   --- Evaluation board for AK4317

Function

☐ On-board serial control circuit

☐ On-board clock generator

☐ Compatible with 3 types of interface

  1) Direct interface with AKD5391, AKD5390/89, AKD5352/1, AKD5350 and AKD5340.
  2) Interface with a signal generator(AKD43XX).
  3) On-board CS8412 as DIR which accepts optical input.
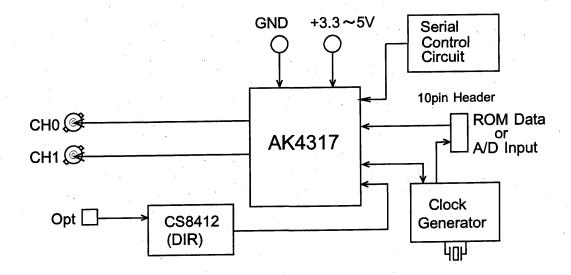
☐ A BNC connector for an external clock input.

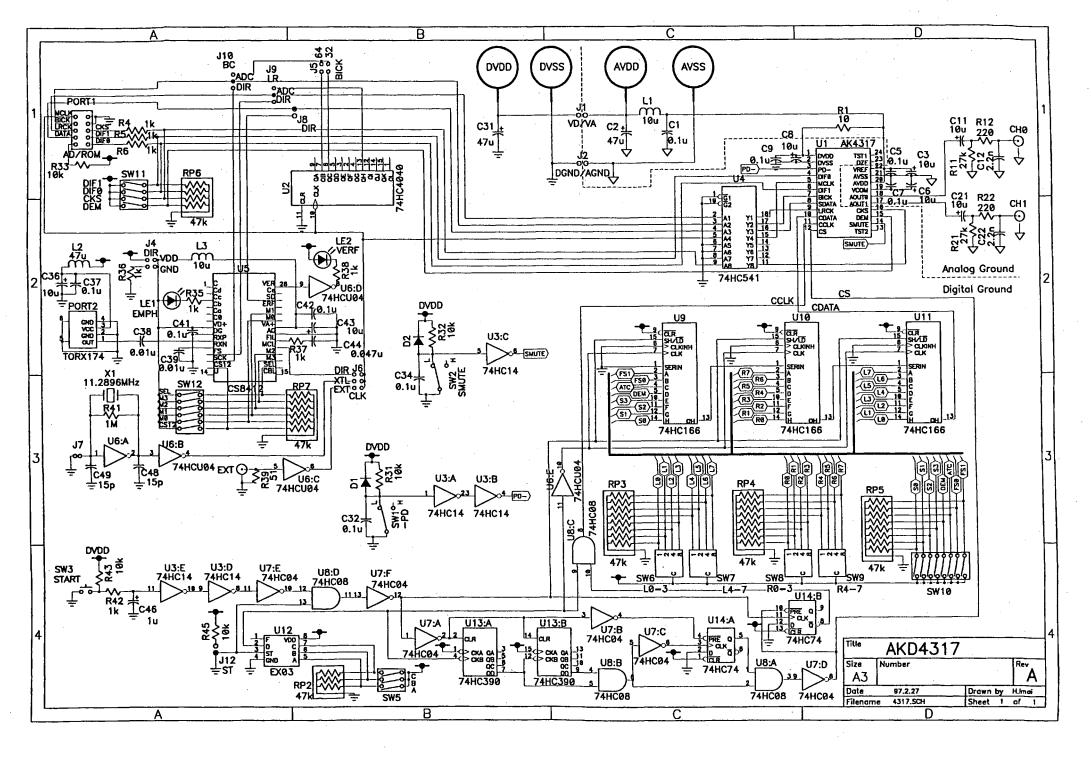

Figure 1. AKD4317 block diagram

AKD4317

Size	Number		Rev
A3			A
Date	97.2.27	Drawn by	H.Imai
Filename	4317.SCH	Sheet	1 of 1

■   External Analog circuit

The AK4317 includes a combination of switched-capacitor filter(SCF) and continuous-time filter(CTF), so any external filters are not required. The analog output of a AK4317 outputs directly from a BNC connector, when VREF is 5V that the output level is about 1Vrms.

■   Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD pin and DVDD pin, respectively. AVDD pin is supplied from analog supply in system and DVDD pin is supplied from AVDD pin via 10 ohms resistor. Decoupling capacitors should be as near to the AK4317 device as possible, with the low value ceramic capacitor being the nearest.

■   Voltage reference

The differential Voltage between VREF pin and AVSS pin set the analog output range. VREF pin is normally connected to AVDD pin with a 0.1uF ceramic capacitor. VCOM pin is a signal ground of this chip. An electrolytic capacitor less than 10uF in parallel with a 0.1uF ceramic capacitor is attached between VCOM pin and AVSS pin eliminates the effects of high frequency noise. No load current maybe drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pin in order to avoid unwanted coupling into the AK4317.

■   Operation sequence

  1. Set up the power supply lines
       AVDD=DVDD=3.3V~5V, AVSS=DVSS=0V
       Each supply line should be distributed from the power unit.
       AVDD should be powered at the same time or earlier than DVDD.
  2. Set up the evaluation modes and jumper pins （See next item）
       Be careful for the operating voltage when use DIR or ROM board.
  3. Set up the DIP SW. （See next item）
  4. Power on.(The AK4317 should be reset once by bringing PD "L" upon power-up.)
  5. SW1 resets the AK4317 during operation
       The AK4317 is reset at lower position and exits resetting at upper position.

■   Set up the evaluation modes and jumper pins

  1. Evaluation Mode
    Applicable Evaluation Mode
       1-① DIR(Optical link) · (Default)
       1-② Ideal sine wave generated by ROM data
       1-③ Using AD converted data
       1-④ All interface signals including master clock are fed externally.

1-① DIR(CS8412)・・・・・・・・・Default

PORT2 is used. DIR generates CLK, BICK and LRCK from the received data through optical connector(TORX174). Used for the evaluation using CD test disk. Nothing should be connected to PORT1. (For J13, see "6. CS8412 set-up" .)
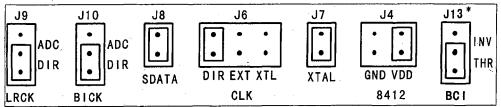
Figure 2. Jumper Set-up（DIR）

1-② Ideal sine wave generated by ROM data

Digital signals generated by AKD43XX are used. PORT1 is used for the interface with AKD43XX. Master clock is sent from AKD4317 to AKD43XX, and then LRCK, BICK, SDATA are supplied from AKD43XX to AKD4317. In case of using external clock through a BNC connector, select "EXT" on J6(CLK) and short J7.
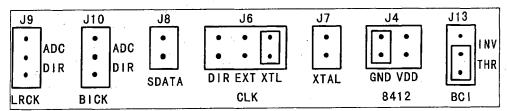
Figure 3. Jumper Set-up(ROM)

1-③ Using AD converted data

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's A/D evaluation boards (AKD5391, AKD5390/89, AKD5352/1, AKD5350 and AKD5340) with PORT1. In case of using external clock through a BNC connector, select "EXT" on J6(CLK) and short J7.
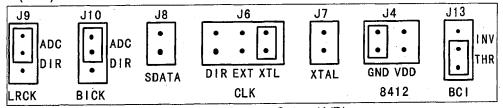
Figure 4. Jumper Set-up(A/D)

1-④ All interface signals including master clock are fed externally.

Under the following set-up, all external signals could be fed through PORT1.
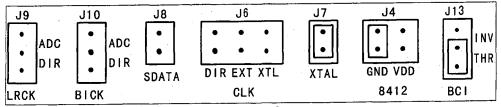On board interfacing devices operate normally at the operating voltage of ≥ 2.7V.

Figure 5. Jumper Set-up

2. BIT CLK(BICK) set-up   [J5]

J5

Either 32fs or 64fs could be selected. Figure 6 shows 64fs example.

64 32

BICK

Figure 6.

3. CKS set-up   [SW11-3]

Either 256fs or 384fs could be selected.
On: 384fs
Off: 256fs
note: The evaluation mode of ① and ③ enables only 256fs of BICK.

4. De-emphasis(DEM pin) set-up   [J3]

Set up the de-emphasis filter(tc=50/15 μ s) corresponding to only fs=44.1kHz by IIR filter.
On: De-emphasis On
Off: De-emphasis Off
note: DEM bit in the serial control can be also controlled. In this case, because of DEM bit and
DEM pin are ORed internally, DEM bit in the serial control should be "0".

5. Audio serial interface format (AK4317)   [SW11-1,2]

Data format of AK4317 is determined by DIF0 and DIF1.

Table 1. Data format of AK4317

DIF1	DIF0	Mode	BICK
OFF	OFF	0: 16bit LSB justified	$\geq$ 32fs
OFF	ON	1: 18bit LSB justified	$\geq$ 36fs
ON	OFF	2: 18bit MSB justified	$\geq$ 36fs
ON	ON	3: I²S Compatible	$\geq$ 36fs or 32fs

6. CS8412(DIR) set-up   [SW12]

Adjust the data format of CS8412(DIR) to AK4317 with SW12.
※ Don't forget that JP13(BCI) should be set up.

Table 2.   DIP SW Set-up of the CS8412 (refer to the CS8412 data sheet.)

Table 2-a

No.	pin name	ON	OFF	
1	SEL	ON *1		
2	M3			
3	M2	see Table 2-b		
4	M1			
5	M0			
6	CS12	Rch	Lch	*2

*1 When "ON", it shows pre-emphasis on EMPH(LED turns on).
*2 Selects the channel whose status is represented.

Table 2-b

M3	M2	M1	M0	Mode	J13
0	0	0	0	0: 16-20bit MSB justified	INV
0	0	1	0	2: I2S Compatible	THR
0	1	0	1	5: 16bit LSB justified	THR
0	1	1	0	6: 18bit LSB justified	THR

1:ON, 0:OFF

■ Soft mute operation [SW2]

The soft mute operation can be controlled by the SW2. When SMUTE pin goes "H"(The SW2 is lower position) , the output signal is gradually attenuated to $-\infty$dB in 1024 LRCK cycles. And when SMUTE pin is returned to "L"(The SW2 is upper position), the mute is cancelled and the output attenuation gradually changes to 0dB in 1024 LRCK cycles. If the soft mute is released within 1024 LRCK cycles after starting the operation, the attenuation is recovered to 0dB with same gradient and cycles.
The soft mute function is effective when changing the signal source without stopping the signal transmission.

■ Serial control circuit [SW6~10]

The AKD4317 includes a serial control circuit. It could set up the volume by using the SW6~9 and output mode, De-emphasis type and attenuation mode by using the SW10. Under the following, how to set up and control.
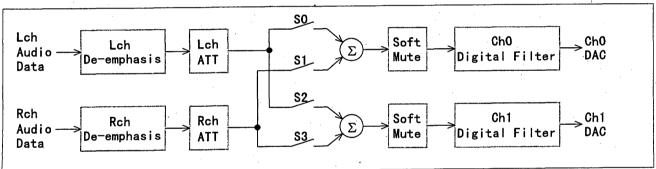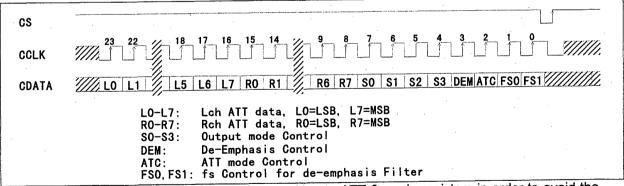

Figure 7. Configuration of attenuator and mixer

L0-L7:   Lch ATT data, L0=LSB, L7=MSB
R0-R7:   Rch ATT data, R0=LSB, R7=MSB
S0-S3:   Output mode Control
DEM: De-Emphasis Control
ATC: ATT mode Control
FS0,FS1:   fs Control for de-emphasis Filter

note: CCLK should be held "H" or "L" except writing to ATT & mode registers in order to avoid the performance degradation.

Figure 8. Serial mode control timing

1. Attenuation level of left and right channel [SW6~9]

SW6: 4bit(L0~L3) of LSB bits in Lch
SW7: 4bit(L4~L7) of MSB bits in Lch
SW8: 4bit(R0~R3) of LSB bits in Rch
SW9: 4bit(R4~R7) of MSB bits in Rch

＊Set up these 4-bits by HEX code.
Equation of attenuation level :

ATT = 20 Log$_{10}$(Binary level/255).
FFH: ATT=0dB,   00H: ATT=MUTE (Infinity zero:-∞)
＊The table of attenuation level are shown in APPENDIX.1(P.17).

The transition between ATT values is same as soft mute operation. When current value is ATT1 and new value is set as ATT2, ATT1 gradually becomes ATT2 with same operation as soft mute. If new value is set as ATT3 before reaching ATT2. ATT value gradually becomes ATT3 from the way of transition.
Cycle time of the soft mute :   Ts = 1024/fs
When resetting, ATT value is set 00H(Infinity zero). ATT value gradually changes from 00H to FFH(0dB) during Ts after exiting reset.

2. Output mode, De-emphasis control, attenuation control and De-emphasis frequency.
[SW10]

2-①. The output modes [SW10-1,2,3,4]

· Normal stereo output
· L/R reverse output
· Monaural mixing output: (L+R)/2
· Output muting with soft mute operation

Table 3. Output mode

S0	S1	S2	S3	AOUT0	AOUT1	Mode
0	0	0	0	MUTE	MUTE	MUTE
0	0	0	1	MUTE	R	
0	0	1	0	MUTE	L	
0	0	1	1	MUTE	(L+R)/2	
0	1	0	0	R	MUTE	
0	1	0	1	R	R	Reverse
0	1	1	0	R	L	
0	1	1	1	R	(L+R)/2	
1	0	0	0	L	MUTE	
1	0	0	1	L	R	Stereo
1	0	1	0	L	L	
1	0	1	1	L	(L+R)/2	
1	1	0	0	(L+R)/2	MUTE	
1	1	0	1	(L+R)/2	R	
1	1	1	0	(L+R)/2	L	
1	1	1	1	(L+R)/2	(L+R)/2	MONO

※ At resetting

2-②. De-emphasis control [SW10-5]

When DEM bit goes "1", De-emphasis filter(50/15 μ s) could be used. Because of DEM bit and DEM pin are ORed internally, DEM pin should be "L". When resetting, DEM bit is set "0"(OFF).

2-③. Attenuation control [SW10-6]

ATT values of both channel are set Lch ATT data by setting ATT bit "1". In this case, Rch ATT data is ignored. When resetting, ATT bit is set "0" (individual control).

2-④. De-emphasis frequency [SW10-7,8]

The de-emphasis(tc=50/15 μ s) corresponding to fs(sampling frequency)=32kHz,44.1kHz and 48kHz is selected by FS0 and FS1 bits. But it is effective which DEM bit is only set "1". DEM pin and DEM bit are ORed internally, DEM pin should be set "L". When resetting, FS0 bit and FS1 bit are set "0".

Table 4. DIP-Switch（SW10）Set-up

No.	PIN	MODE	
1	S0	Set up the output	
2	S1	mode.	
3	S2	See the Table 3.	
4	S3		
5	DEM	De-emphasis mode	
6	ATC	Attenuation mode	
7	FS0	De-emphasis frequency	
8	FS1	See the Table 5.	

Table 5. De-emphasis frequency

FS0	FS1	Frequency
OFF	OFF	44.1KHz
ON	OFF	OFF
OFF	ON	48KHz
ON	ON	32kHz

∗ "H" is set at ON and "L" at OFF.

3. Frequency for control clock(CCLK) [SW5]

Table 6. DIP-Switch(SW5) frequency for control clock

C	B	A	Frequency
~~OFF~~	~~OFF~~	~~OFF~~	~~10MHz~~
OFF	OFF	ON	5MHz
OFF	ON	OFF	2.5MHz
OFF	ON	ON	1250kHz
ON	OFF	OFF	625kHz
ON	OFF	ON	312.5kHz
ON	ON	OFF	156.25kHz
ON	ON	ON	78.125KHz

[J12]: Set up the control clock
    Open: The control clock is output.
    Short: The control clock is stand-by mode.

∗ **The control clock should be set less than 5MHz.**

4. When pushing the SW3, the control data set by ①&② is latched into the AK4317.

∗ **When resetting, ATT values of both channels are FFH and the attenuation levels are set to 0dB. The output mode is also set to normal stereo output. DEM bit, ATC bit, FS0 bit and FS1 bit are set to ALL "0".**

■   The function of the others

    [SW1]   Resets the AK4317. Put the upper position during conversion.
    [LE1]   Indicates whether the input data is pre-emphasized or not. LED turns on when the data is pre-emphasized.
    [LE2]   Monitors VERF pin of the CS8412. LED turns on when some error has occurred to CS8412.

AK4317 Measurement Examples

Dynamic performance by ROHDE&SCHWARZ UPD04

fs	32kHz	44.1kHz	48kHz	Measurement Filter
THD+N	-87.6dB	-88.1dB	-88.8dB	20kLPF
Dynamic Range	91.2dB	92.3dB	92.7dB	20kLPF+A-Weight
S/N	91.3dB	92.4dB	92.6dB	20kLPF+A-Weight

[Conditions]
- Device : AK4317
- DVDD=AVDD : 5.0V
- Measurement unit : ROHDE6SCHWARZ UPD04
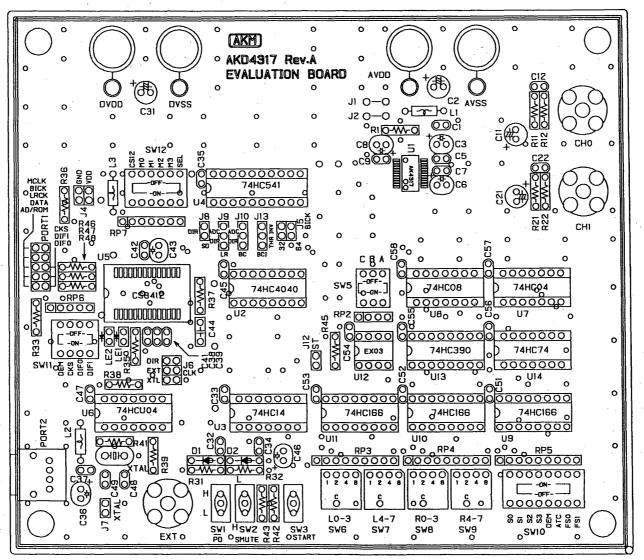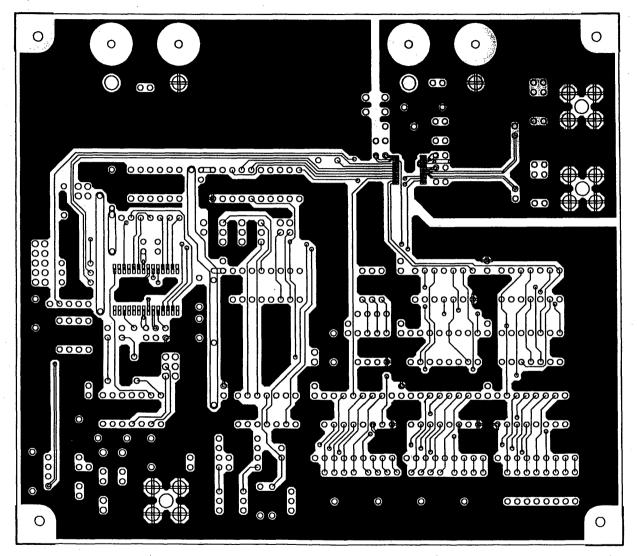- Interface : DIR
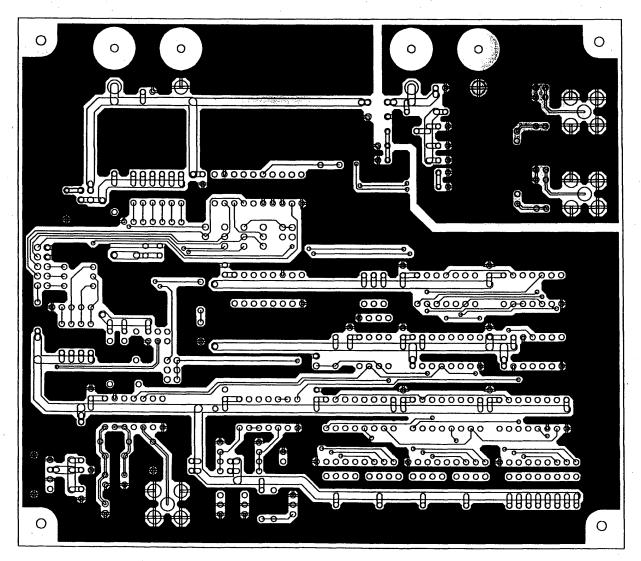- CLK : 256fs
- BICK : 64fs
- Input data : 18bit
- fin : 1kHz
- Temperature : Room temperature

[AKM]

AKD4317 Rev.A
EVALUATION BOARD

DVDD   DVSS   AVDD   AVSS

C31   C2

J1 O—O
J2 O—O   L1

R1   C1

C8   U1   C3
C9   C5
C7
C6

C12
R11 R12   CH0

C11

C22
R21 R22   CH1
C21

MCLK
BICK
LRCK
DATA
AD/ROM

PORT1

CKS
DIFI
DIFO

R36   GND VDD   L3   SW12
CSI2 M0 M1 M2 M3 SEL
OFF
ON

C35   74HC541   U4

R46
R47
R48

RP7

U5   C42 C43

CS8412

J8 J9 J10 J13   J5 BICK
DIR   THR INV
S0   ADC ADC DIR   32 64
LR BC BCI

74HC4040   U2

C B A   C58   C57
OFF
ON
SW5   RP2
C45   R37
C44   R45
RP6

R33   OFF ON   SW11
OEM CKS DIFO DIFI
LE2 LEI R35
R38   DIR EXT XTL
C41 C38 C39   J6 CLK

74HC08   U8
74HC04   U7

C55   C56
EX03   U12   74HC390   U13   74HC74   U14
J12 ST   C54   C52   C51
C53

C47   C33   74HC14   U3
U6   74HCU04

74HC166   U11
74HC166   U10
74HC166   U9

PORT2   L2
R41
XTAL   R39
C37 C49 C48
C36   J7   XTAL   EXT

D1 C32 D2 C34 C46
R31   L
H   L
SW1 PD   SW2 SMUTE   R43 R42   SW3 START
R32

RP3   RP4   RP5

1 2 4 8   1 2 4 8   1 2 4 8   1 2 4 8
C   C   C   C
L0-3   L4-7   R0-3   R4-7
SW6   SW7   SW8   SW9

ON
OFF
S0 S1 S2 S3 OEM ATC FS0 FS1
SW10

AKD4317 RevA L1 SBK

AKD4317 RevA L1

AKD4317 RevA .L2