

LPM9014

N-Channel Enhancement Mode Field Effect Transistor

General Description

The LPM9014 uses advanced trench technology to provide excellent RDS(ON), low gate charge operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications. Standard Product LPM9014 is Pb-free (meets ROHS & Sonv 259 specifications). LPM9014L is a Green Product ordering option. LPM9014 and LPM9014L are electrically identical.

Features

VDS(V) = 20V

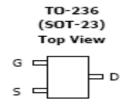
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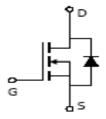
 $RDS(ON) < 50m\Omega (VGS = 4.5V)$

RDS(ON) $< 63 \text{m}\Omega \text{ (VGS = 2.5V)}$

RDS(ON) $< 87m\Omega$ (VGS = 1.8V)

Pin Configurations





Absolute Maximum Ratings T _A =25°C unless otherwise noted								
Parameter		Symbol	Maximum	Units				
Drain-Source Voltage		V _{DS}	20	~				
Gate-Source Voltage		V _{GS}	±8	V				
Continuous Drain	T _A =25°C		4.2					
Current ^A	T _A =70°C	I₀	3.2	A				
Pulsed Drain Current ⁸		I _{DM}	15					
	T _A =25°C	PD	1.4	w				
Power Dissipation A	T _A =70°C	75	0.9	VV				
Junction and Storage Temperature Range		T _J , T _{STG}	-55 to 150	°C				

Thermal Characteristics									
Parameter		Symbol	Тур	Max	Units				
Maximum Junction-to-Ambient ^A	t ≤ 10s	≤ 10s R _{eJA}		90	°C/W				
Maximum Junction-to-Ambient A	Steady-State	T eJA	100	125	°C/W				
Maximum Junction-to-Lead ^C	Steady-State	R _{eJL}	63	80	°C/W				



Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter Conditions		Min	Тур	Max	Units			
STATIC PARAMETERS									
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	20			V			
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =16V, V _{GS} =0V			1	μА			
		T _J =55°	C		5	.			
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±8V			100	nΑ			
$V_{GS(th)}$	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	0.4	0.6	1	V			
I _{D(ON)}	On state drain current	V _{GS} =4.5V, V _{DS} =5V	15			Α			
R _{DS(ON)} Sta	Static Drain-Source On-Resistance	V _{GS} =4.5V, I _D =4.2A		41	50	mΩ			
		T _J =125°	C	58	70				
	State State Society Strikesistanes	V _{GS} =2.5V, I _D =3.7A		52	63	mΩ			
		V _{GS} =1.8V, I _D =3.2A		67	87	mΩ			
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =4.2A		11		S			
V_{SD}	Diode Forward Voltage	I _S =1A,V _{GS} =0V		0.76	1	V			
Is	Maximum Body-Diode Continuous Current				2	Α			
DYNAMIC	PARAMETERS								
C _{iss}	Input Capacitance			436		pF			
Coss	Output Capacitance	V _{GS} =0V, V _{DS} =10V, f=1MHz		66		pF			
C _{rss}	Reverse Transfer Capacitance]		44		pF			
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		3		Ω			
SWITCHII	NG PARAMETERS								
Qg	Total Gate Charge			6.2		nC			
Qgs	Gate Source Charge	V _{GS} =4.5V, V _{DS} =10V, I _D =4.2A		1.6		nC			
Q_{gd}	Gate Drain Charge]		0.5		nC			
t _{D(on)}	Turn-On DelayTime			5.5		ns			
t _r	Turn-On Rise Time	V_{GS} =5V, V_{DS} =10V, R_L =2.7 Ω ,		6.3		ns			
t _{D(off)}	Turn-Off DelayTime	$R_{GEN}=6\Omega$		40		ns			
t _f	Turn-Off Fall Time			12.7		ns			
t _{rr}	Body Diode Reverse Recovery Time	I _F =4A, dl/dt=100A/μs		12.3		ns			
Qm	Body Diode Reverse Recovery Charge	I _F =4A, dI/dt=100A/μs		3.5		nC			

A: The value of R_{BIA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R $_{\text{NA}}$ is the sum of the thermal impedence from junction to lead R $_{\text{NL}}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using $80\,\mu s$ pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The SOA curve provides a single pulse rating.



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

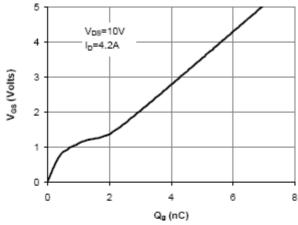


Figure 7: Gate-Charge Characteristics

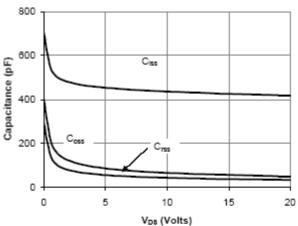


Figure 8: Capacitance Characteristics

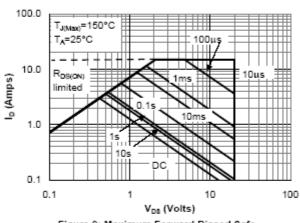


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

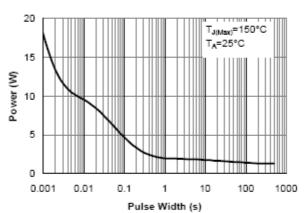


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

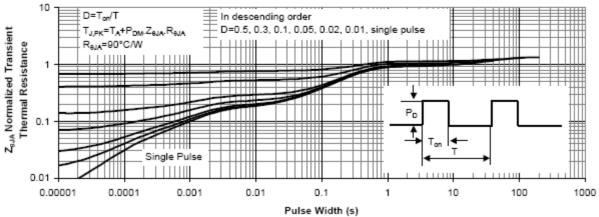


Figure 11: Normalized Maximum Transient Thermal Impedance