

Keysight M9203A

PXIe High-Speed Digitizer/ Wideband Digital Receiver

2 channels, 12-bit, up to 3.2 GS/s,
DC to 2 GHz bandwidth

Data Sheet



PXIExpress™

Overview



Introduction

The Keysight M9203A is a very fast and low noise PXIe High-Speed Digitizer/Wideband Digital Receiver featuring wide analog bandwidth, making it ideal for wireless, radar and satellite communication applications or any application requiring wideband signal capture, and at the same time very high dynamic range. Thanks to its PCI Express® backplane connection, the M9203A supports continuous data streaming to disk.

Product description

The M9203A is a dual-slot 3U PXIe 12-bit High-Speed Digitizer/Wideband Digital Receiver running at 3.2 GS/s, with up to 2 GHz instantaneous analog bandwidth and providing a large 4 GB DDR3 acquisition memory. The M9203A features a large Xilinx Virtex-6 FPGA that can implement different functionalities depending on which firmware option you choose.

The M9203A PXIe High-Speed Digitizer/Wideband Digital Receiver can also be combined with the Keysight 89600 VSA software for advanced dual-channel signal analysis.

For information on other firmware options please contact Keysight Technologies: digitizers@keysight.com

Example applications

- Wireless communication (5G, LTE)
- Emerging communication standards (e.g. DOCSIS 3.1)
- Radar and wideband signal capture
- Radar and satellite communication applications
- Semiconductor automated test

Product features

- 1 channel with 12-bit resolution up to 3.2 GS/s sampling rate with interleaving enabled
- 2 channels up to 1.6 GS/s simultaneous sampling rate
- DC up to 2 GHz bandwidth
- 50 Ω input impedance, DC coupled
- Selectable 1 V or 2 V full scale range (FSR)
- ± 200 fs channel-to-channel skew stability
- 15 ps RMS trigger time interpolator (TTI) precision
- Up to 4 GB DDR3 on-board memory
- Enhanced real-time processing using Xilinx Virtex-6 FPGA
- Support for loading custom real-time processing
- High data throughput PCIe® Gen2 (x8) backplane
- Real-time digital down-conversion (-DDC) with adjustable center frequency and analysis bandwidth
- Real-time digitizer raw data streaming and recording bundle
- Real-time digital down-conversion with I/Q data streaming (-CB0) and recording bundle (-CB2)

Uncompromising values

- Fast PXIe 12-bit wideband digitizer with on-board real-time processing
- Capture wide bandwidth signals
- High dynamic range acquisition for better measurement fidelity
- Accurate long term measurement
- Capable of switching between multiple firmware programs
- Self-trigger mode for unequaled synchronous noise reduction
- Open FPGA for custom process
- Reduced test time by tuning and zooming on signals (-DDC)
- Up to 1 GHz baseband streaming and recording (-CB0)
- Dual channel phase coherent streaming and recording with up to 320 MHz alias protected IBW (-CB2)

Hardware platform

Product overview

The M9203A is PXI Express compliant. Designed to benefit from fast data interfaces, the product can be integrated in PXIe and PXI Hybrid chassis slots. The PXI format offers high performance in a small, rugged package. It is an ideal deployment platform for many automated measurements systems.

On-board real-time processing

At the heart of the M9203A PXIe High-Speed Digitizer/Wideband Digital Receiver is a data processing unit (DPU) based on the powerful Xilinx Virtex-6 FPGA. This DPU is responsible for controlling the module functionality, data flow and real-time signal processing. This powerful feature allows data reduction and storage to be carried out at the digitizer level, minimizing transfer volumes and speeding-up analysis.

Block diagram

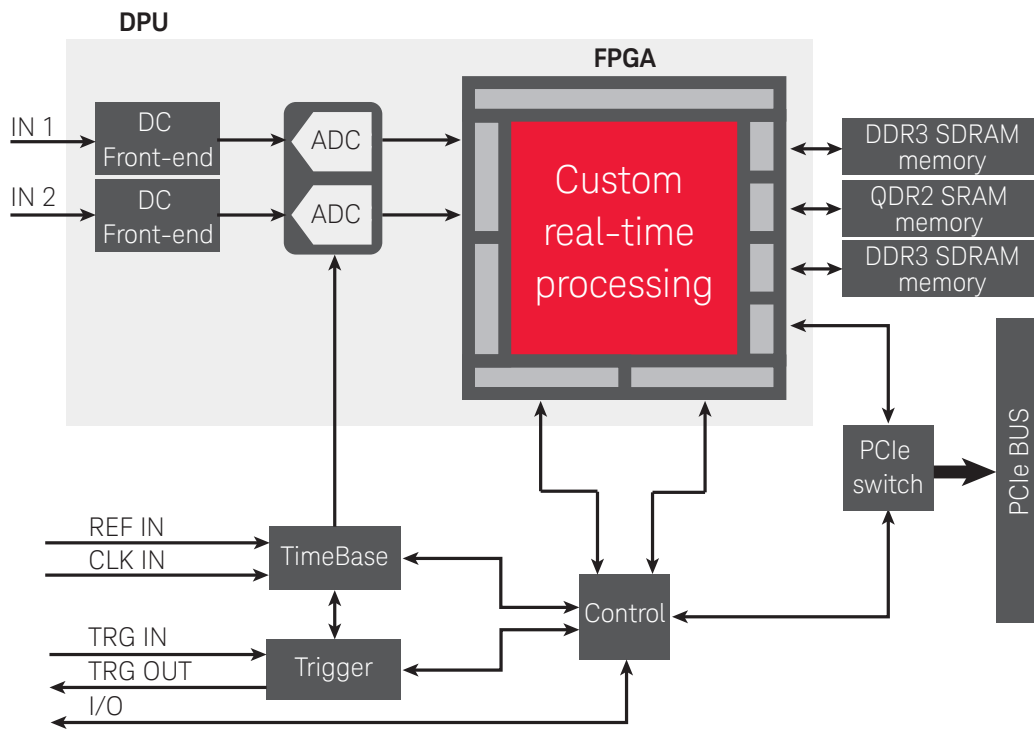


Figure 1. Simplified block diagram of the M9203A PXIe High-Speed Digitizer/Wideband Digital Receiver.

Software Platform

Keysight Software Suite

Keysight IO Libraries Suite offers fast and easy connection to instruments and the newest version extends that capability to include modular instruments.

Drivers

The module comes with the IviDigitizer class compliant Keysight MD2 IVI-COM and IVI-C drivers that work in the most popular development environments including Visual C/C++, C#, VB.NET, MATLAB, and LabVIEW. Linux is also supported using the IVI-C driver.

Easy software integration

To help you get started and complete complex tasks quickly, the M9203A PXIe Wideband Digitizer is supplied with a comprehensive portfolio of module drivers, documentation, examples, and software tools to help you quickly develop test systems with your software platform of choice.

Compliance

The M9203A is PXI Express compliant. Designed to benefit from fast data interfaces, the product can be integrated in PXIe and PXI Hybrid chassis slots.

Software applications

In addition, the M9203A includes the Keysight MD2 soft front panel (SFP) graphical interface. This software application can be used to explore the capabilities of the Keysight modular high-speed digitizers.

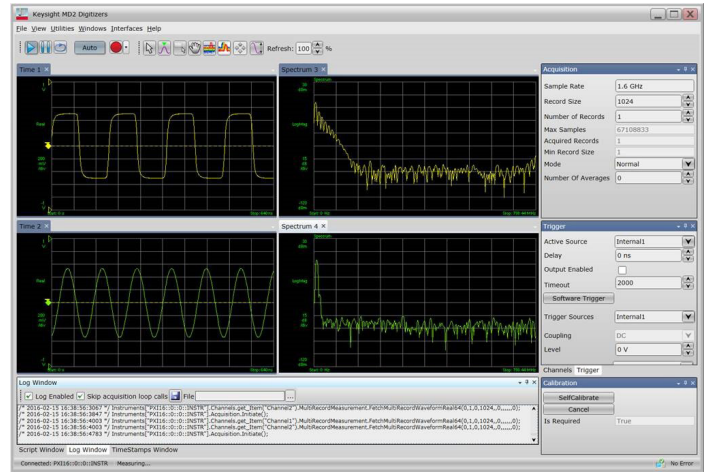


Figure 2. MD2 software front panel (SFP) interface.

For advanced measurement analysis, the M9203A PXIe High-Speed Digitizer/Wideband Digital Receiver can be combined with Keysight's 89600 Vector Signal Analysis software, the industry's standard for signal analysis and demodulation. The M9203A allows fast connection to the 89600 VSA software through its high data throughput PCIe backplane, compared to traditional instruments.

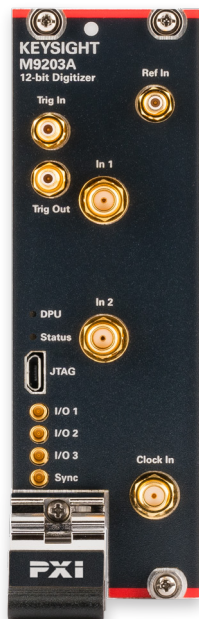


Figure 3. M9203A front panel with analog inputs and multiple I/O signals.

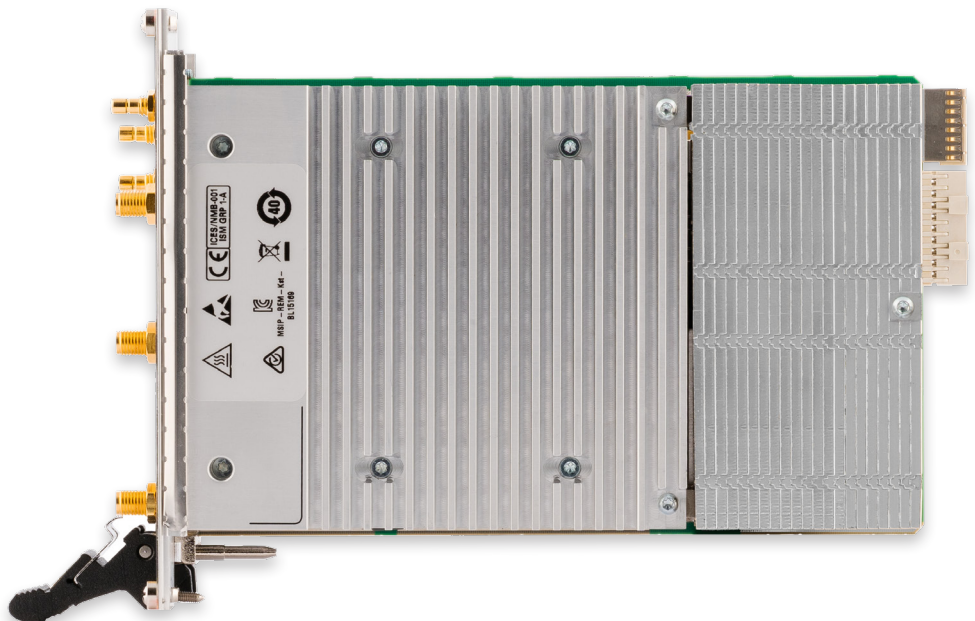


Figure 4. M9203A PXIe 12-bit High-Speed Digitizer/Wideband Digital Receiver offers a small size for easy integration within a PXIe chassis.

Firmware Options

The M9203A PXIe High-Speed Digitizer/Wideband Digital Receiver provides several firmware options:

- **DGT**: Digitizer firmware
- **INT**: Interleaved channel sampling functionality
- **FDK**¹: Custom firmware capability
- **TSR**²: Triggered simultaneous acquisition and readout
- **DDC**: Wideband real-time digital down-conversion

Easy firmware switch

A simple call to the configuration function will enable to switch to the required option.

DGT digitizer firmware

The digitizer firmware:

- Allows standard data acquisition, including: digitizer initialization, setting of the acquisition and clocking modes, management of channel triggering for best synchronization, storing data in the internal memory and/or transferring them through the backplane bus.
- Implements multi-record acquisition functionality.
- Supports fixed internal clocking frequency with internal or external reference, and variable frequency external clock.
- Offers programmable binary decimation to lower the sample rate by a factor of 2^n where n is defined in the range 1 to 10 for single record.
e.g. you can select from 1.6 GS/s down to 1.5625 MS/s.
- Trigger time interpolator (TTI): high precision integrated time to digital converter can be used to increase time measurement accuracy.

INT interleaved channel sampling functionality

This interleave option allows two channels to be combined and to reach 3.2 GS/s in one channel acquisition mode.

FDK custom firmware capability

This option enables loading⁴ custom firmware created with the U5340A FPGA development kit⁵.

TSR triggered simultaneous acquisition and readout

The triggered simultaneous acquisition and readout architecture allows to continuously acquire new records while reading previous ones.

TSR solution is dedicated to applications requiring no trigger loss, achieving longer recording time when compares with standard digitizer (-DGT).

TSR option main features:

- High trigger rate with guaranteed no lost trigger for specific configuration³.
- Easy to use solution, implementing an optimal and automated control of memory addressing.
- Selecting larger memory size option allows longer record size and provides larger buffer for data transfer to host PC, especially useful for applications with non-periodic trigger or very high trigger rate during a limited period.

DDC real-time digital down-conversion

The real-time digital down-conversion option (-DDC), in addition to the basic digitizer functionality, implements a real-time digital decimation and filtering on the digitized data, allowing the user to tune and zoom on the signals of interest. This exclusive IP algorithm provides very powerful and flexible digital down-conversion on 2 channels. The filters and local oscillators (LO) are synchronized to maintain constant phase and timing relationships allowing phase-coherent post processing.

The DDC provides three main functions:

- Frequency shifting (tune): Independently shifting each channels IF signal into baseband, allows the analysis bandwidth to be set around the signal of interest.
- Data reduction (zoom): Reducing the bandwidth and sample rate to match the analyzed signal decreases the amount of data that needs to be transferred for a given capture duration, in turn accelerating post-processing operations.
- Magnitude trigger: Setting the magnitude level that the down converted signal needs to achieve at a specified frequency and bandwidth to generate a digital trigger on all channels.

These functions allow isolation of the signal of interest from other signals in a crowded spectrum, improved dynamic range as the integrated noise is reduced, and increased SNR and effective number of bits (ENOB). The resulting advantage for your application is a reduced test time, while improving overall test efficiency.

1. A calibration digitizer function is available with each firmware.
2. Only available with DGT option.
3. Please contact Keysight to find out the repetition rate that can be achieved in your application.
4. On the Virtex-6 LX195T DPU FPGA.
5. There are 11 W maximum power dedicated to FPGA processing, the custom firmware design must fit within this power provision.

Firmware Development

U5340A - FPGA Development Kit¹

The FPGA development kit is primarily intended to open the design of the FPGA to specific user requirements by providing a development framework that interfaces to the underlying hardware.

The FPGA development kit combines capabilities to:

- Achieve multi GS/s real-time processing on a full digitizer framework by leveraging the full density and speed of the FPGA.
- Shorten time-to-market with turn-key, easy-to-use development flow and debug.

There are several rationales to consider developing custom signal processing such as:

- Data throughput optimization
- Real time processing
- Implementation of custom IP and OEM technical know-how
- Re-usability and upgradability.

The FPGA development kit includes everything you need: source code, ready-to-use base design, a set of cores to easily interface to the underlying hardware, a test-bench environment for design and simulation, and automated building script.

For more information:

Keysight U5340A - FPGA Development Kit for High-Speed Digitizers
 Keysight product brochure 5991-2424EN
<http://literature.cdn.keysight.com/litweb/pdf/5991-2424EN.pdf>

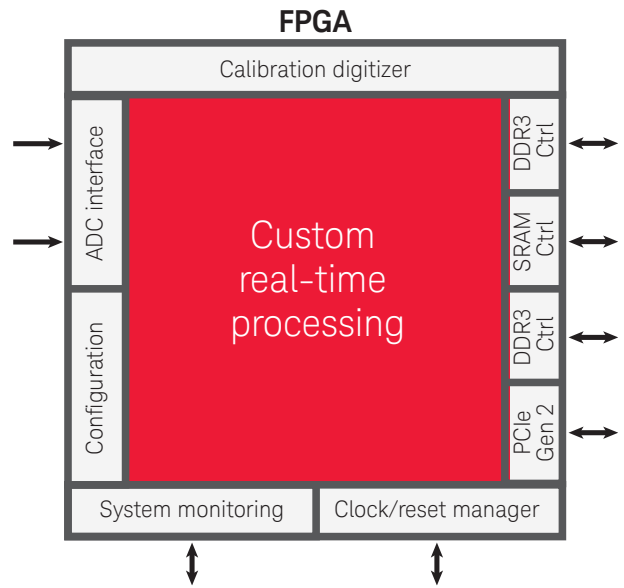


Figure 5. Enlarged block diagram of the FPGA Xilinx Virtex-6

- Predefined Keysight IP cores
- Custom real-time processing (using the FPGA development kit)

1. This standalone software package must be acquired separately.

Application Options¹

For specific applications the M9203A PXIe High-Speed Digitizer/Wideband Digital Receiver can be configured with specific options:

- **CB0**: Digitizer streaming and recording
- **CB2**: Digital down converter streaming and recording at 1.6 GS/s
- **BB1**: High fidelity digitizer

CB0 digitizer streaming and recording

CB0 is a turnkey reference bundle, based on the continuous simultaneous acquisition and readout architecture, implementing a real time digitizer data recorder for gapless acquisition. It includes a command line application ensuring performance of up to 2 GB/s² in a specific qualified system. An easy to use data viewer application is also provided.

This digitizer streaming and recording option with bundled applications provides:

- Guaranteed recording specification
- Various recording speed controlled by application
- Adaptable sampling rate (decimation and external clock)
- Data throughput optimization (12-bit, 10-bit or 8-bit mode).

This option is added on top of a M9203A pre-configured version composed of:

- 1.6 GS/s sampling rate (-SR2) or up to 2 GS/s (-SR2, -INT, with external clock)
- Full bandwidth (-F10)
- 4 GB acquisition memory (-M40)
- Digitizer firmware (-DGT)

The digitizer data streamer application is an intuitive command line application which allows to control the M9203A and adapts its data rate to the target application.

The data viewer is a graphical user interface (GUI) application which allows to read, display, select and export the data stored.



Figure 6. Streaming options (-CB0, -CB2) are proposed with a recommended host PC and SSD. Performance is guaranteed with specific configurations³.

Maximum streaming and recording performance is guaranteed using an additional qualified host computer system with specific storage devices configuration.⁴

1. Application options are delivered on the high-speed digitizer DVD.
2. Equivalent to: 2 GS/s in 8-bit mode, 1.6 GS/s in 10-bit mode, and 1.3 GS/s in 12-bit mode.
3. To reach the guaranteed performances the system requires both an external computer and data storage.
4. Keysight proposes full system and installation services. Please contact support at digitizers@keysight.com for additional information.

CB2 digital down-conversion streaming and recording

This bundle enables continuous gapless acquisition, implementing:

- Digital down converter functionality in real time
- Data steaming to host
- Multichannel recording to disk all I/Q samples for later analysis.
- Independent local-oscillators, with phase-coherency between channels.

The -CB2 option is added on top of a M9203A pre-configured version composed of:

- 1.6 GS/s sampling rate (-SR2)
- Full bandwidth (-F10)
- 4 GB acquisition memory (-M40)
- Digitizer firmware (-DGT)

This option provides:

- Guaranteed recording specification up to 320 MHz instantaneous bandwidth (IBW) with tunable intermediate frequency with recommended configuration.
- Data throughput optimization (I/Q samples with 32-bit, 16-bit or 12-bit mode).

The option includes an intuitive command line application allowing to control the M9203A and a data viewer providing a simple graphical user interface (GUI) which allows to read, display, select and export the data stored.

Maximum streaming and recording performance is guaranteed using an additional qualified host computer system with specific storage devices configuration.⁴

BB1 high fidelity digitizer

This high fidelity digitizer option provides enhanced performance by:

- Compensating the ADC and front-end distortion
- Minimizing interleave spurs
- Reducing the overall noise bandwidth.

This results in highly improved and uniform measurement fidelity across the useful bandwidth, which greatly benefits RF and wireless frequency domain measurements. The digitizer's post processing compensation also delivers better spurious-free dynamic range (SFDR) and intermodulation product (IMx) specifications.

This application option is pre-configured with:

- 1.6 GS/s sampling rate (-SR2)

Leaving choice of bandwidth and memory, for optional use in -BB1 mode, recommendation is:

- 650 MHz bandwidth (-F05)
- 256 MB acquisition memory (-M02)

It allows the following usage as high fidelity digitizer:

- 1.6 GS/s with 650 MHz bandwidth, up to 64 MSamples/ch.
- 800 MS/s with 400 MHz bandwidth, up to 32 MSamples/ch.
- 400 MS/s with 200 MHz bandwidth, up to 16 MSamples/ch.
- 200 MS/s with 100 MHz bandwidth, up to 8 MSamples/ch.
- 100 MS/s with 50 MHz bandwidth, up to 4 MSamples/ch.

Technical Specifications and Characteristics

Analog input (IN1 and IN2 SMA connectors)		
Number of channels		2 (without INT option), 2 or 1 (with INT option)
Impedance		50 Ω \pm 2 %
Coupling		DC
Full scale ranges (FSR)		1 V and 2 V
Maximum input voltage		1V FSR: Clamp at \pm 3.6 V, absolute maximum DC voltage rating \pm 4.6 V 2V FSR: Clamp at \pm 6.3 V, absolute maximum DC voltage rating \pm 5.0 V
Input voltage offset		-2xFSR to +2xFSR
Input frequency range (-3 dB bandwidth)	-F05, -SR2	DC to 650 MHz (<i>nominal</i>) in 1V FSR at 1.6 GS/s DC to 650 MHz (<i>nominal</i>) in 2V FSR at 1.6 GS/s
	-F05, -SR2, -INT	DC to 650 MHz (<i>nominal</i>) in 1V FSR at 3.2 GS/s DC to 650 MHz (<i>nominal</i>) in 2V FSR at 3.2 GS/s
	-F10, -SR2	DC to 1.9 GHz (<i>nominal</i>) in 1V FSR at 1.6 GS/s DC to 2.0 GHz (<i>nominal</i>) in 2V FSR at 1.6 GS/s
	-F10, -SR2, -INT	DC to 1.4 GHz (<i>nominal</i>) in 1V FSR at 3.2 GS/s DC to 1.4 GHz (<i>nominal</i>) in 2V FSR at 3.2 GS/s
DC gain accuracy		\pm 0.5% (<i>nominal</i>) in 1V FSR \pm 0.7% (<i>nominal</i>) in 2V FSR
Offset accuracy		\pm 0.5% in 1V FSR \pm 1.5% in 2V FSR
Time skew ¹	Skew between channels ²	50 ps (<i>nominal</i>)
	Channel-to-channel skew stability ³	\pm 200 fs pk (<i>nominal</i>) 75 fs RMS (<i>nominal</i>) ²
Bandwidth limit filters (BWL)		650 MHz (<i>nominal</i>) for -SR2
Effective number of bits (ENOB) ⁴	-SR2	@ 410 MHz 9.1 (<i>nominal</i>)
Signal to noise ratio (SNR) ⁴	-SR2	@ 410 MHz 57 dB (<i>nominal</i>)
Spurious free dynamic range (SFDR) ⁴	-SR2	@ 410 MHz 64 dBc (<i>nominal</i>)
Total harmonic distortion (THD) ⁴	-SR2	@ 410 MHz -64 dB (<i>nominal</i>)

1. The channel-to-channel skew is defined as the magnitude of time delay difference between two digitized channel inputs, granted the same signal is provided to each channel at the exact same time.
2. The measurement represents the maximum time skew between 2 channels of a single unit, measured with a Sinefit method on 100 kSamples, for a sinusoid signal at 400 MHz and averaged 10 times.
3. Skew and offset stability are measured at 25 °C in a climatic chamber. The skew and offset between channels are measured every 5 minutes over 12 hours and after 1 hour stabilization time and the values represent the dispersion of the measurements.
4. Measured for a -1 dBFS input signal in internal clock mode with option -F10 at 1.6 GS/s (option -SR2).

Technical Specifications and Characteristics *(continued)*

Digital conversion			
Resolution			12 bits
Acquisition memory	-M02		256 MB (64 MSamples/ch)
	-M10		1 GB (256 MSamples/ch)
	-M40		4 GB (1 GSamples/ch)
Sample clock sources			Internal or external
Internal clock source			Internal, external reference
Real-time sampling rates	-SR2		1.6 GS/s
	-SR2, -INT		3.2 GS/s
Sampling jitter			225 fs (<i>nominal</i>) ¹
Clock accuracy			±15 ppm (<i>nominal</i>)
External clock source (CLK IN MMCX connector)			
Impedance			50 Ω (<i>nominal</i>)
Frequency range ²	-SR2		1.8 GHz to 3.2 GHz
Signal level			+5 dBm to +15 dBm (<i>nominal</i>), 0 V DC
Coupling			AC
External reference clock (REF IN SMB connector)			
Impedance			50 Ω (<i>nominal</i>)
Frequency range			100 MHz ±1 kHz (<i>nominal</i>)
Signal level			-3 dBm to +3 dBm (<i>nominal</i>)
Coupling			AC
Acquisition modes (depends on firmware options)			Single shot, sequence ³ , continuous

1. Jitter figure based on phase noise integration from 100 Hz to 1600 MHz.

2. The sampling rate corresponds to half of the external clock frequency in 2-channel mode (non interleaved channels). In interleaved mode (only available with the INT option), the sampling rate corresponds to the frequency of the external clock signal.

3. Up to 131072 records. Record maximum length = memory size/number of channels.

Technical Specifications and Characteristics *(continued)*

Trigger		
Trigger modes		Positive or negative edge
Trigger sources		External, Software, Channel
Channel trigger frequency range		DC to 250 MHz
External trigger (TRG IN SMB connector)		
Coupling		DC
Impedance		50 Ω (<i>nominal</i>)
Level range		± 5 V (<i>nominal</i>)
Minimum amplitude		0.5 V pk-pk
Frequency range		DC to 2 GHz (<i>nominal</i>)
Maximum time stamp duration	-SR2	32 days
Trigger time interpolator resolution ⁴		6.25 ps (<i>nominal</i>)
Trigger time interpolator precision ⁴		15 ps RMS (<i>nominal</i>)
Rearm time (deadtime)	-SR2	500 ns (<i>nominal</i>)
Trigger out (TRG OUT SMB connector) ¹		1 (programmable), 50 Ω source
	Signal level	0.8 Vpp ± 2.5 Voffset (<i>nominal</i>) into high impedance
Control IO (I/O 1 and 2 MMCX connectors)²		
Output functions		Acquisition active Trigger is armed Trigger accept resynchronization 100 MHz reference clock divided by 2 ³ Sampling clock divided by 32 ³ Low level High level FPGA synchronization
Input/output function		FPGA programmable I/O

1. At 10 MHz on a 50 Ω load.

2. I/O 3 reserved for future use.

3. Only on I/O 1.

4. At maximum sample rate or at decimated sampling rate down to 1/16 of the highest sample rate (1/32 of the highest sample rate with interleaving).

Technical Specifications and Characteristics *(continued)*

Environmental and physical¹		
Temperature range	Operating	0 to +50 °C (sea-level to 10,000 feet) ² 0 to +45 °C (10,000 to 15,000 feet) ²
	Non-operating	-40 to +70 °C
Altitude		Up to 15,000 feet (4'572 meters)
EMC		Complies with European EMC Directive <ul style="list-style-type: none"> - IEC/EN 61326-1 - CISPR Pub 11 Group 1, class A - AS/NZS CISPR 11 - ICES/NMB-001 This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme à la norme NMB-001 du Canada.
Acoustic		European Machinery Directive Acoustic noise emission LpA < 70 dB Operator position Normal operation mode
Power dissipation		
+ 3.3 V	+ 12 V	Power on PXI connector
3.2 A (<i>typical</i>)	3.5 A (<i>typical</i>)	55 W (<i>typical</i>)
Mechanical characteristics		
Form Factor		3U/2-slot PXI-Express Chassis slot compatibility: PXI Hybrid, PXIe Front panel complies with IEEE1101.10 certification
Size		Length 185 mm x Width 130 mm x Height 40mm
Weight		0.8 kg (1.76 lbs)

1. Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.

Technical Specifications and Characteristics *(continued)*

System requirements		
Topic	Windows	Linux
Operating systems	Windows 10 (32-bit and 64-bit), All versions Windows 8.1 (32-bit and 64-bit), All versions Windows 7 SP1 (32-bit and 64-bit). Note: If using high-speed digitizer applications DVD, Windows 7 (64-bit) is supported.	Linux Kernel 2.6 or higher (32 or 64-bit), Debian 7.0, CentOS 6
Processor speed	1 GHz 32-bit (x86), 1 GHz 64-bit (x64), no support for Itanium 64	As per the minimum requirements of the chosen distribution
Available memory	1 GB minimum ¹	As per the minimum requirements of the chosen distribution
Available disk space	2.5 GB available hard disk space, includes: ² – 1 GB for Keysight IO Libraries Suite – 1 GB for Microsoft .NET Framework Note: 400 MB for high-speed digitizer applications.	100 MB
Display	Minimum of 1024 x 768, 96 or 120 DPI	No display required
Browser	Use a supported version of Internet Explorer; see http://support.microsoft.com/kb/969393	Distribution supplied browser

Definitions for specifications

Specifications describe the warranted performance of calibrated cards that have been stored for a minimum of 2 hours within the operating temperature range of 0 to 50 °C, unless otherwise stated, and after a 45 minute warm-up period. Data represented in this document are specifications unless otherwise noted.

Characteristics describe product performance that is useful in the application of the product, but that is not covered by the product warranty. Characteristics are often referred to as Typical or Nominal values.

- **Typical** describes characteristic performance, which 80% of cards will meet when operated over a 20 to 30 °C temperature range. Typical performance is not warranted.
- **Nominal** describes representative performance that is useful in the application of the product when operated over a 20 to 30 °C temperature range. Nominal performance is not warranted.

Note: All graphs contain measured data from several units at room temperature unless otherwise noted.

Calibration

The M9203A is factory calibrated and shipped with a certificate of calibration.

1. On older PCs with minimum RAM, installation can take a long time when installing the IO Libraries Suite and the .NET Framework.
2. Because of the installation procedure, less disk space may be required for operation than is required for installation. The amount of space listed above is required for installation. The .NET Framework Runtime Components are installed by default with most Windows installations, so you may not need this amount of available disk space.

Configuration and Ordering Information

Software information

Supported operating systems and host computers	Windows 10, 8.1 or 7 (32-bit and 64-bit), All versions Linux
Standard compliant drivers	IVI-COM, IVI-C, MATLAB
Supported application development environments (ADE)	VisualStudio (VB.NET, C#, C/C++), VEE, LabVIEW, LabWindows/CVI, MATLAB

Related products

Model	Description
M9018A	PXIe 18-slot Chassis
M9021A	PCIe Cable Interface
M9048A	PCIe Desktop Adapter
M9036A	PXIe Embedded Controller
M9037A	PXIe High Performance Embedded Controller
M9393A	PXIe Performance Vector Signal Analyzer: 50 GHz
M9362AD01	PXIe Quad Downconverter: 10 MHz to 50 GHz
89601B	89600 VSA software, transportable license
U5340A	FPGA Development Kit for High-Speed Digitizers

Accessories

Model	Description
U5300A-102	MMCX male to BNC male cable, 1 m
U5300A-112	SMB female to BNC male cable, 0.1 m

Please contact Keysight for other options not shown:
digitizers@keysight.com

Ordering information

Model	Description
M9203A	PXIe 12-bit PXIe High-Speed Digitizer/Wideband Digital Receiver Includes: -Software examples and product information on CD -MMCX male to BNC male cable, 1m (qty 1) -Warranty extended to 3 years

Configurable options

Sampling rate

- ✓ M9203A-SR2 1.6 GS/s sampling rate (3.2 GS/s with -INT option)

Bandwidth

- ✓ M9203A-F05 650 MHz bandwidth
- M9203A-F10 Full bandwidth

Memory

- M9203A-M02 256 MB (64 MS/ch) acquisition memory
- ✓ M9203A-M10 1 GB (256 MS/ch) acquisition memory
- M9203A-M40 4 GB (1 GS/ch) acquisition memory

Firmware

- ✓ M9203A-DGT Digitizer firmware
- M9203A-INT Interleaved channel sampling functionality
- M9203A-FDK Custom firmware capability
- M9203A-TSR Triggered simultaneous acquisition and readout
- M9203A-DDC Wideband real-time digital down-conversion

Applications

- M9203A-CB0 Digitizer streaming and recording
- M9203A-CB2 Digital down-converter streaming at 1.6 GS/s
- M9203A-BB1 High fidelity digitizer

✓ These options represent the standard configuration

Advantage services: calibration and warranty

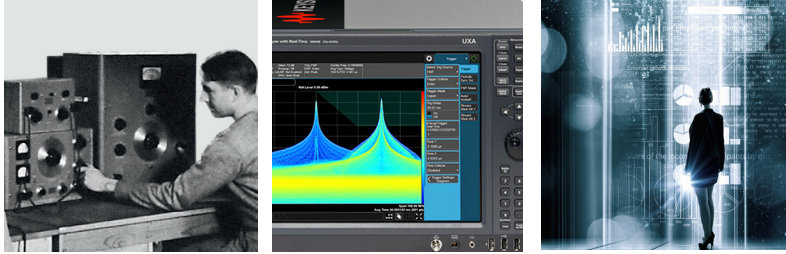
Keysight Advantage Services is committed to your success throughout your equipment's lifetime.

M9203A-A6J	Commercial calibration certificate with test data
Included	Return-to-Keysight warranty – 3 years
R-51B-001-5Z	Return-to-Keysight warranty – 5 years

Evolving Since 1939

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From Hewlett-Packard to Agilent to Keysight.



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Asia Pacific

Australia	1 800 629 485
China	800 810 0189
Hong Kong	800 938 693
India	1 800 11 2626
Japan	0120 (421) 345
Korea	080 769 0800
Malaysia	1 800 888 848
Singapore	1 800 375 8100
Taiwan	0800 047 866
Other AP Countries	(65) 6375 8100

Europe & Middle East

Austria	0800 001122
Belgium	0800 58580
Finland	0800 523252
France	0805 980333
Germany	0800 6270999
Ireland	1800 832700
Israel	1 809 343051
Italy	800 599100
Luxembourg	+32 800 58580
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Russia	8800 5009286
Spain	800 000154
Sweden	0200 882255
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Published in USA, February 27, 2018
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