

20V P-Channel Enhancement-Mode MOSFET

$V_{DS} = -20V$

$R_{DS(ON)}$, $V_{GS} @ -4.5V$, $I_{DS} @ -2.8A = 100m\Omega$

$R_{DS(ON)}$, $V_{GS} @ -2.5V$, $I_{DS} @ -2.0A = 150m\Omega$

Features

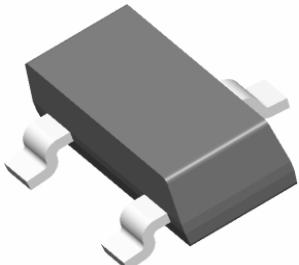
Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

Fully Characterized Avalanche Voltage and Current

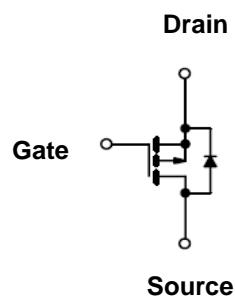
Improved Shoot-Through FOM

**TO-236
(SOT-23)**



Top View

Internal Schematic Diagram



N-Channel MOSFET

Maximum Ratings and Thermal Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|--|-----------------|------------|--------------|
| Drain-Source Voltage | V_{DS} | -20 | V |
| Gate-Source Voltage | V_{GS} | ± 8 | |
| Continuous Drain Current | I_D | -2.3 | A |
| Pulsed Drain Current ¹⁾ | I_{DM} | -10 | |
| Maximum Power Dissipation | P_D | 0.9 | W |
| | | 0.57 | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55 to 150 | $^\circ C$ |
| Avalanche Energy with Single Pulse $I_D=50A$, $V_{DD}=25V$, $L=0.5mH$ | E_{AS} | | mJ |
| Junction-to-Case Thermal Resistance | $R_{\theta JC}$ | | $^\circ C/W$ |
| Junction-to-Ambient Thermal Resistance (PCB mounted) ²⁾ | $R_{\theta JA}$ | 145 | |

Note: 1. Maximum DC current limited by the package

2. 1-in² 2oz Cu PCB board

P-Channel Enhancement-Mode MOSFET ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------------|--------------|--|-------|--------|-----------|-----------|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS} = 0V, I_D = -10\mu A$ | -20 | - | - | V |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = -4.5V, I_D = -2.8A$ | | 69 | 100 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = -2.5V, I_D = -2.0A$ | | 83 | 150 | $m\Omega$ |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = -250\mu A$ | -0.45 | | -0.95 | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = -9.6V, V_{GS} = 0V$ | | | -1 | μA |
| Gate Body Leakage | I_{GSS} | $V_{GS} = \pm 8V, V_{DS} = 0V$ | | | ± 100 | nA |
| Gate Resistance | R_g | | | | | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = -5V, I_D = -4.0A$ | | 6.5 | | S |
| Dynamic | | | | | | |
| Total Gate Charge | Q_g | $V_{DS} = -6V, I_D = -2.8A$ $V_{GS} = -4.5V$ | | 15.23 | | nC |
| Gate-Source Charge | Q_{gs} | | | 5.49 | | |
| Gate-Drain Charge | Q_{gd} | | | 2.74 | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = -6V, R_L = 6\Omega$ $I_D = -1A, V_{GEN} = -4.5V$ $R_G = 6\Omega$ | | 17.28 | | ns |
| Turn-On Rise Time | t_r | | | 3.73 | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 36.05 | | |
| Turn-Off Fall Time | t_f | | | 6.19 | | |
| Input Capacitance | C_{iss} | $V_{DS} = -6V, V_{GS} = 0V$ $f = 1.0 \text{ MHz}$ | | 882.51 | | pF |
| Output Capacitance | C_{oss} | | | 145.54 | | |
| Reverse Transfer Capacitance | C_{rss} | | | 97.26 | | |
| Source-Drain Diode | | | | | | |
| Max. Diode Forward Current | I_s | | | | -2.4 | A |
| Diode Forward Voltage | V_{SD} | $I_s = -1.6A, V_{GS} = 0V$ | | -0.8 | -1.2 | V |

Note: Pulse test: pulse width <= 300us, duty cycle <= 2%

