High Efficiency Power Supply for Small Size Display

Features

- **Two Outputs:**
  -±5V (APW7252A)
  -±5.2V (APW7252B)
- **Wide Input Voltage from 2.5V to 5.5V**
- **>82% Efficiency with 12mA Load Between OUTP and OUTN**
- **Fully Integrated MOSFETs for Synchronous Rectification**
- **Integrated Compensation and Feedback Circuits**
- **I²C Adjustable Output Voltages**
- **1uA Shutdown Supply Current**
- **Programmable Active Discharge**
- **WLCSP1.92x1.28-15 Package**
- **Lead Free Green Devices Available (RoHS Compliant)**

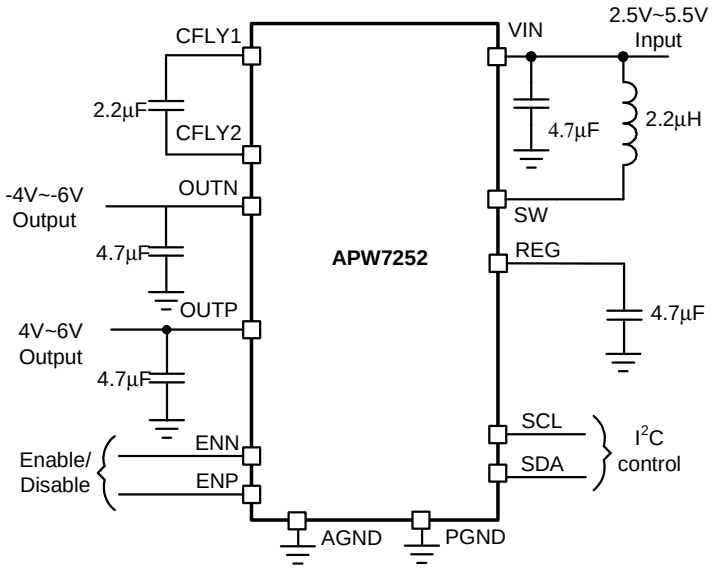
General Description

The APW7252 is boost architecture IC and the major providing to positive and negative voltage output driven. The APW7252 is synchronize boost IC and also synchronize charge pump output driven. The APW7252 has simply circuit application, only providing input supply¡Boutput supply ¡Bpositive voltage and negative voltage capacitor. That¡¦s advantage cost, cheap and simple scheme. The APW7252 is available in WLCSP 1.92x1.28-15 ball Packages.

Applications

- **Smart Phone**
- **Portable Device**

Simplified Application Circuit

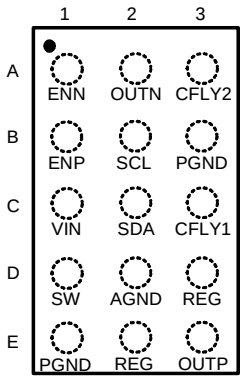


Ordering and Marking Information

APW7252 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code HA : WLCSP 1.92x1.28-15 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7252A HA : **W52A** / **X**	X - Date Code
APW7252B HA : **W52B** / **X**	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the leadfree requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

Pin Configuration



(TOP View)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{REG}, V_{CFLY1} V_{OUTP}	REG, CFLY1, OUTP to GND Voltage	-0.3 ~ 7	V
V_{OUTN}, V_{CFLY2}	OUTN to GND Voltage	+0.3 ~ -7	V
V_{VIN}, V_{SCL}, V_{SDA}, V_{ENN}, V_{ENP}	VIN, SCL, SDA/FAULT, ENN, ENP to GND Voltage	-0.3 ~ 7	V
V_{SW}	SW to GND Voltage	-0.3 ~ V_{REG}+0.3	V
	Human Body Model	2	kV
	Charged Device Model	500	V
	Latch Up	100	mA
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	260	°C

Note1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	76.5	°C/W
θ_{JC}	Junction-to-Case (top) Resistance in free air	0.2	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{VIN}	VIN to GND Voltage	2.5 ~ 5.5	V
V_{SDA}, V_{ENN}, V_{ENP}	VIN, SCL, SDA, ENN, ENP to GND Voltage	0 ~ 5.5	V
I_{OUT}	Output Current between OUTP and OUTN	0~40	mA
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

V_{VIN} = 3.7V, ENN = ENP = V_{VIN}, V_{OUTP} = 5.2V, V_{OUTN} = -5.2 V, T_A = -40°C to 85°C; typical values are at T_A = 25°C, Unless otherwise noted.

Symbol	Parameter	Test Conditions	APW7252			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{VIN}	VIN Supply Current	V_{ENP}=V_{ENN}=3.7V	–	540	-	μA
I_{VIN_SD}	VIN Supply Current in Shutdown	V_{ENP}=V_{ENN}=0V	–	1	3	μA
UNDER-VOLTAGE LOCKOUT						
V_{UVLO_R}	VIN UVLO Rising Threshold Voltage	V_{VIN} rising, T_A= -40 ~ 85 °C (Note4)	2.3	2.4	2.5	V
V_{UVLO_F}	VIN UVLO Falling Threshold Voltage	V_{VIN} rising, T_A= -40 ~ 85 °C (Note4)	2.1	2.2	2.3	V
V_{UVLO_HYS}	VIN UVLO Threshold Hyeteresis		–	0.2	–	V
BOOST REGULATOR						
V_{REG}	REG Output Voltage	Register VREG_SET = 0x00, no load	-	4	-	V
	REG Programmable Range		4	-	6.2	V
	REG Output Voltage Accuracy		-3	-	3	%
I_{BST_ILIM}	Boost nFET Current Limit	V_{VIN} = 3.7 V, L=2.2uH, T_A = 25°C	0.6	-	-	A
$R_{ON\_BST\_L}$	Boost Low Side Switch On-resistance	T_A=25℃, I=100mA,	-	300	-	mΩ
$R_{ON\_BST\_H}$	Boost High Side Switch On-resistance	T_A=25℃, I=100mA,	-	500	-	mΩ
I_{LXP_LEAK}	SW Leakage Current	V_{SW}=6V, V_{ENP}=V_{ENN}=0V	-	-	10	μA
D_{MAX}	SW Maximum Duty		-	91	-	%
F_{SW_BST}	Boost Switching Frequency		1.35	1.8	2.25	MHz
T_{SS_BST}	Boost Soft start Time	T_A=25℃, C_{VBST}=10μF	-	600	-	μs
NEGATIVE REGULATOR (OUTN)						
V_{OUTN}	OUTN Output Voltage	Register VOUTN_SET=0x00, no load	-	-4	-	V
	OUTN Programmable Range		-4	-	-6	V
	OUTN Output Voltage Accuracy		-1	-	1	%
F_{SW_OUTN}	Charge Pump Switching Frequency		-	900	-	kHz
	Load Regulation	ΔI_{OUT}=40mA	-	15	-	%/A
I_{CFLY1_LEAK}	CFLY1 Pin Leakage Current	V_{CFLY1}=6V, V_{ENN}=0V	-	-	10	μA
I_{CFLY2_LEAK}	CFLY2 Pin Leakage Current	V_{CFLY2}=-6V, V_{ENN}=0V	-10	-	-	μA
R_{ON_CFLY1}	CFLY1 to GND On Resistance	I=100mA	-	0.35	-	Ω
R_{ON_CFLY2}	CFLY2 to GND On Resistance	I=-100mA, PMOSFET	-	0.75	-	Ω

Electrical Characteristics (Cont.)

V_{VIN} = 3.7V, ENN = ENP = V_{VIN}, V_{OUTP} = 5.2V, V_{OUTN} = -5.2 V, T_A = -40°C to 85°C; typical values are at T_A = 25°C, Unless otherwise noted.

Symbol	Parameter	Test Conditions		APW7252			Unit
				Min	Typ	Max	
$R_{ON\_REG\_CFLY1}$	REG to CFLY1 On Resistance	I=100mA		-	0.65	-	Ω
$R_{ON\_OUTN\_CFLY2}$	OUTN to CFLY2 On Resistance	I=-100mA		-	0.55	-	Ω
R_{DIS_OUTN}	OUTN Discharge Resistance	V_{OUTN}=-1V		-	100	-	Ω
T_{SS_OUTN}	OUTN Softstart Time	T_A=25℃		-	0.6	-	ms
	Load Transient V_{OUTN} Peak-to-Peak Voltage	V_{VIN}=3.7V, V_{REG} =5.4V, V_{OUTP} =5.2V, V_{OUTN} =-5.2V, C_{VREG}=4.7uF, C_{OUTP} =4.7uF, C_{OUTN}=4.7uF, L=2.2uH, C_{FLY}=2.2uF, T_A=25℃	I_{OUT}(VP to VN)=0mA-40mA-0mA, Tr=100ns, Tf=400ns	-	-	3.5	%
			I_{OUT}(VP to VN)=12mA-40mA-12mA, Tr=100ns, Tf=400ns	-	-	3.5	%
	Line Transient V_{OUTN} Peak-to-Peak Voltage	V_{VIN}=2.8V to 4.5V to 2.8V, Tr=Tf=24us, V_{REG} =5.4V, V_{OUTP} =5.2V, V_{OUTN} =-5.2V, C_{VREG}=4.7uF, C_{OUTP} =4.7uF, C_{OUTN}=4.7uF, L=2.2uH, C_{FLY}=2.2uF, T_A=25℃	no load	-	-	0.85	%/V
			I_{OUT} (VP to VN)=5mA	-	-	1.25	%/V
			I_{OUT} (VP to VN)=35mA	-	-	2.5	%/V
POSITIVE REGULATOR (OUTP)							
V_{OUTP}	OUTP Output Voltage	Register VOUTP_SET=0x00, no load		-	4	-	V
	OUTP Programmable Range			4	-	6	V
	OUTP Output Voltage Accuracy			-1	-	1	%
V_{DRP_OUTP}	OUTP Dropout Voltage	V_{LOAD_OUTP}=100mA		-	-	150	mV
	Load Regulation	ΔI_{OUT}=80mA		-	3.4	-	%/A
R_{DIS_OUTP}	OUTP Discharge Resistance	V_{OUTP}=1V		-	100	-	Ω
T_{SS_OUTP}	OUTP Softstart Time	T_A=25℃		-	0.6	-	ms
	Load Transient V_{OUTP} Peak-to-Peak Voltage	V_{VIN}=3.7V, V_{REG} =5.4V, V_{OUTP} =5.2V, V_{OUTN} =-5.2V, C_{VREG}=4.7uF, C_{OUTP} =4.7uF, C_{OUTN}=4.7uF, L=2.2uH, C_{FLY}=2.2uF, T_A=25℃	I_{OUT}(VP to VN)=0mA-40mA-0mA, Tr=100ns, Tf=400ns	-	-	2	%
			I_{OUT}(VP to VN)=12mA-40mA-12mA, Tr=100ns, Tf=400ns	-	-	2	%

Electrical Characteristics (Cont.)

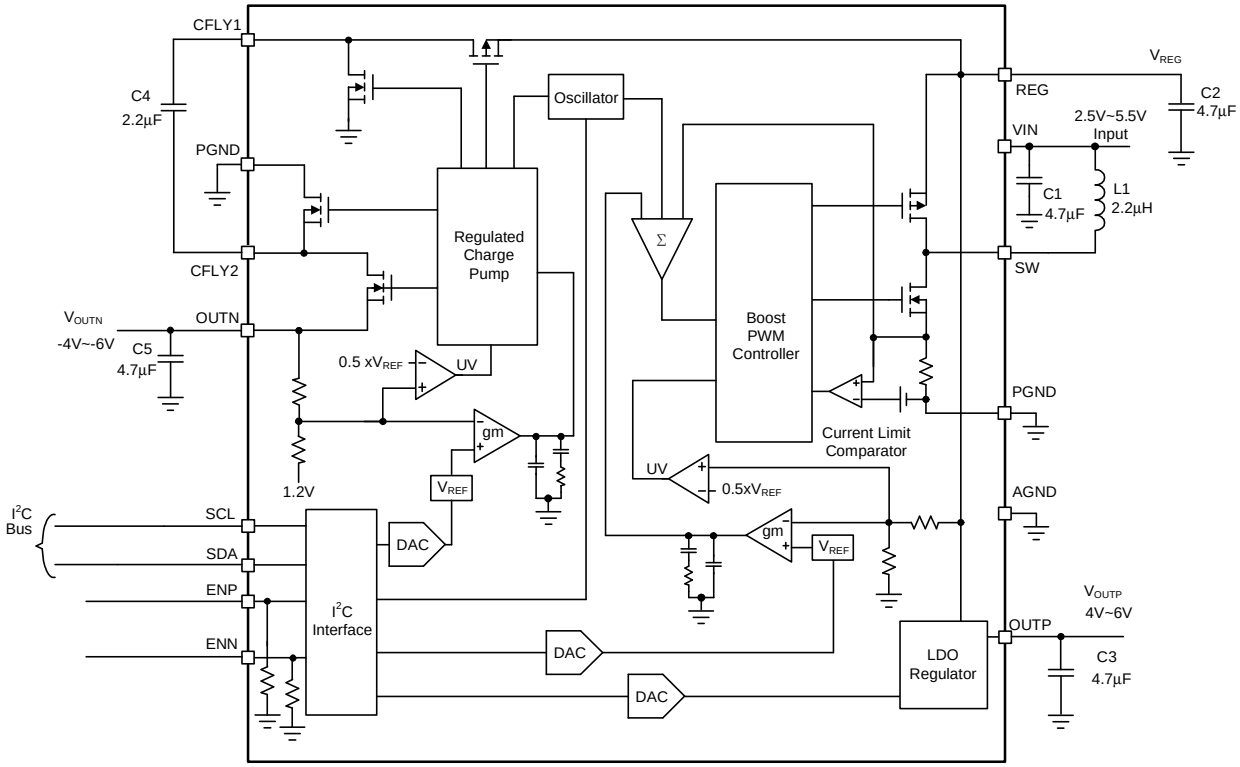
V_{VIN} = 3.7V, ENN = ENP = V_{VIN}, VOUTP = 5.4V, V_{OUTN} = -5.4 V, T_A = -40°C to 85°C; typical values are at T_A = 25°C, Unless otherwise noted.

Symbol	Parameter	Test Conditions		APW7252			Unit
				Min	Typ	Max	
	Line Transient V_{OUTP} Peak-to-Peak Voltage	V_{VIN}=2.8V to 4.5V to 2.8V, Tr=Tf=24us, V_{REG} =5.4V, V_{OUTP} =5.2V, V_{OUTN} =-5.2V, C_{VREG}=4.7uF, C_{OUTP} =4.7uF, C_{OUTN}=4.7uF, L=2.2uH, C_{FLY}=2.2uF, T_A=25℃	no load	-	-	0.85	%/V
			I_{OUT}=5mA	-	-	1	%/V
			I_{OUT}=35mA	-	-	1.3	%/V
	Thermal Shutdown			-	160	-	℃
	Thermal Shutdown Hysteresis			-	10	-	℃
	REG Under-voltage Threshold			-	0.5*V_{REG}	-	V
	OUTP Under-voltage Threshold			-	0.5*V_{OUTP}	-	V
	OUTN Under-voltage Threshold			-	0.5*V_{OUTN}	-	V
LOGIC/DIGITAL							
V_{IL}	Logic Input Low Voltage	ENN, ENP ,SCL, SDA		-	-	0.54	V
V_{IH}	Logic Input High Voltage	ENN, ENP ,SCL, SDA		1.1	-	-	V
	Input Logic High Threshold			0.8	-	1	V
	Input Logic High Threshold Hysteresis					200	mV
	Internal Pull-down Resistance	ENN, ENP		-	200	-	kΩ
	I^2C SCL Clock Frequency			-	-	400	kHz
SMBus Control							
	SMBDAT and SMBCLK Logic	High Logic		1.1	-	-	V
		Low Logic		-	-	0.54	V
	SMBDAT and SMBCLK Leakage Current			-	0.01	1	uA
F_{SMB}	SMBus Operating Frequency			10	-	100	KHz
T_{BUF}	Bus free time between stop and start condition			4.7	-	-	us
T_{HD_STA}	Hold time after start condition	After this period, the first clock is generated		4	-	-	us
T_{SD_STA}	Repeated start condition setup time			4.7	-	-	us
T_{SD_STO}	Stop condition setup time			4	-	-	us
T_{HD_DAT}	Data hold time			300	-	-	ns
T_{SU_DAT}	Data setup time			250	-	-	ns
$T_{TIMEOUT}$	Detect clock low timeout			25	-	35	ms
T_{LOW}	Clock low period			4.7	-	-	us
T_{HIGH}	Clock high period			4	-	50	us
T_{LOW_SEXT}	Slave device cumulative clock low extend time_slave			-	-	25	ms
T_{LOW_MEXT}	Master device cumulative clock low extend time_master			-	-	10	ms
T_{F_SMB}	Fall time of SMB DAT/CLK			-	-	300	ns
T_{R_SMB}	Rise time of SMB DAT/CLK			-	-	1000	ns
T_{SMB_POR}	Power on reset of SMB	Time in which a device must be operation after power on reset		-	3	500	ms

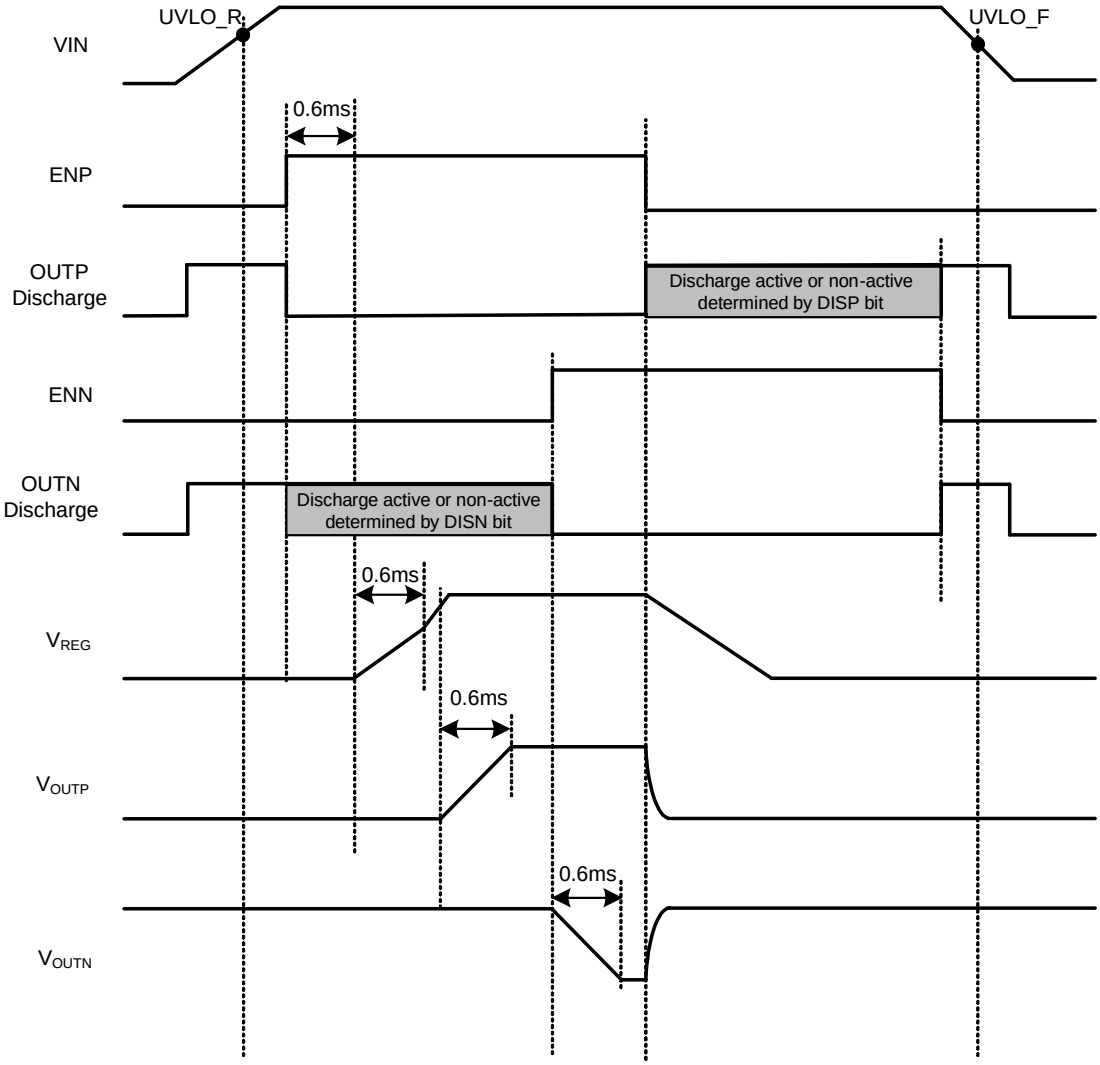
Pin Description

PIN		Function
NO.	NAME	
A1	ENN	VN Enable Input. Note, this pin has 200kΩ (typ.) pull-down to AGND.
A2	OUTN	Negative Charge Pump Output. Connect a 4.7µF capacitor to ground. Connecting two 4.7µF capacitors to ground will lower the negative charge pump output voltage ripple.
A3	CFLY2	Charge Pump Negative Connection. Place a capacitor between CFLY1 and CFLY2 to generate the OUTN voltage.
B1	ENP	REG and OUTP Enable Input. Note, this pin has 200kΩ (typ.) pull-down to AGND.
B2	SCL	Serial Clock Connection for I^2C Interface.
B3, E1	PGND	Power ground.
C1	VIN	Input Supply. Connect a 4.7µF to ground.
C2	SDA	Serial Data Connection for I^2C Interface.
C3	CFLY1	Charge Pump Positive Connection. Place a capacitor between CFLY1 and CFLY2 to create the OUTN voltage.
D1	SW	Switch node for boost converter. Connect an inductor between the VIN and SW pins for boost converter operation.
D2	AGND	Analog ground.
D3,E2	REG	Boost Converter Output. The boost converter output supplies the power to the negative charge pump and LDO. Connect a 4.7µF capacitor to ground.
E3	OUTP	LDO Output. Connect a 4.7µF capacitor to ground.

Block Diagram and Typical Application Circuit

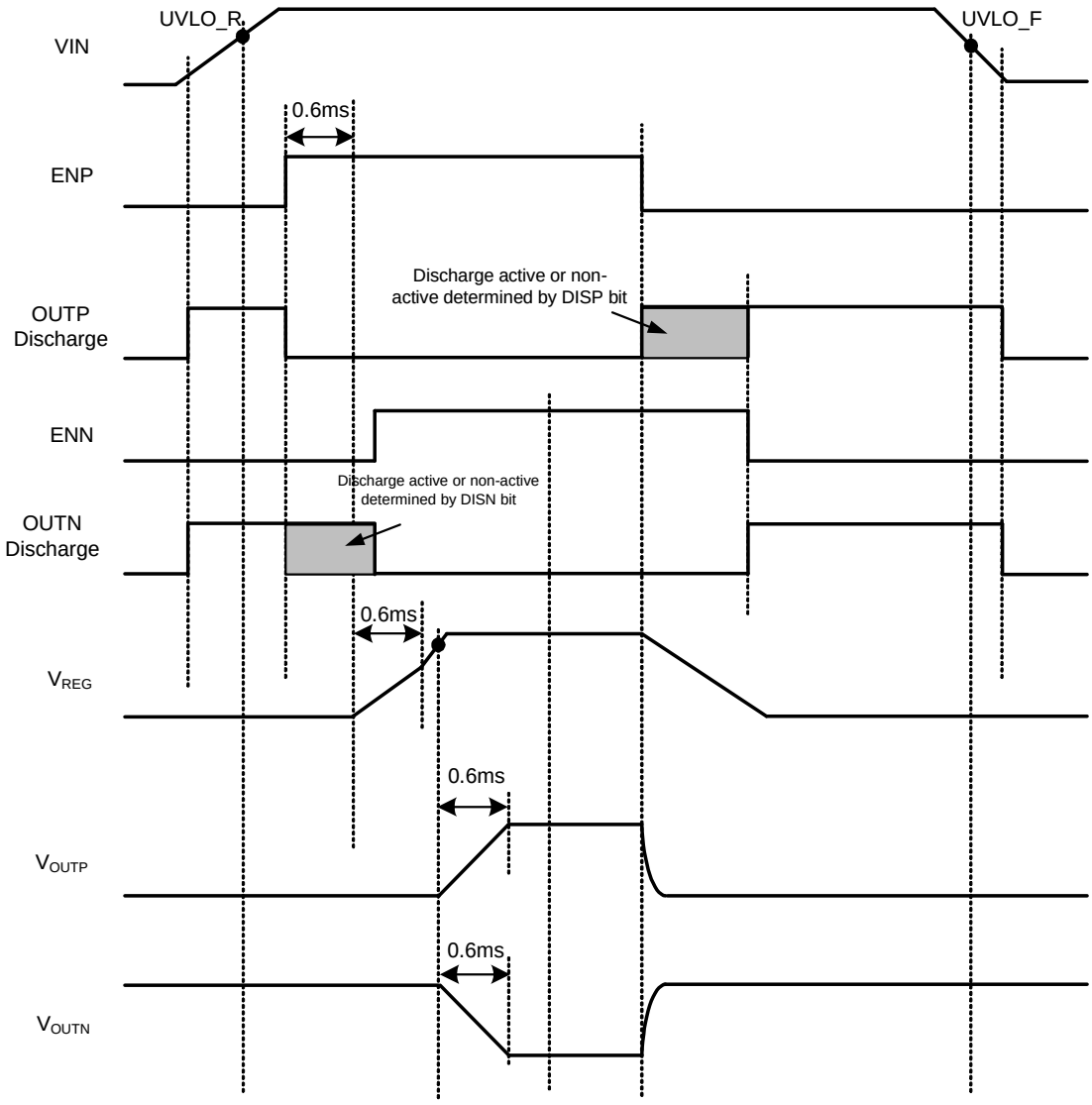


Power On / Off Sequence



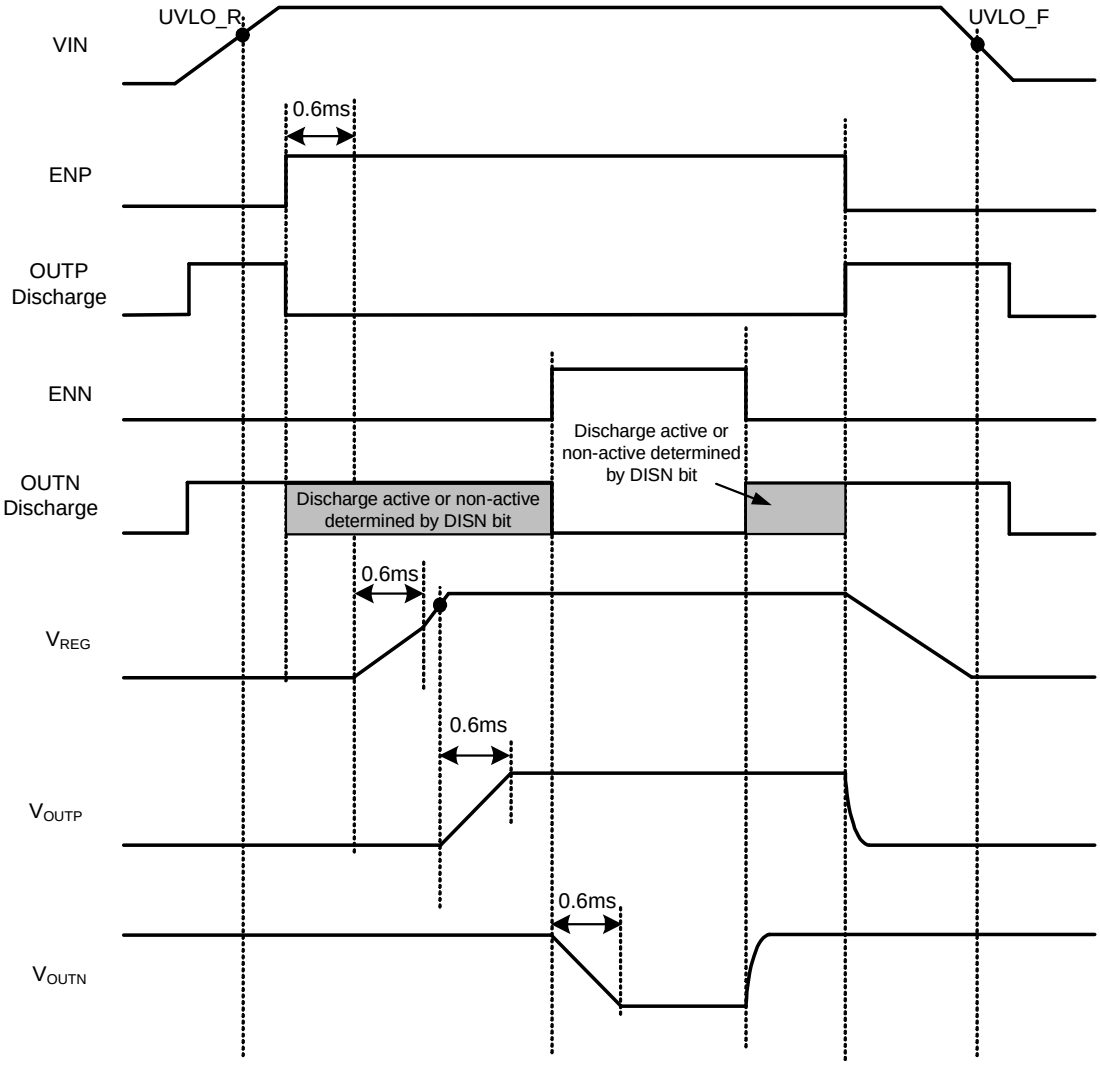
Power On-ENN rising after V_{REG} softstart finished

Power On/Off Sequence (Cont.)



Power On-ENN rising before V_{REG} softstart finished

Power On/Off Sequence (Cont.)



Power Off-ENN falling before ENP falling

I²C Control

7-bit hard coded device address:

b7	b6	b5	b4	b3	b2	b1	b0
0	1	1	1	1	1	0	R/W

Read=1
Write=0

Write 1 byte

(Command byte is sent after the address and detemines which register receives the data that follows the command byte.)

Slave Address							$R/\overline{W}$		Register Address		Register Data		
S	0	1	1	1	1	1	0	0	A	Command Byte	A	Data Byte	A	P

Read 1 byte

(Command byte is sent after the address and detemines which register is accessed. After a start, the Device address is sent again and LSB is set to logic 1. Data defined by command byte then is sent by APW7252.)

Slave Address							$R/\overline{W}$		Register Address			Slave Address		$R/\overline{W}$		Register Data 1		
S	0	1	1	1	1	1	0	0	A	Command Byte	A	S			1	A	Data Byte 1	$\overline{A}$	P

Timing Diagram

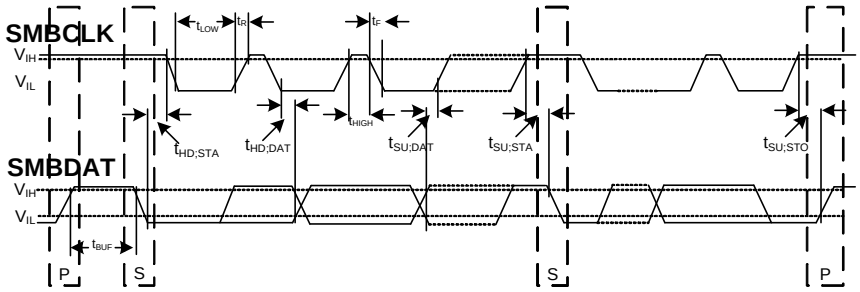


Figure 1: SMBus Common AC Specification

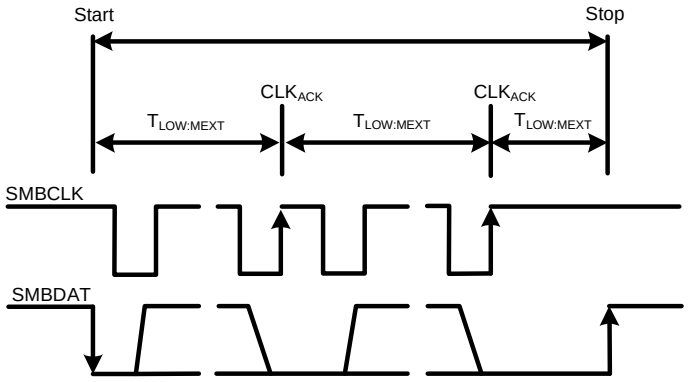


Figure 2: Timing Diagram of SMBus Timeout

Register Map

Table 1: Register Map

Slave Address : 0111110							
Address	Bit	Name	Default Value	Description	Resolution	Range	R/W
00h	[4:0]	VOUTP_SET	0x0	VOUTP Voltage adjustment	100mV	4V ~ 6V	R/W
01h	[4:0]	VOUTN_SET	0x0	VOUTN Voltage adjustment	100mV	-4V ~ -6V	R/W
02h	[4:0]	VREG_SET	0x0	VREG Voltage adjustment	100mV	4V ~ 6.2V	R/W
03h	[1:0]	Discharge Control	0x03	VOUTP/VOUTN Discharge Resistance Enable/Disable	-	-	R/W
04h	[4:0]	Vendor ID	0x00	Vendor ID Code	-	-	R

Register Definition

Register 00:VOUTP_SET

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit name	Reserved	Reserved	Reserved	VOUTP_SET[4:0]				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Name	Bit Definition							

VOUTP_SET[4:0]

VOUTP Voltage adjustment:

00000:	4V	01011:	5.1V
00001:	4.1V	01100:	5.2V (Default:7252B)
00010:	4.2V	01101:	5.3V
00011:	4.3V	01110:	5.4V
00100:	4.4V	01111:	5.5V
00101:	4.5V	10000:	5.6V
00110:	4.6V	10001:	5.7V
00111:	4.7V	10010:	5.8V
01000:	4.8V	10011:	5.9V
01001:	4.9V	10100:	6.0V
01010:	5.0V (Default:7252A)	10101~11111:	6.0V

Register Definition (Cont.)

Register 01:VOUTN_SET

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit name	Reserved	Reserved	Reserved	VOUTN_SET[4:0]				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Name	Bit Definition							
VOUTN_SET[4:0]	VOUTN Voltage adjustment: 00000: -4V 00001: -4.1V 00010: -4.2V 00011: -4.3V 00100: -4.4V 00101: -4.5V 00110: -4.6V 00111: -4.7V 01000: -4.8V 01001: -4.9V 01010: -5.0V (Default:7252A) 01011: -5.1V 01100: -5.2V (Default:7252B) 01101: -5.3V 01110: -5.4V 01111: -5.5V 10000: -5.6V 10001: -5.7V 10010: -5.8V 10011: -5.9V 10100: -6.0V 10101~11111: -6.0V							

Register Definition (Cont.)

Register 02:VREG_SET

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit name	Reserved	Reserved	Reserved	VREG_SET[4:0]				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Name	Bit Definition							
VREG_SET[4:0]	**VREG Voltage adjustment:** 00000: 4V 00001: 4.1V 00010: 4.2V 00011: 4.3V 00100: 4.4V 00101: 4.5V 00110: 4.6V 00111: 4.7V 01000: 4.8V 01001: 4.9V 01010: 5.0V 01011: 5.1V 01100: 5.2V (Default:7252A) 01101: 5.3V 01110: 5.4V (Default:7252B) 01111: 5.5V 10000: 5.6V 10001: 5.7V 10010: 5.8V 10011: 5.9V 10100: 6.0V 10101: 6.1V 10110: 6.2V 10111~11111: 6.2V							

Register Definition (Cont.)

Register 03: DISCHARGE_CONTROL

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DISP	DISN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Name	Bit Definition							
DISN	VOUTN Discharge Resistance Enable/Disable: 0: Disable VOUTN Discharge Resistance 1: Enable VOUTN Discharge Resistance							
DISP	VOUTP Discharge Resistance Enable/Disable: 0: Disable VOUTP Discharge Resistance 1: Enable VOUTP Discharge Resistance (Note: IF ENN and ENP are goes low then Discharge function was always turn on.)							

Register 04: VENDOR ID

Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit name	Reserved	Reserved	Reserved	VENDOR ID Code [4:0]				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Name	Bit Definition							
VENDOR ID Code [4:0]	Vendor ID Code: 00101: Default							

Function Description

Under-Voltage Lockout

An under-voltage lockout function prevents the device from operating if the input voltage on VIN is lower than approximately 2.4V. The device automatically enters the shutdown mode if the voltage on VIN drops below approximately 2.2V. This under-voltage lockout function is implemented in order to prevent the malfunctioning of the converter.

Soft-start

The APW7252 has a built-in digital soft-start to control the rise rate of the output voltage and limit the input current surge during start-up. During soft-start, the reference voltage, output from a DAC, raises up step by step to control the output voltage to rise gently.

Frequency Modulation Mode (PFM)

The APW7252's boost converter and negative charge pump will automatically enter in PFM mode operation to reduce the dominant switching losses. These controls get low quiescent current, help to maintain high efficiency over the complete load range.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7252. When the junction temperature exceeds 160°C, a thermal sensor turns off the both power MOSFET's, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulate the output voltage again after the junction temperature cools by 10°C. The OTP designed with a 10°C hysteresis lowers the average Junction Temperature (T_J) during continuous thermal overload conditions, increasing the life time of the device.

Under Voltage Protection (UVP)

The under-voltage protection circuit monitors the outputs to protect the device against short-circuit or heavy load conditions. When one of the output voltages is falls below the UVP threshold (50% of VREF), a fault signal is generated and the device turns off all outputs. The device is then latched off and will initials a soft-start process until re-cycle ENP and ENN or VIN.

Over Current Protection (OCP)

The APW7252 monitors the output current of the boost converter, flowing through the N-Channel power MOSFET, and limits the IC from damages during overload, short-circuit and over-voltage conditions.

Enable and Shutdown

Driving ENP and ENN to ground turns off the VP and VN voltage respectively. When both ENN and ENP is in logic low state, the boost converter is also enters shutdown mode and VIN quiescent supply current reduces to less than 3μA.

Discharge Resistance Enable/Disable

APW7252 Discharge resistance function always turn on condition are ENN and ENP were setting low when input voltage is high than POR. secondly, the input voltage is low than POR then that's always turn on no matter ENN and ENP were setting high or low states. The independent discharge function of V_{OUTP} and V_{OUTN} can be by DISP bit and DISN bit. If the V_{OUTP} and V_{OUTN} were normal operation then Discharge resistance function was disabling.

Function Description

Input Voltage Capacitor Selection

The APW7252 is boost architecture application of power IC. The major boost architecture is providing to positive and negative voltage output driving capable. The ceramic capacitors are recommended for input capacitor applications. Low ESR will effectively reduce the input voltage ripple caused by switching operation. The 4.7uF capacitors are sufficient for most applications. The input capacitor selection was suggestion X5R or X7R type.

Output Voltage (Boost converter) Capacitor Selection

For the boost converter output voltage capacitor suggests choose low ESR filter ceramic capacitor. A minimum ceramic of 4.7uF or high than value capacitor has advantages response for load transient and ripple. The output capacitor selection was suggestion X5R or X7R type.

Output Voltage (Positive) Capacitor Selection

The positive voltage is LDO architecture. The input capacitor use Low ESR ceramic capacitor, a minimum of 4.7uF or more than 4.7uF capacitor. The output capacitor selection was suggestion X5R or X7R type.

Output Voltage (negative) Capacitor Selection

The negative voltage is charge pump architecture. The input capacitor use Low ESR ceramic capacitor, a minimum of 4.7uF or more than 4.7uF capacitor. The output capacitor selection was suggestion X5R or X7R type. This capacitor chooses to will impact the negative output voltage accuracy and load regulation.

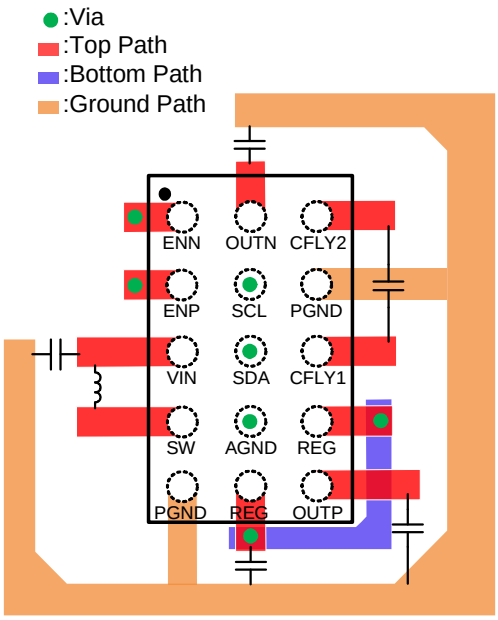
Flying Capacitor Selection

The negative voltage is charge pump architecture, its must need to connect an external capacitor. The flying capacitor suggestion use 2.2uF ceramic capacitor. The flying capacitor selection was suggestion X5R or X7R type.

Layout Suggestion

The fig.3 is Layout suggestion. A few notes can be let APW7252 has high performance. Please refer as below notes for your modify PCB layout.

1. Input, output, flying, positive and negative capacitors can be closed to the IC terminal as far as possible.
2. REG pin have 2 pins must to connected together.
3. The SW pin node trace is short as far as possible.
4. The Ground path keeps to the one plane area.
5. PGND must be shorted together with AGND on the same ground plane.

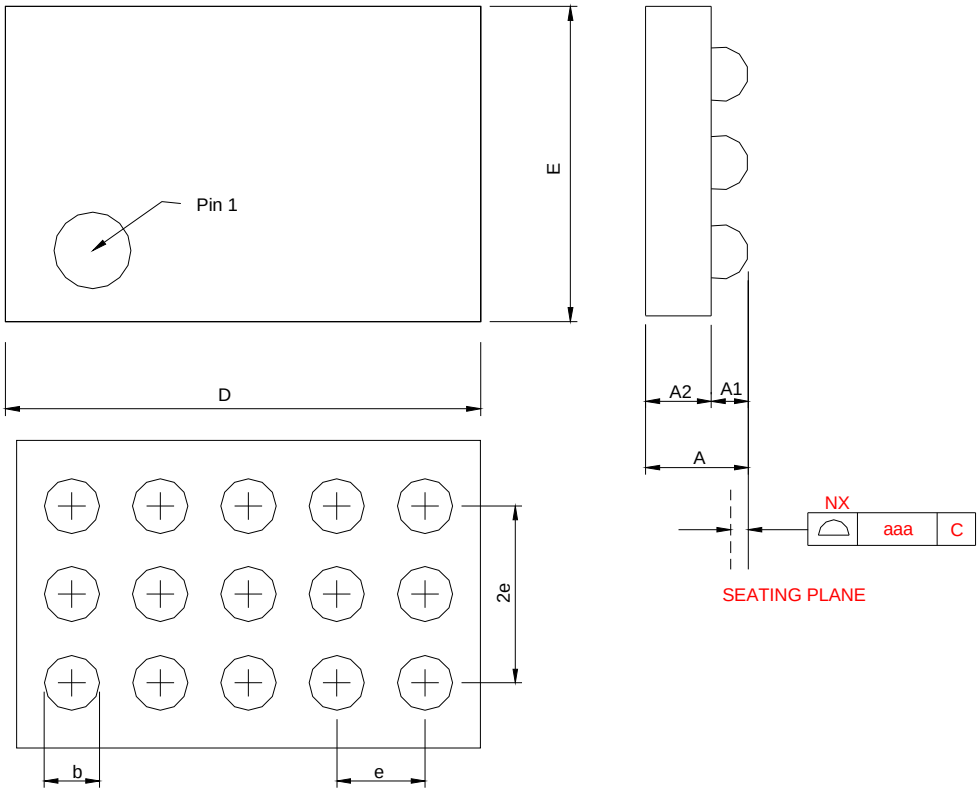


(TOP View)

Figure.3 Layout Suggestion

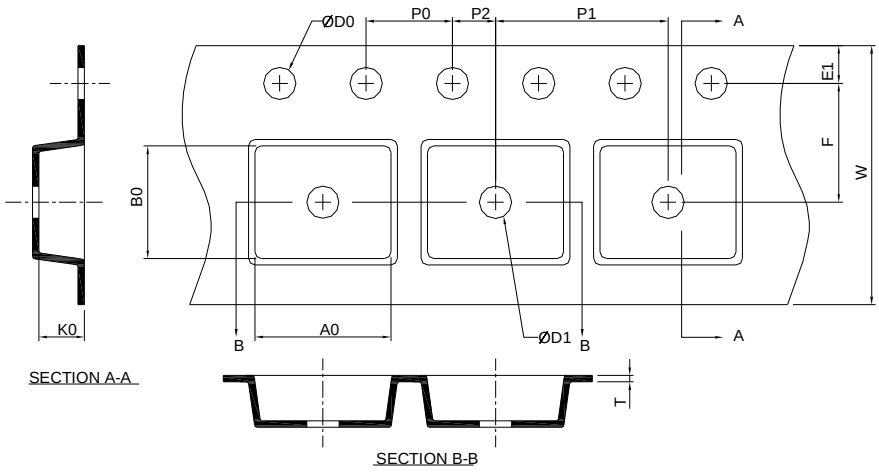
Package Information

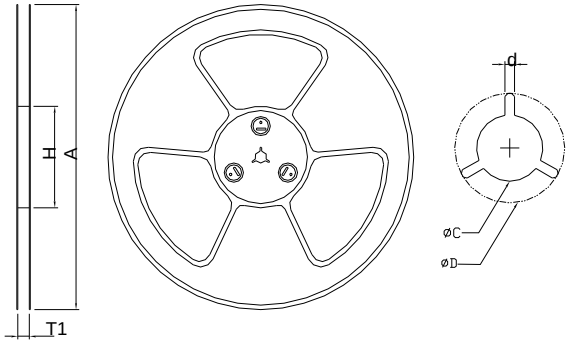
WLCSP1.28x1.92-15



SYMBOL	WLCSP1.28*1.92-15			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		0.62		0.024
A1	0.12	0.20	0.005	0.008
A2	0.35	0.42	0.014	0.017
b	0.20	0.30	0.008	0.012
D	1.92	1.98	0.076	0.078
E	1.28	1.34	0.050	0.053
e	0.40 BSC		0.016 BSC	
aaa	0.05		0.002	

Carrier Tape & Reel Dimensions





Application	A	H	T1	C	d	D	W	E1	F
WLCSP(1.9X2.1)	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	0.5 MIN.	0.25±0.02	1.55±0.05	2.05±0.05	0.70±0.05

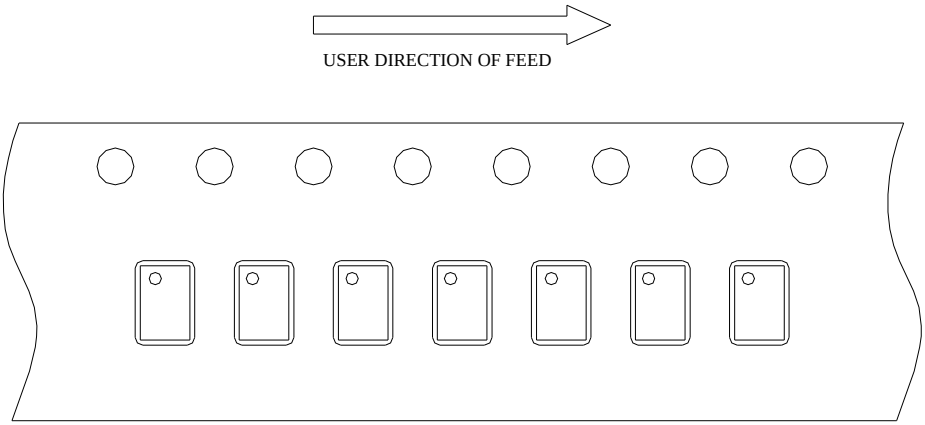
(mm)

Devices Per Unit

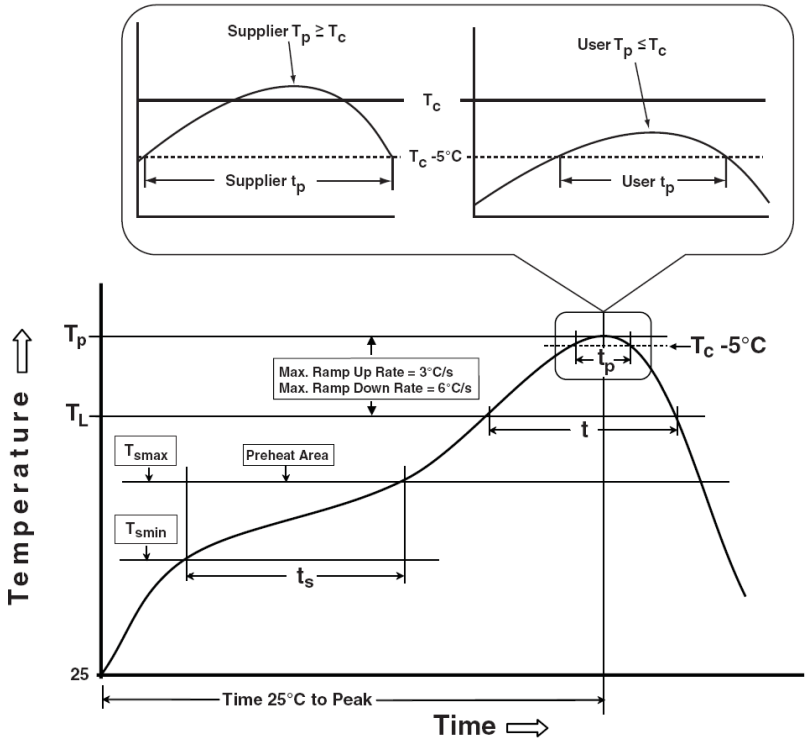
Package Type	Unit	Quantity
WLCSP(1.28x1.92)	Tape & Reel	3000

Taping Direction Information

WLCSP1.28x1.92-15



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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