

N-channel 800 V, 1.50 Ω typ., 4 A MDmesh™ K5 Power MOSFET in a DPAK package

Datasheet - production data

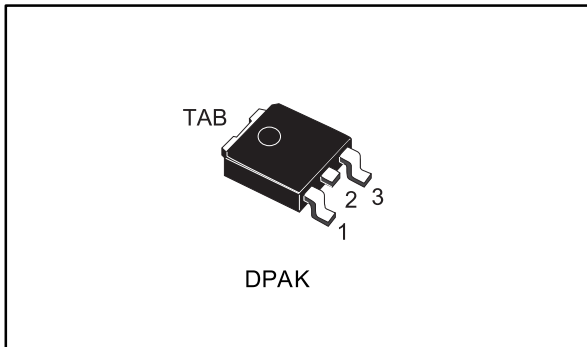
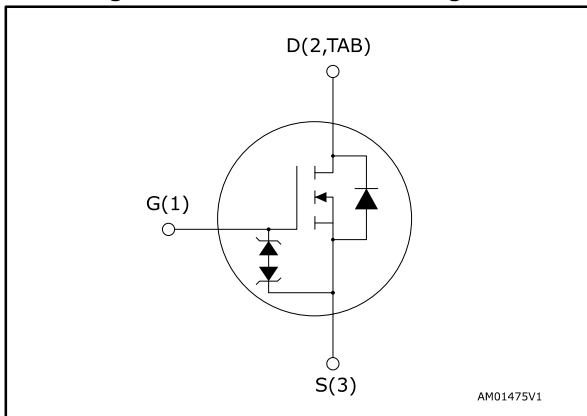


Figure 1: Internal schematic diagram



Features

| Order code | V _{DS} | R _{DS(on)} max. | I _D |
|------------|-----------------|--------------------------|----------------|
| STD5N80K5 | 800 V | 1.75 Ω | 4 A |

- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

| Order code | Marking | Package | Packing |
|------------|---------|---------|---------------|
| STD5N80K5 | 5N80K5 | DPAK | Tape and reel |

Contents

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1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---------------|---|-------------|------------------|
| V_{GS} | Gate-source voltage | ± 30 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 4 | A |
| I_D | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 2.3 | A |
| $I_D^{(1)}$ | Drain current (pulsed) | 16 | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 60 | W |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 4.5 | V/ns |
| $dv/dt^{(3)}$ | MOSFET dv/dt ruggedness | 50 | |
| T_j | Operating junction temperature range | - 55 to 150 | $^\circ\text{C}$ |
| T_{stg} | Storage temperature range | | |

Notes:

(1)Pulse width limited by safe operating area

(2) $I_{SD} \leq 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 640\text{ V}$

(3) $V_{DS} \leq 640\text{ V}$

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|----------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 2.08 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb | 50 | $^\circ\text{C}/\text{W}$ |

Notes:

(1)When mounted on FR-4 board of 1 inch², 2 oz Cu

Table 4: Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax}) | 1.2 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 165 | mJ |

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 5: On/off-state

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|--|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$ | 800 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$ $T_C = 125\text{ °C}^{(1)}$ | | | 50 | μA |
| I_{GSS} | Gate body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DD} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$ | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 2\text{ A}$ | | 1.50 | 1.75 | Ω |

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|---------------------------------------|---|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 177 | - | pF |
| C_{oss} | Output capacitance | | - | 15 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 0.3 | - | pF |
| $C_{o(tr)}^{(1)}$ | Equivalent capacitance time related | $V_{GS} = 0$, $V_{DS} = 0\text{ to }640\text{ V}$ | - | 33 | - | pF |
| $C_{o(er)}^{(2)}$ | Equivalent capacitance energy related | | | | 12 | |
| R_g | Intrinsic gate resistance | $f = 1\text{ MHz}$, $I_D = 0\text{ A}$ | - | 16 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 640\text{ V}$, $I_D = 4\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 15: "Test circuit for gate charge behavior") | - | 5 | - | nC |
| Q_{gs} | Gate-source charge | | - | 1.7 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 2.9 | - | nC |

Notes:

⁽¹⁾ $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁽²⁾ $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 7: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 400\text{ V}$, $I_D = 2\text{ A}$, $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform") | - | 12.7 | - | ns |
| t_r | Rise time | | - | 11.7 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 23 | - | ns |
| t_f | Fall time | | - | 14.8 | - | ns |

Table 8: Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 4 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 16 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 4\text{ A}$, $V_{GS} = 0\text{ V}$ | - | | 1.5 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times") | - | 265 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 1.59 | | μC |
| I_{RRM} | Reverse recovery current | | - | 12 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times") | - | 386 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 2.18 | | μC |
| I_{RRM} | Reverse recovery current | | - | 11.3 | | A |

Notes:

(1)Pulse width limited by safe operating area

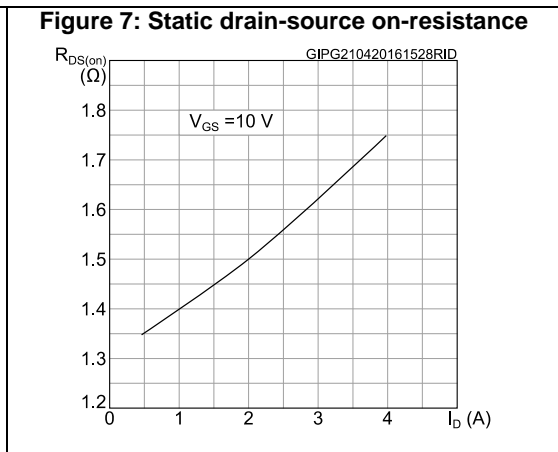
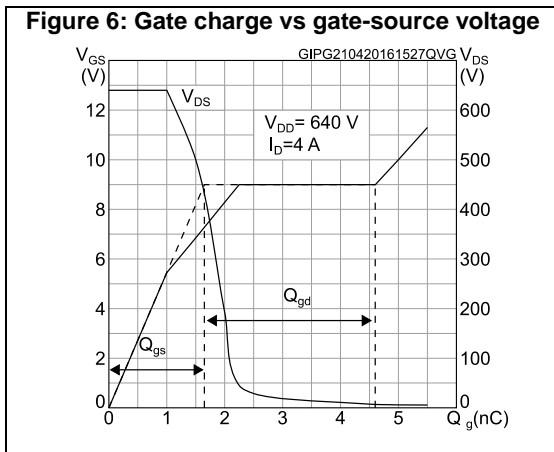
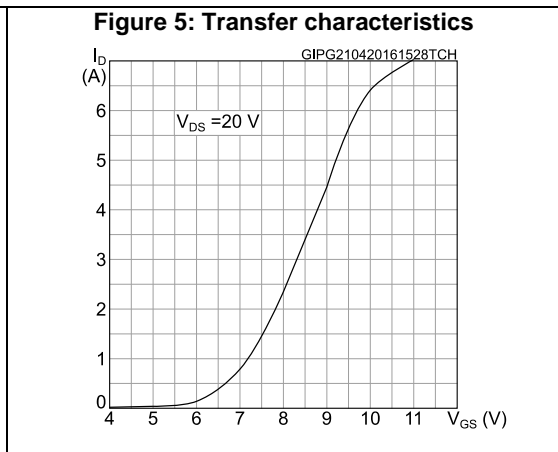
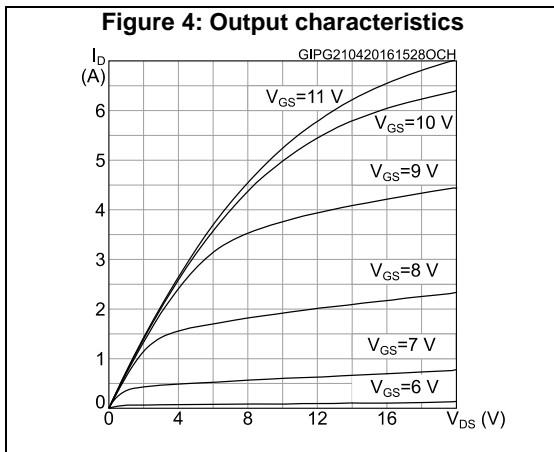
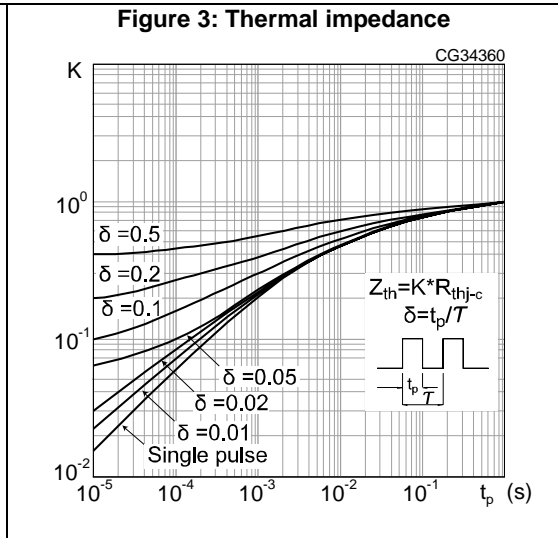
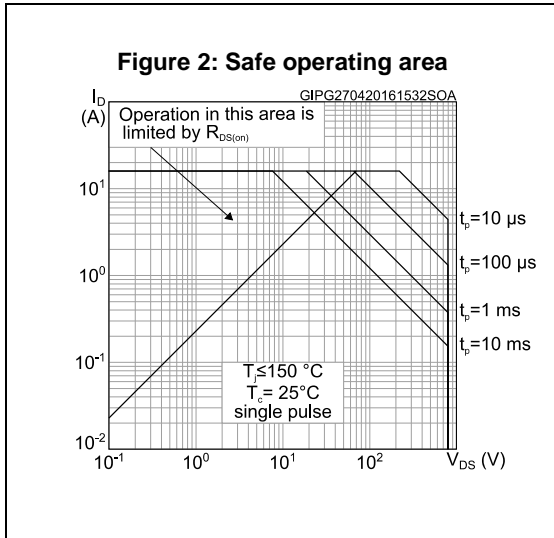
(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

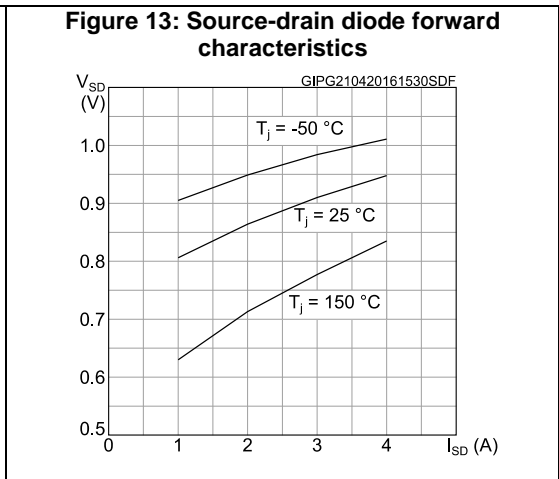
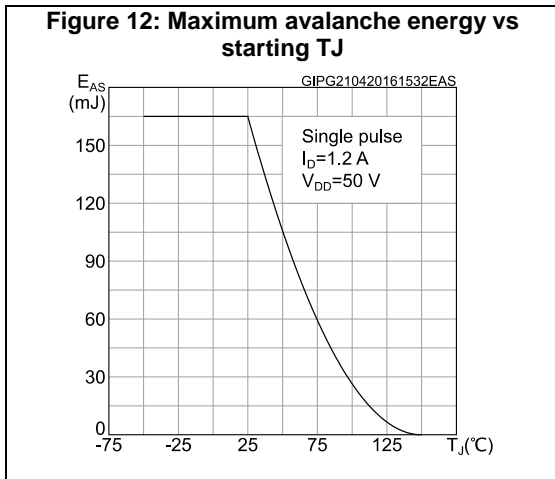
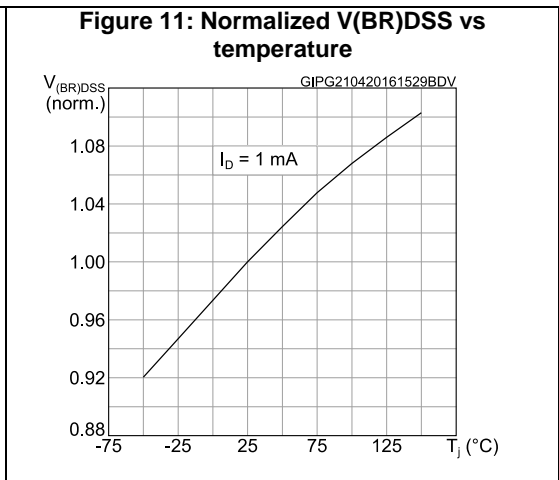
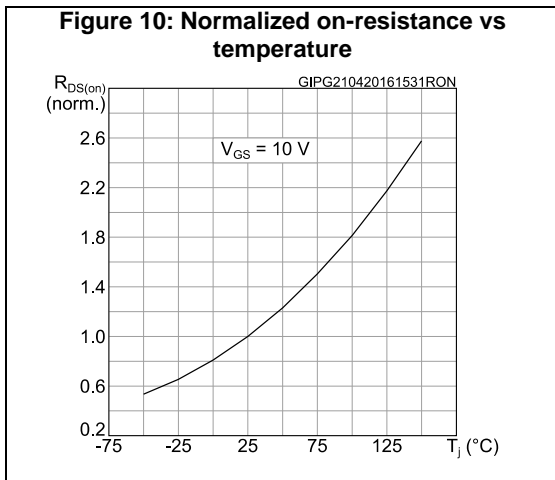
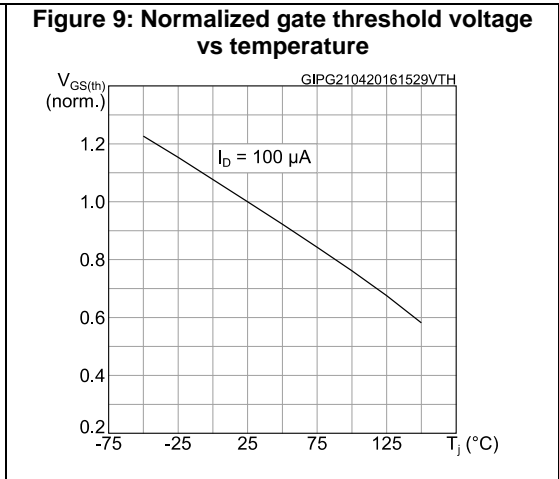
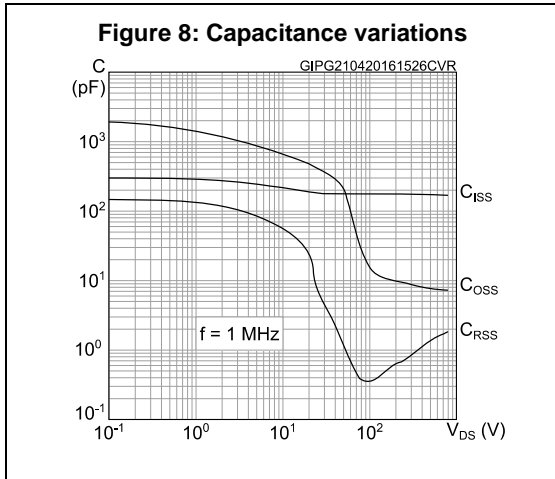
Table 9: Gate-source Zener diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------|---|------|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$ | 30 | - | - | V |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

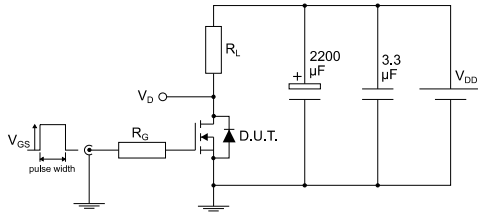
2.1 Electrical characteristics (curves)





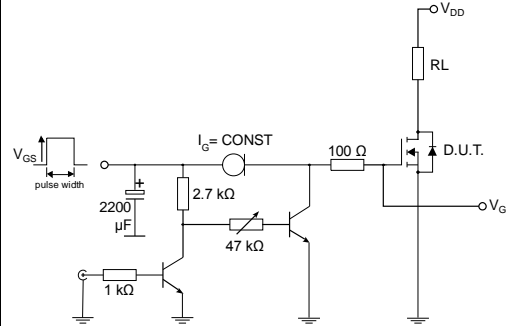
3 Test circuits

Figure 14: Test circuit for resistive load switching times



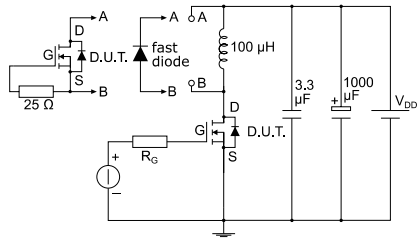
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Figure 15: Test circuit for gate charge behavior



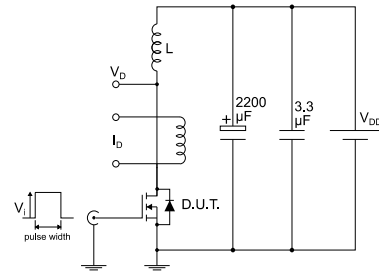
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Figure 16: Test circuit for inductive load switching and diode recovery times



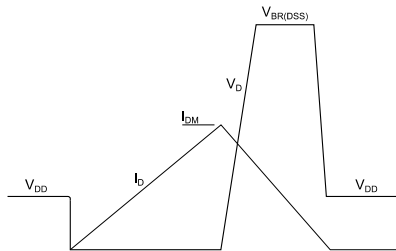
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Figure 17: Unclamped inductive load test circuit



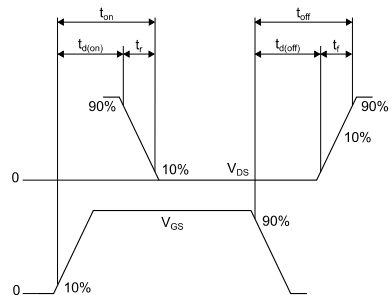
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Figure 18: Unclamped inductive waveform



AM01472v1

Figure 19: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 mechanical data

Figure 20: DPAK (TO-252) type A2 package outline

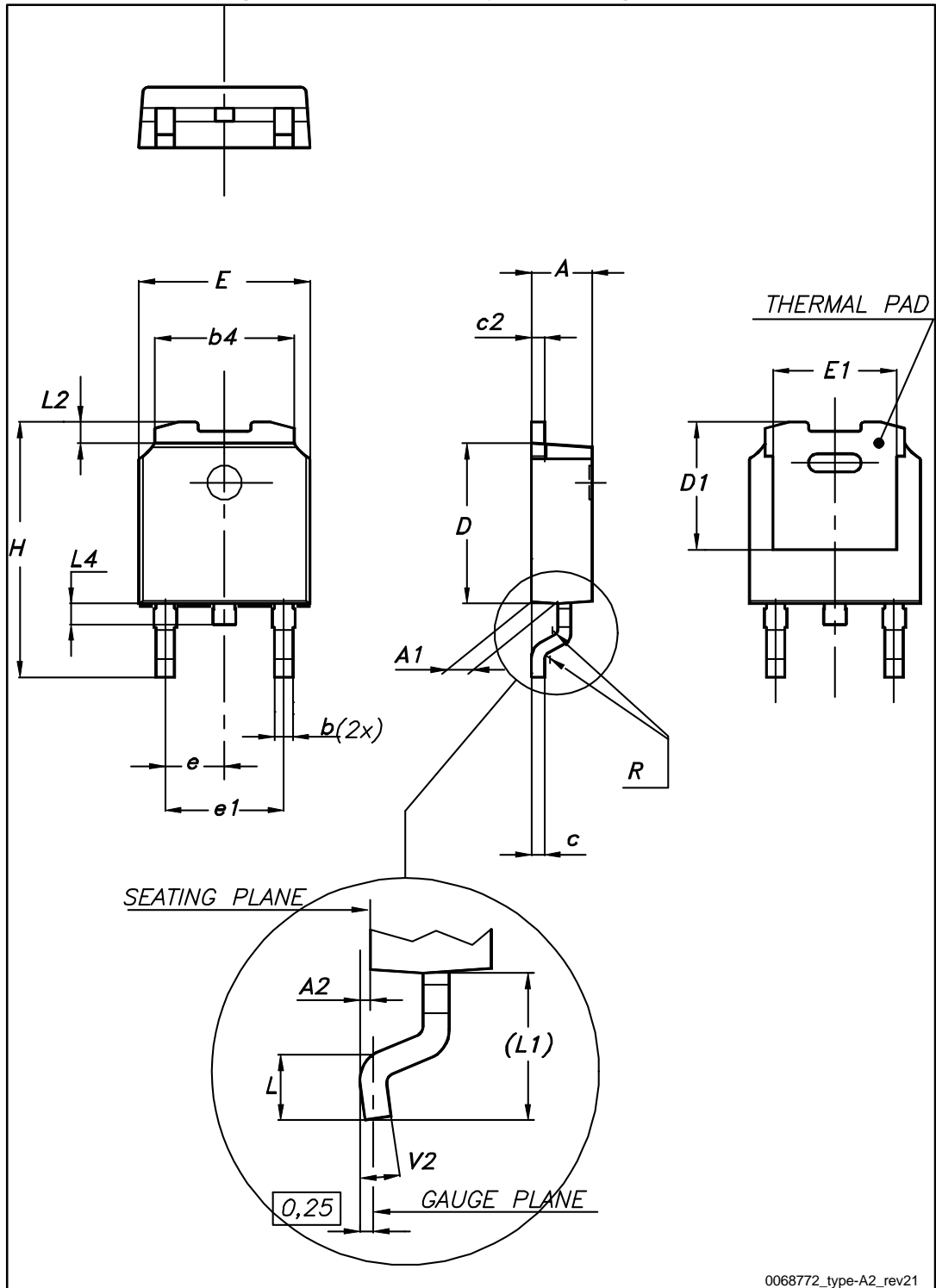
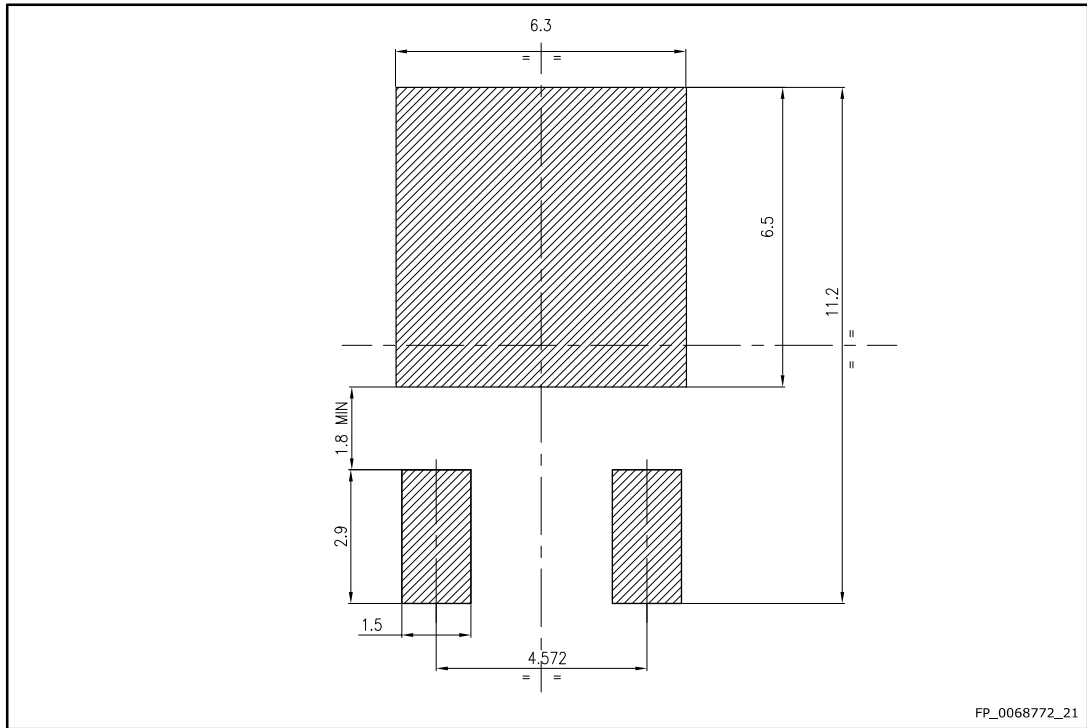


Table 10: DPAK (TO-252) type A2 mechanical data

| Dim. | mm | | |
|------|------|------|-------|
| | Min. | Typ. | Max. |
| A | 2.20 | | 2.40 |
| A1 | 0.90 | | 1.10 |
| A2 | 0.03 | | 0.23 |
| b | 0.64 | | 0.90 |
| b4 | 5.20 | | 5.40 |
| c | 0.45 | | 0.60 |
| c2 | 0.48 | | 0.60 |
| D | 6.00 | | 6.20 |
| D1 | 4.95 | 5.10 | 5.25 |
| E | 6.40 | | 6.60 |
| E1 | 5.10 | 5.20 | 5.30 |
| e | 2.16 | 2.28 | 2.40 |
| e1 | 4.40 | | 4.60 |
| H | 9.35 | | 10.10 |
| L | 1.00 | | 1.50 |
| L1 | 2.60 | 2.80 | 3.00 |
| L2 | 0.65 | 0.80 | 0.95 |
| L4 | 0.60 | | 1.00 |
| R | | 0.20 | |
| V2 | 0° | | 8° |

Figure 21: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) packing information

Figure 22: DPAK (TO-252) tape outline

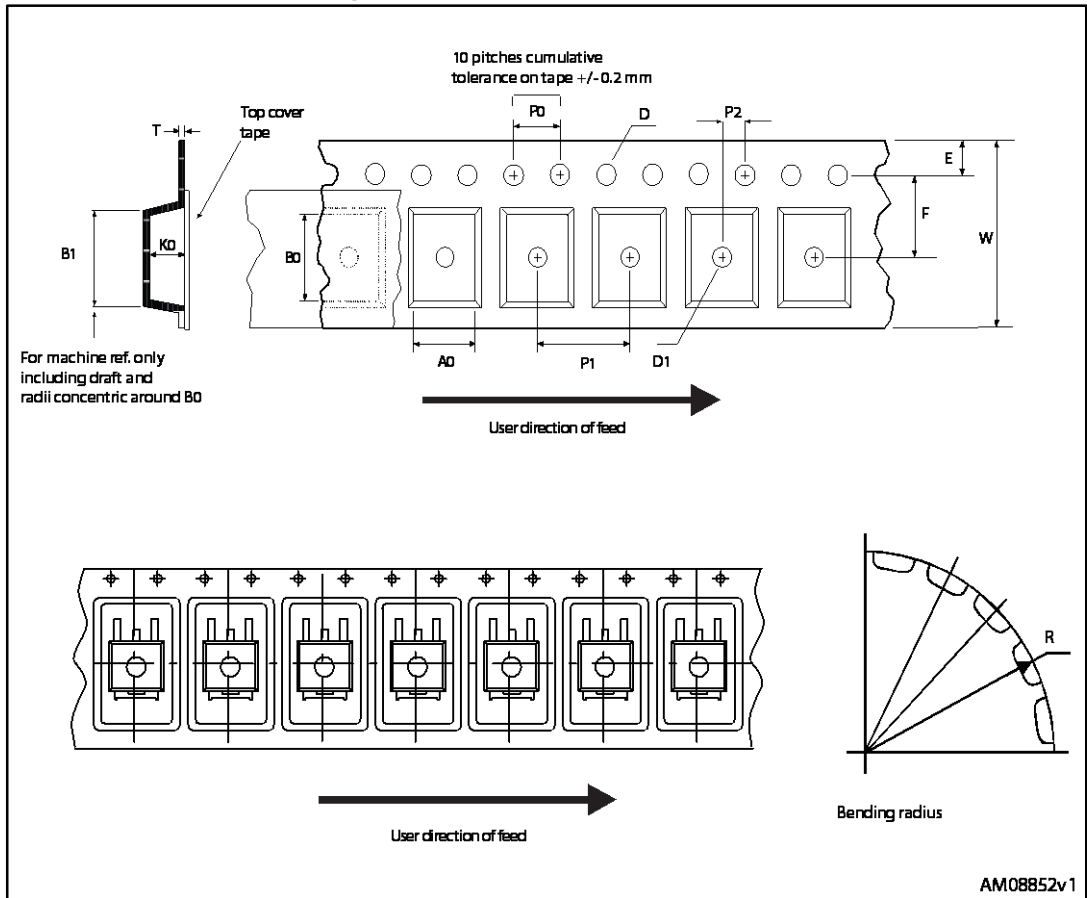


Figure 23: DPAK (TO-252) reel outline

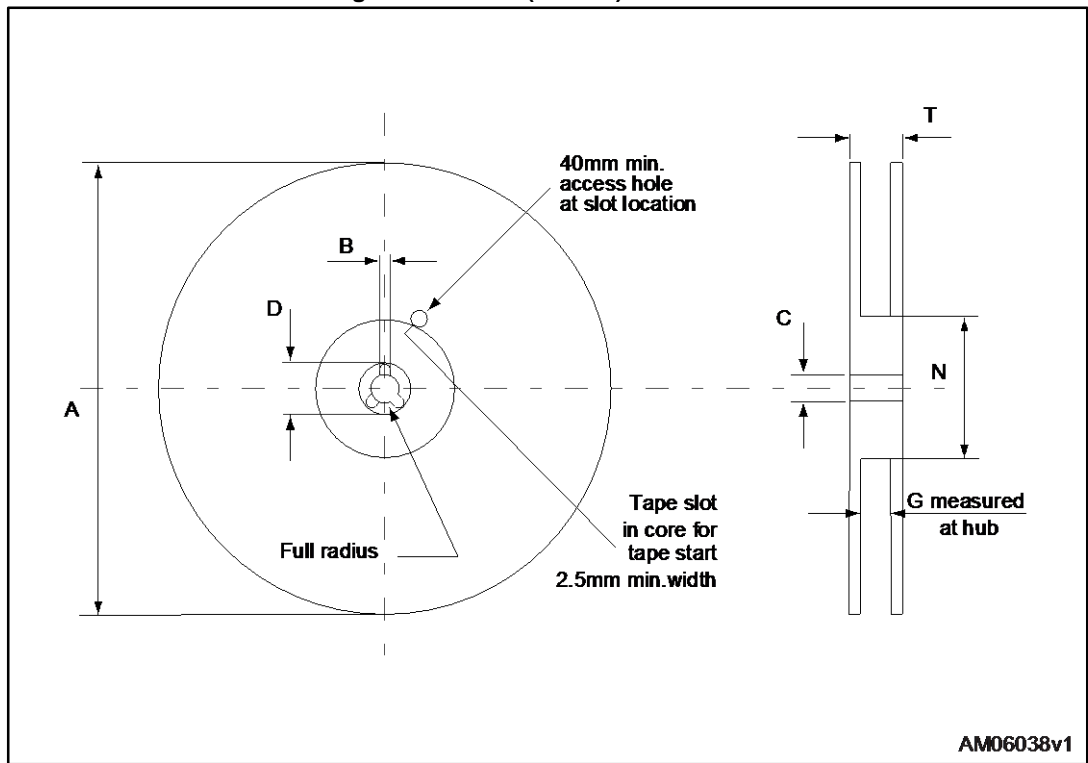


Table 11: DPAK (TO-252) tape and reel mechanical data

| Tape | | | Reel | | |
|------|------|------|-----------|------|------|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 6.8 | 7 | A | | 330 |
| B0 | 10.4 | 10.6 | B | 1.5 | |
| B1 | | 12.1 | C | 12.8 | 13.2 |
| D | 1.5 | 1.6 | D | 20.2 | |
| D1 | 1.5 | | G | 16.4 | 18.4 |
| E | 1.65 | 1.85 | N | 50 | |
| F | 7.4 | 7.6 | T | | 22.4 |
| K0 | 2.55 | 2.75 | | | |
| P0 | 3.9 | 4.1 | Base qty. | | 2500 |
| P1 | 7.9 | 8.1 | Bulk qty. | | 2500 |
| P2 | 1.9 | 2.1 | | | |
| R | 40 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 15.7 | 16.3 | | | |

5 Revision history

Table 12: Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 08-Jan-2016 | 1 | First release. |
| 09-May-2016 | 2 | Modified: title Modified: <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 3: "Thermal data"</i> , <i>Table 5: "On/off-state"</i> , <i>Table 6: "Dynamic"</i> , <i>Table 7: "Switching times"</i> and <i>Table 8: "Source-drain diode"</i> Added: <i>Section 3.1: "Electrical characteristics (curves)"</i> Modified: <i>Section 4: "Test circuits"</i> Minor text changes |

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