Si2403

SILICON LABORATORIES

V.22BIS ISOMODEM® CHIPSET WITH ERROR CORRECTION

Features

- Data modem formats
  - ITU-T, Bell
  - 300 bps up to 2400 bps
  - V.42, MNP2-4
- Caller ID decode
- 3.3 V power
- No external ROM or RAM required
- UART with flow control
- AT command set support

- Integrated DAA
  - Over 5000 V capacitive isolation
  - Parallel phone detect
  - Globally-compliant line interface
  - Overcurrent detection
- Fast connect
- Parallel interface
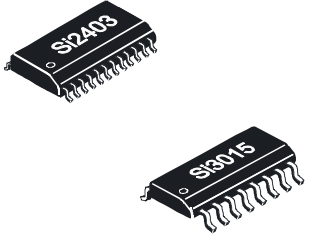- Call progress support
- Firmware upgradeable

Applications

- Set-top boxes
- E-mail terminals
- Point-of-sale terminals

- Digital video recorders
- Security systems
- Remote monitoring

Description

The Si2403 is a complete, ITU-V.22bis-compliant, 2400 bps modem chipset with integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line requirements with a single design. Available in two small packages, it eliminates the need for a separate DSP data pump, external RAM and ROM, modem controller, codec, isolation transformer, relays, opto-isolators, and 2- to 4-wire hybrid. The ISOmodem® chipset is ideal for embedded modem applications due to its small board space, low power consumption, and global compliance.

Functional Block Diagram
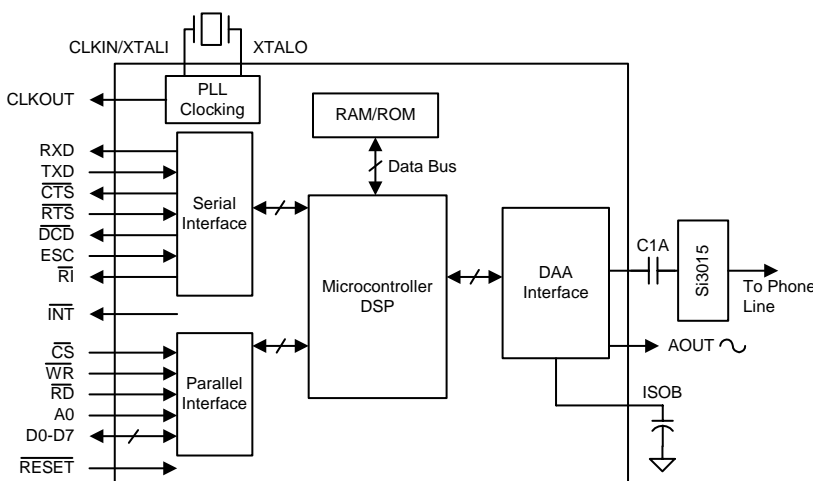
Ordering Information

This data sheet is valid only for those chipset combinations listed on page 63.

Pin Assignments

Patents pending

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	K-Grade, F-Grade	0	25	70	°C
Si2403 Supply Voltage, Digital[3]	V_D		3.0	3.3	3.6	V

Notes:
1. The Si2403 specifications are guaranteed when the typical application circuit (including component tolerance) and any Si2403 and any Si3015 are used. See "Typical Application Schematic" on page 11.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. The digital supply, V_D, operates from 3.0 to 3.6 V. The Si2403 interface supports 5 V logic (CLKIN/XTALI supports 3.3 V logic only).

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Table 2. DAA Loop Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT[1] = 1 DCT = 11 (CTR21)	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 42 mA, ACT = 1 DCT = 11 (CTR21)	—	—	14.5	V
DC Termination Voltage	V_{TR}	I_L = 50 mA, ACT = 1 DCT = 11 (CTR21)	—	—	40	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, ACT = 1 DCT = 11 (CTR21)	40	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT = 0 DCT = 01 (Japan)	—	—	6.0	V
DC Termination Voltage	V_{TR}	I_L = 100 mA, ACT = 0 DCT = 01 (Japan)	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ACT = 0 DCT = 10 (FCC)	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 100 mA, ACT = 0 DCT = 10 (FCC)	9	—	—	V
On-Hook Leakage Current	I_{LK}	V_{TR} = −48 V	—	—	7	µA
Operating Loop Current	I_{LP}	FCC/Japan Modes	13	—	120	mA
Operating Loop Current	I_{LP}	CTR21	13	—	60	mA
DC Ring Current[2]		DC flowing through ring detection circuitry	—	—	7	µA
Ring Detect Voltage[3]	V_{RD}	RT = 0	11	—	22	V_{rms}
Ring Detect Voltage[3]	V_{RD}	RT = 1	17	—	33	V_{rms}
Ring Frequency	F_R		15	—	68	Hz
Ringer Equivalence Number[4]	REN		—	—	0.2	

Notes:
1. ACT = U67, bit 5; DCT = U67, bits 3:2; RT = U67, bit 0; RZ = U67, bit 1.
2. R25 and R26 installed.
3. The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.
4. C15, R14, Z2, and Z3 not installed. RZ = 0.

Si2403
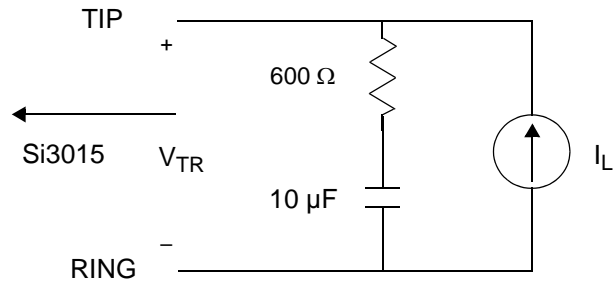
Figure 1. Test Circuit for Loop Characteristics

Table 3. DC Characteristics, V_D = 3.3 V

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	$I_O = -2$ mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	$I_O = 2$ mA	—	—	0.35	V
Input Leakage Current	I_L		−10	—	10	µA
Pullup Resistance Pins 3, 4, 9, 11, 13, 14, 16, 23, 24	R_{PU}		50	100	200	kΩ
Total Supply Current[*]	I_D	V_{D33} pin	—	26	35	mA
Total Supply Current, Powerdown[*]	I_D	PDN = 1	—	80	—	µA
*Note: All inputs at 0 or V_D. All inputs held static except clock, and all outputs unloaded (Static I_{OUT} = 0 mA).						

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Table 4. DAA AC Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate	Fs		—	9.6	—	kHz
Crystal Oscillator Frequency	F_{XTL}		—	4.9152	—	MHz
Transmit Frequency Response		Low –3 dBFS Corner	—	5	—	Hz
Receive Frequency Response		Low –3 dBFS Corner	—	5	—	Hz
Transmit Full Scale Level[1]	V_{FS}		—	1	—	V_{PEAK}
Receive Full Scale Level[1]	V_{FS}		—	1	—	V_{PEAK}
Dynamic Range[2,3,4]	DR	ACT[5] = 0, DCT[5] = 10 (FCC) I_L = 100 mA	—	82	—	dB
Dynamic Range[2,3,6]	DR	ACT = 0, DCT = 01 (Japan) I_L = 20 mA	—	83	—	dB
Dynamic Range[2,3,4]	DR	ACT = 1, DCT = 11(CTR21) I_L = 60 mA	—	84	—	dB
Transmit Total Harmonic Distortion[4,7]	THD	ACT = 0, DCT = 10 (FCC) I_L = 100 mA	—	–85	—	dB
Transmit Total Harmonic Distortion[5,7]	THD	ACT = 0, DCT = 01 (Japan) I_L = 20 mA	—	–76	—	dB
Receive Total Harmonic Distortion[6,7]	THD	ACT = 0, DCT = 01 (Japan) I_L = 20 mA	—	–74	—	dB
Receive Total Harmonic Distortion[4,7]	THD	ACT = 1, DCT = 11 (CTR21) I_L = 60 mA	—	–82	—	dB
AOUT Dynamic Range		VIN = 1 kHz	—	40	—	dB
AOUT THD		VIN = 1 kHz	—	40	—	dB
AOUT Full-Scale Level			—	0.7V_{DD}	—	V_{PP}
AOUT Mute Level			—	60	—	dB

Notes:
1. Measured at TIP and RING with 600 Ω termination at 1 kHz.
2. DR = 20 x log |Vin| + 20 x log (RMS signal/RMS noise).
3. Measurement is 300 to 3400 Hz. Applies to transmit and receive paths.
4. Vin = 1 kHz, –3 dBFS, Fs = 10300 Hz.
5. ACT = U67, bit 5; DCT = U67, bits 3:2.
6. Vin = 1 kHz, –6 dBFS, Fs = 10300 Hz.
7. THD = 20 x log (RMS distortion/RMS signal).

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D	4.1	V
Input Current, Si2403 Digital Input Pins	I_{IN}	±10	μA
Digital Input Voltage	V_{IND}	−0.3 to 5.3	V
CLKIN/XTALI Input Voltage	V_{XIND}	−0.3 to (V_D + 0.3)	V
Operating Temperature Range	T_A	−10 to 100	°C
Storage Temperature Range	T_{STG}	−40 to 150	°C
Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.			

Table 6. Switching Characteristics
(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade)

Parameter	Symbol	Min	Typ	Max	Unit
CLKOUT Output Clock Frequency		2.4576	—	39.3216	MHz
Baud Rate Accuracy	t_{BD}	−1	—	1	%
$\overline{CTS}$ or $\overline{RTS}$ ↑ High to Start Bit↓	t_{RTS}	10	—	—	ns
$\overline{RESET}$ ↓ to $\overline{RESET}$ ↑	t_{RS}	5.0	—	—	ms
$\overline{RESET}$ ↑ to 1st AT Command	t_{AT}	300	—	—	ms
Address Setup	t_{AS}	15	—	—	ns
Address Hold	t_{AH}	0	—	—	ns
$\overline{WR}$ Low Pulse Width	t_{WL}	50	—	—	ns
Write Data Setup Time	t_{WDSU}	20	—	—	ns
Write Cycle Time	t_{WC}	120	—	—	ns
Chip Select Setup	t_{CSS}	10	—	—	ns
Chip Select Hold	t_{CSH}	0	—	—	ns
$\overline{RD}$ Low Pulse Width	t_{RL}	50	—	—	ns
$\overline{RD}$ Low to Data Driven Time	t_{RLDD}	—	—	20	ns
Data Hold	t_{DH}	10	—	—	ns
$\overline{RD}$ High to Hi-Z Time	t_{DZ}	—	—	30	ns
Read Cycle Time	t_{RC}	120	—	—	ns
Note: All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_D − 0.4$ V, $V_{IL} = 0.4$ V					

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UART Time for Modem Receive Path (8N1 Mode)

8-Bit Data
Mode

RX

| Start | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | Stop |

t_{RTS}

t_{RTH}

$\overline{RTS}$
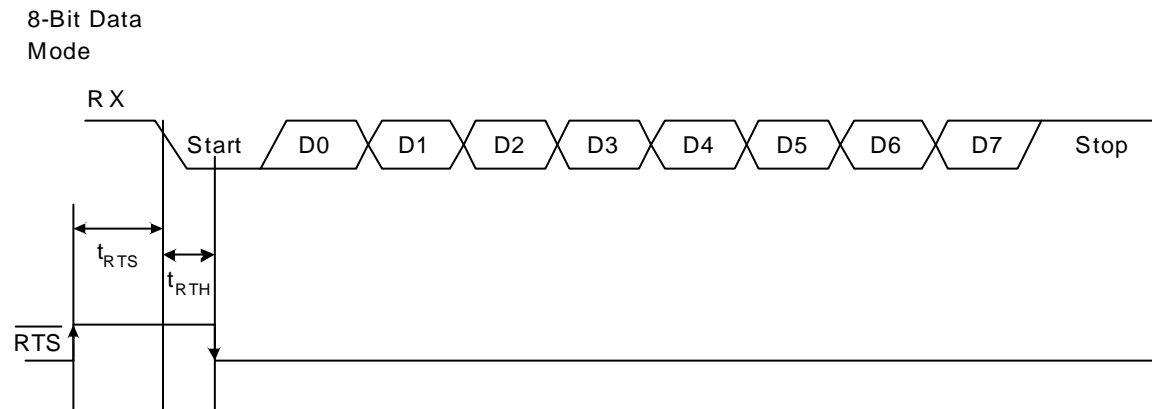
UART Timing for Modem Transmit Path (9N1 Mode with 9th Bit Escape)

9-Bit Data
Mode

TX

| Start | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | ESC | Stop |

t_{RTS}

t_{CTH}

$\overline{CTS}$
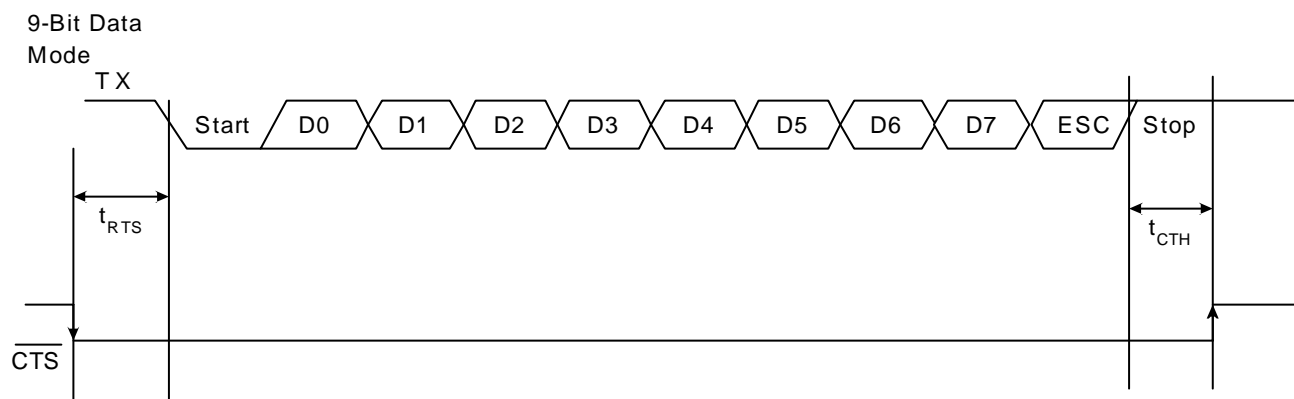
Figure 2. Asynchronous UART Serial Interface Timing Diagram

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Si2403
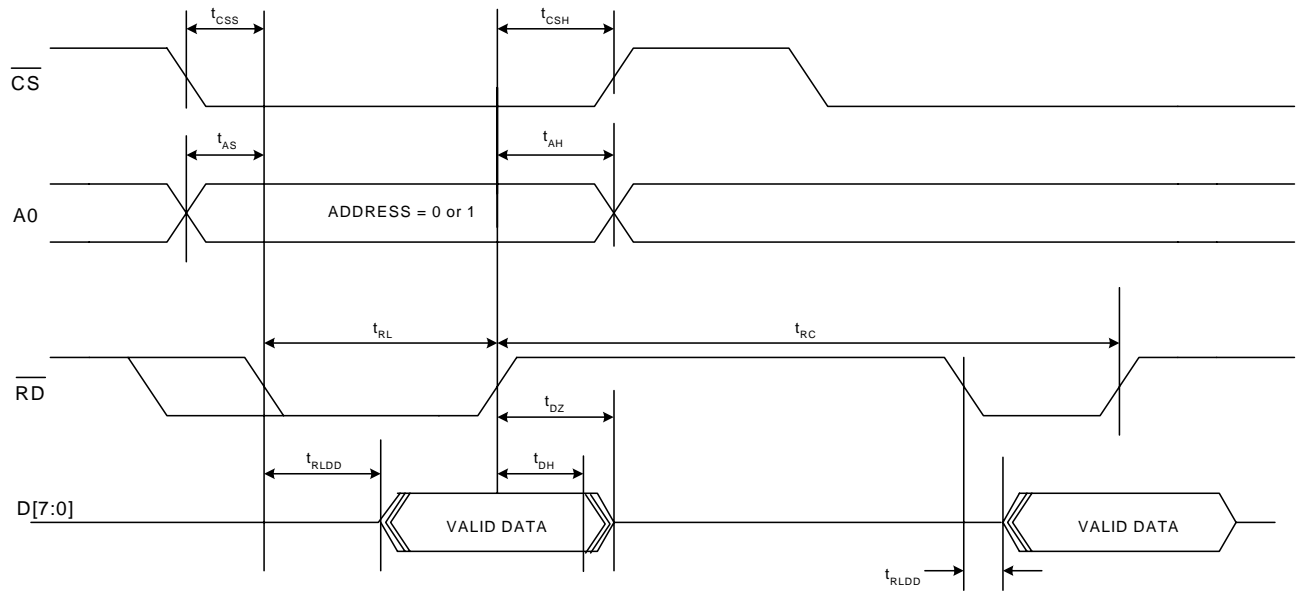
Figure 3. Parallel Interface Read Timing
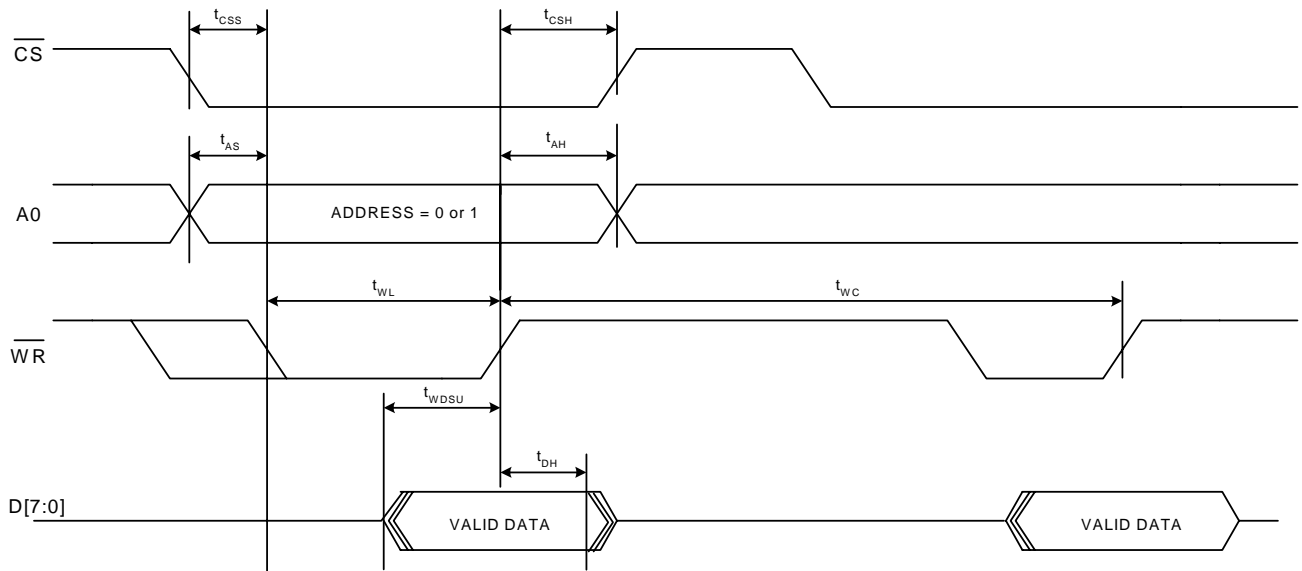
Figure 4. Parallel Interface Write Timing

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2. Typical Application Schematic

Refer to AN48 for Layout Guidelines
Please submit layout to Silicon Labs
for review prior to PCB fabrication.

Decoupling caps for U1 VD
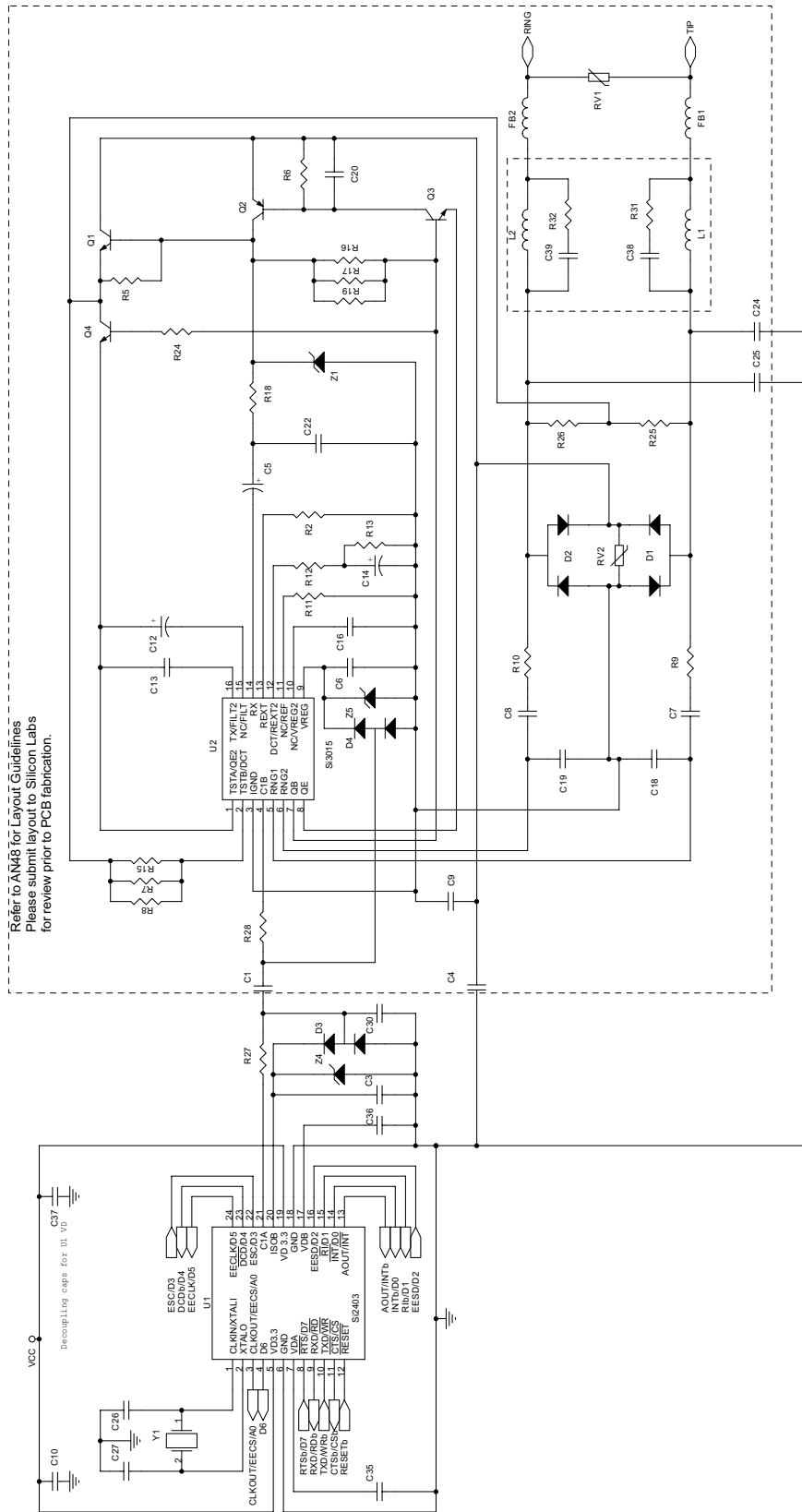
Note 1: R12, R13 and C14 are only required if complex AC termination is used (ACT bit = 1).
Note 2: See "Ringer Impedance" section for optional Czech Republic support.
Note 3: See "Billing Tone Immunity" section for optional billing tone filter (Germany, Switzerland, South Africa).
Note 4: R27, R28, D3, D4, Z4, Z5, R31, R32 may be populated for enhanced lightning option.
Note 5: L1,L2, C38, C39, R31, R32 are for EN55022/CISPR-22 Conducted Disturbance compliance.

3. Bill of Materials: Si2403 Chipset

Component	Value	Supplier(s)
C1,C4[1]	150 pF, 3 kV, X7R, ±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C3,C13,C35,C36	0.22 µF, 16 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C5[2]	0.1 µF, 50 V, Elec/Tant, ±20%	Venkel, Johanson, Murata, Panasonic
C6,C10,C16,C37	0.1 µF, 16 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata
C7,C8[3]	560 pF, 250 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C9	22 nF, 250 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata, Panasonic
C12	1.0 µF, 16 V, Tant, ±20%	Venkel, Panasonic
C14[2]	0.68 µF, 16 V, X7R/Elec/Tant, ±20%	Novacap, Venkel, AUX, Murata, Panasonic
C18,C19[3]	3.9 nF, 16 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata
C20	0.01 µF, 16 V, X7R, ±20%	Novacap, Venkel, Johanson, Murata
C22[4]	1800 pF, 50 V, X7R, ±20%	Not installed
C24,C25[1]	1000 pF, 3 kV, X7R, ±10%	Novacap, Venkel, Johanson, Murata, Panasonic
C26,C27	33 pF, 16 V, NPO, ±5%	Novacap, Venkel, Johanson, Murata
C30[4]	10 pF, 16 V, NPO, ±10%	Not Installed
C38,C39[2,5]	47 pF, 16 V, X7R, ±10%	Venkel
D1,D2[6]	Dual Diode, 300 V, 225 mA	Central Semiconductor
D3,D4[1]	BAV99 Dual Diode, 70 V, 350 mW	Diodes Inc., OnSemiconductor, Fairchild
FB1,FB2	Ferrite Bead, 600 Ω, ±25%, 200 mA	Murata
L1,L2[2,5]	68 µH, 120 mA, 4 Ω max, ±10%	Murata, Panasonic
Q1,Q3	A42, NPN, 300 V	OnSemiconductor, Fairchild, Zetex
Q2	A92, PNP, 300 V	OnSemiconductor, Fairchild, Zetex
Q4[7]	BCP56, NPN, 60 V, 1/2 W	OnSemiconductor, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, ST Microelectronics, Microsemi, TI

Notes:

1. The Si2403 design survives up to 3500 V longitudinal surges without R27, R28, D3, D4, Z4, and Z5. Adding the R27, R28, D3, D4, Z4, and Z5 enhanced lightning options increases longitudinal surge survival to greater than 6600 V. The isolation capacitors, C1, C4, C24, and C25, must also be rated to greater than the surge voltage. Y-class capacitors are recommended for highest surge survival.
2. For FCC-only designs, C14, C38, C39, R12, R13, R31, and R32 are not required (leave Si3015 pin 12 unconnected); L1 and L2 may be replaced with a short; R2 may be ±5%; with Z1 rated at 18 V, C5 may be rated at 16 V; also see Note 9.
3. If the auto answer, ring detect, and caller ID features are not used, R9, R10, C7, and C8 may be removed.
4. C22 and C30 may provide an additional improvement in emissions/immunity, depending on design and layout. Population option recommended. See "AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer's Guide" for details.
5. Compliance with EN55022 and/or CISPR-22 conductance disturbance tests requires the following: L1, L2, C38, C39, R31, and R32; D1 and D2 must be 400 V rated, and RV2 must be populated. See also "EN55022 and CISPR-22 Compliance" in "AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer's Guide".
6. Several diode bridge configurations are acceptable (suppliers include General Semi., Diodes Inc.)
7. Q4 may require copper on board to meet 1/2 W power requirement. (Contact manufacturer for details.)
8. RV2 can be installed to improve performance for multiple longitudinal surges.
9. The R7, R8, R15, and R16, R17, R19 resistors may each be replaced with a single resistor of 1.78 kΩ, 3/4 W, ±1%. For FCC-only designs, 1.78 kΩ, 1/16 W, ±5% resistors may be used.
10. If the parallel phone detection feature is not used, R25 and R26 may be removed.
11. To ensure compliance with ITU specifications, frequency tolerance must be less than 100 ppm including initial accuracy, 5-year aging, 0 to 70 °C, and capacitive loading. Crystals with 50 ppm initial accuracy typically satisfy this requirement.

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Component	Value	Supplier(s)
RV2[5,8]	270 V, MOV	Not Installed
R2[2]	402 Ω, 1/16 W, ±1%	Venkel, Panasonic
R5	100 kΩ, 1/16 W, ±1%	Venkel, Panasonic
R6	120 kΩ, 1/16 W, ±5%	Venkel, Panasonic
R7,R8,R15,R16,R17,R19[9]	5.36 kΩ, 1/4 W, ±1%	Venkel, Panasonic
R9,R10[3]	56 kΩ, 1/10 W, ±5%	Venkel, Panasonic
R11	9.31 kΩ, 1/16 W, ±1%	Venkel, Panasonic
R12[2]	78.7 Ω, 1/16 W, ±1%	Venkel, Panasonic
R13[2]	215 Ω, 1/16 W, ±1%	Venkel, Panasonic
R18	2.2 kΩ, 1/10 W, ±5%	Venkel, Panasonic
R24	150 Ω, 1/16 W, ±5%	Venkel, Panasonic
R25, R26[10]	10 MΩ, 1/16 W, ±5%	Venkel, Panasonic
R27, R28[1]	10 Ω, 1/10 W, ±5%	Venkel, Panasonic
R31, R32[2,5]	470 Ω, 1/16 W, ±5%	Venkel, Panasonic
U1	Si2403	Silicon Labs
U2	Si3015	Silicon Labs
Y1	4.9152 MHz, 20 pF, 100 ppm[11], 150 ESR	Not Installed
Z1[1]	Zener Diode, 43 V, 1/2 W	Vishay, OnSemiconductor, Rohm
Z4,Z5[1]	Zener Diode, 5.6 V, 1/2 W	Vishay, OnSemiconductor, Rohm

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1. The Si2403 design survives up to 3500 V longitudinal surges without R27, R28, D3, D4, Z4, and Z5. Adding the R27, R28, D3, D4, Z4, and Z5 enhanced lightning options increases longitudinal surge survival to greater than 6600 V. The isolation capacitors, C1, C4, C24, and C25, must also be rated to greater than the surge voltage. Y-class capacitors are recommended for highest surge survival.
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9. The R7, R8, R15, and R16, R17, R19 resistors may each be replaced with a single resistor of 1.78 kΩ, 3/4 W, ±1%. For FCC-only designs, 1.78 kΩ, 1/16 W, ±5% resistors may be used.
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Table 7. Protocol Characteristics

Item	Specification
Data Rate 2400 bps 1200 bps 300 bps 300 bps	ITU-T V.22bis ITU-T V.22bis, V.23, or Bell 212A ITU-T V.21 Bell 103
Data Format Bit asynchronous	Selectable 8, 9, 10, or 11 bits per character
Compatibility	V.23, V.22bis, V.22, V.21, Bell 212A, and Bell 103
Operating Mode Switched network	Two-wire full-duplex
Data Modulation 2400 bps 1200 bps 0 to 300 bps	16-level QAM/600 Baud ±0.01% 4-level PSK/600 Baud ±0.01% FSK 0–300 Baud ±0.01%
Answer Tone ITU-T V.22bis, V.22, and V.21 modes Bell 212A and 103 modes	2100 Hz ±3 Hz 2225 Hz ±3 Hz

Transmit Carrier
ITU-T V.22, V.22bis/Bell 212A
  Originate mode
  Answer mode
ITU-T V.21
  Originate mode
  Answer mode
Bell 103
  Originate mode
  Answer mode
	1200 Hz ±0.5 Hz
	2400 Hz ±1 Hz
	
	Mark (980 Hz ±12 Hz) Space (1180 Hz ±12 Hz)
	Mark (1650 Hz ±12 Hz) Space (1850 Hz ±12 Hz)
	
	Mark (1270 Hz ±12 Hz) Space (1070 Hz ±12 Hz)
	Mark (2225 Hz ±12 Hz) Space (2025 Hz ±12 Hz)

Output Level Permissive—Switched network	–9 dBm maximum

Receive Carrier
ITU-T V.22, V.22bis/Bell 212A
  Originate mode
  Answer mode
ITU-T V.21
  Originate mode
  Answer mode
Bell 103
  Originate mode
  Answer mode
	2400 Hz ±7 Hz
	1200 Hz ±7 Hz
	
	Mark (1850 Hz ±12 Hz) Space (1650 Hz ±12 Hz)
	Mark (1850 Hz ±12 Hz) Space (1650 Hz ±12 Hz)
	
	Mark (2225 Hz ±12 Hz) Space (2025 Hz ±12 Hz)
	Mark (1270 Hz ±12 Hz) Space (1070 Hz ±12 Hz)

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Table 7. Protocol Characteristics (Continued)

Item	Specification
Carrier Detect (level for ITU-T V.22bis, V.22, V.21, 212, 103) in Switched Network	Acquisition (–43 dBm) Release (–48 dBm)
Hysteresis	2 dBm minimum
DTE Interface	EIA/TIA-232-E (ITU-T V.24/V.28/ISO 2110)
Line Equalization	Automatic Adaptive
Connection Options	Loss of Carrier in ITU-T V.22bis and lower
Phone Types	500 (rotary dial), 2500 (DTMF dial)
Dialing	Pulse and Tone
DTMF Output Level	Per Part 68
Pulse Dial Ratio	Make/Break: 39/61%
Ring Cadence	On 2 seconds; Off 4 seconds
Call Progress Monitor	BUSY CONNECT (rate) NO CARRIER NO DIALTONE OK RING RINGING

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Si2403

4. Functional Description

The ISOmodem® chipset is a complete embedded-modem chipset with integrated direct-access arrangement (DAA) that provides a programmable line interface to meet global telephone line requirements. Available in two small packages, this solution includes a DSP data pump, a modem controller, on-chip RAM and ROM, an analog front end (AFE), a DAA, and analog output.

The Si2403 accepts standard modem AT commands and provides connect rates up to 2400 bps full-duplex over the public switched telephone network (PSTN). The Si2403 features a complete set of modem protocols including all ITU-T standard formats up to 2400 bps.

The Si2403 provides numerous additional features for embedded modem applications. The modem includes full caller ID detection and decoding for global standards. Call progress is supported through echoing result codes and is also programmable to meet global settings. Because the Si2403 integrates the DAA, analog features, such as parallel phone detect, overcurrent detection, and global PTT compliance with a single design, are included.

This device is ideal for embedded modem applications due to its small board space, low power consumption, and global compliance. The Si2403 solution includes a silicon DAA using Silicon Laboratories' proprietary capacitive isolation technology. This highly-integrated DAA can be programmed to meet worldwide PTT specifications for ac termination, dc termination, ringer impedance, and ringer threshold. In addition, the Si2403 has been designed to meet the most stringent worldwide requirements for out-of-band energy, billing-tone immunity, lightning surges, and safety requirements.

The Si2403 is designed to be rapidly incorporated into existing modem applications. The device interfaces directly through either a serial UART to a microcontroller or to a PC through a standard RS-232 transceiver. This interface allows for PC evaluation of the modem immediately upon powerup via the AT commands using standard terminal software. The Si2403 also provides an 8-bit parallel port.

The Si2403 solution requires only a few low-cost discrete components to achieve global compliance. See "Typical Application Schematic" on page 11.

4.1. Digital Interface

The ISOmodem chipset digital I/O can be configured as either a serial UART interface with flow control or as a parallel 8-bit interface.

Selection of a serial or parallel I/O interface is determined by the state of AOUT/$\overline{\text{INT}}$ (Si2403, pin 13) during the rising edge of $\overline{\text{RESET}}$. An internal pullup resistor forces the default state to serial mode operation. An external 10 kΩ pulldown resistor can be connected to AOUT/$\overline{\text{INT}}$ to force selection of parallel mode. Additionally, when selecting parallel mode, $\overline{\text{CS}}$ should remain high until after the rising edge of $\overline{\text{RESET}}$. Configuration of pins 3, 4, 8–11, 13–16, and 22–24 is determined by this interface selection.

4.2. Serial Interface

The ISOmodem chipset supports data terminal equipment (DTE) rates up to 307.2 kbps with the standard serial UART format. Upon powerup, the UART defaults to a 19.2 kbps baud rate. If a pulldown resistor ≤ 10 kΩ is placed between D2 (Si2403, pin 16) and GND (Si2403, pin 6), the DTE rate is set by the autobaud feature after reset.

The serial interface also provides a hardware pin, $\overline{\text{DCD}}$ (data carrier detect), which remains low as long as the Si2403 is connected.

The $\overline{\text{INT}}$ interrupt pin can be programmed to alert the host of changes to the interrupts listed in I/O Control 0 (U70).

4.2.1. Autobaud

The ISOmodem chipset includes an automatic baud rate detection feature that allows the host to start transmitting data at any standard DTE rate from 300 bps to 307.2 kbps. This feature is enabled by placing a pulldown resistor ≤10 kΩ between D2 (pin 16) and GND.

4.3. Parallel Interface

The parallel interface is an 8-bit data bus with a single bit address. Figure 3 on page 10 shows the required timing for the parallel interface.

If A0 = 0, the data bus represents a read/write to the "Parallel Interface 0 (0x00)" register on page 57. If A0 = 1, the data bus represents a read/write to the "Parallel Interface 1 (0x01)" register on page 58).

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4.4. Command Mode

Upon reset, the ISOmodem® chipset is in command mode and accepts "AT" commands. An outgoing modem call can be made using the "ATDT#" (tone dial) or "ATDP#" (pulse dial) command after the device is configured. If the handshake is successful, the modem responds with the response codes detailed in Table 12 on page 32 and enters data mode.

4.5. Data Mode

The ISOmodem chipset is in data mode while it has a connection to another modem or is in the process of establishing a connection.

In command and data mode, the Si2403 operates in asynchronous DTE mode only. Data protocols are available to provide error correction to improve reliability (V.42 and MNP2-4).

Each connection between two modems in data mode begins with a handshaking sequence. During that sequence, the modems determine the line speed, data protocol, and related parameters for the data link. Configuration through AT commands determines the range of choices available to the modem during the negotiation process.

4.6. Fast Connect

The ISOmodem chipset supports a Fast Connect mode of operation to reduce the time of a connect sequence in originate mode. The Fast Connect modes can be enabled for V.21, V.22, V.22bis, Bell103, and Bell212. In addition, the Si2403 may be set to either default asynchronous data communications equipment (DCE) mode or a transparent HDLC synchronous mode.

4.7. Clocking/Low-Power Modes

The ISOmodem chipset contains an on-chip phase-locked loop (PLL) and clock generator. Using either a single crystal or master clock input, the Si2403 can generate all the internal clocks required to support the featured modem protocols. Either a 4.9152 MHz clock (3.3 V max input—see Table 5 on page 8) on XTALI or a 4.9152 MHz crystal across XTALI and XTALO form the master clock (±100 ppm max) for the Si2403. This clock source is sent to an internal PLL that generates all necessary internal system clocks including the DSP clock. Figure 5 shows a block diagram of how the DSP clock and the CLKOUT are derived.

Using the S24 S-register, the Si2403 can be set to automatically enter sleep mode after a pre-programmed time of inactivity with either the DTE or the remote modem. The sleep mode is entered after (S24) seconds have passed since the TX FIFO has been empty. The Si2403 remains in the sleep state until either a 1 to 0 transition on TXD (serial mode) or a 1 to 0 transition on $\overline{CS}$ (parallel mode) occurs.

Additionally, the Si2403 may be placed in a complete Powerdown mode. Complete powerdown is accomplished via U65[13] (PDN). Once the PDN bit is written, the Si2403 completely powers down and can only be powered back on via the $\overline{RESET}$ pin.

A 78.6432 MHz/(R1 + 1) clock is produced on the CLKOUT pin that may be used as an external system clock. R1 may be programmed via U5E to any value between 1 and 31 (default value = 31).

4.9152 MHz
CLKIN (pin 1) → 78.6432 MHz PLL → To internal clocking

÷ (R1 + 1) → CLKOUT (pin 3)

$1 \leq R1 \leq 31$
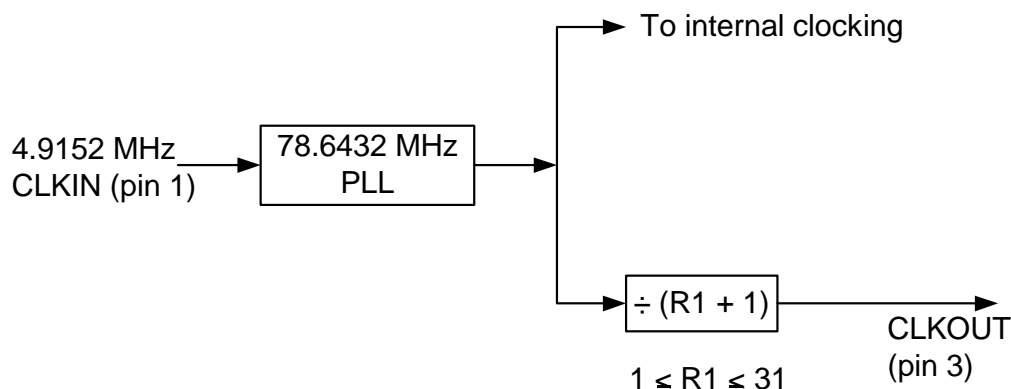
Figure 5. DSP and CLKOUT Generation

4.8. Error Correction

The ISOmodem® chipset can employ error-correction (reliable) protocols to ensure error-free delivery of asynchronous data sent between the host and the remote end. The Si2403 supports V.42 and MNP2-4 error correction protocols. V.42 (LAPM) is most commonly used and is enabled by default.

4.9. Wire Mode

Wire mode is used to communicate with standard non-error correcting modems. When optioned with \N3, the ISOmodem chipset falls back to wire mode if it fails in an attempt to negotiate a V.42 or MNP link with the remote modem. Error correction is not active in wire mode.

4.10. Caller ID Operation

The ISOmodem chipset supports full type 1 caller ID detection and decode for the US Bellcore, European ETSI, UK, and Japanese caller ID protocols. Caller ID is enabled via the +VCID and +VCDT commands.

4.11. Parallel Phone Detection

The ISOmodem chipset is able to detect when another telephone, modem, or other device is using the phone line.

This allows the host to avoid interrupting another phone call when the phone line is already in use and to intelligently handle an interruption when the Si2403 is using the phone line.

4.11.1. On-Hook Line-in-Use Detection

When the ISOmodem chipset is sharing the telephone line with other devices, it is important that it not interrupt a call in progress. To detect whether another device is using the shared telephone line, the host can use the Si2403 to monitor the TIP-RING dc voltage with the LVCS (Line Voltage and Current Sense) register (U79, bits 4:0). See Figure 6 on page 19. See also the %Vn commands for automatic line-in-use detection.

4.11.2. Off-Hook Intrusion Detection

When the ISOmodem chipset is off-hook, an algorithm is implemented in the Si2403 to automatically monitor the TIP-RING loop current via the LVCS register. When the Si2403 is off-hook, the LVCS register switches from representing the TIP-RING voltage to representing the TIP-RING current. (See Figure 7 on page 19.) Upon detecting an intrusion, the Si2403 alerts the host to the condition via the INT pin.
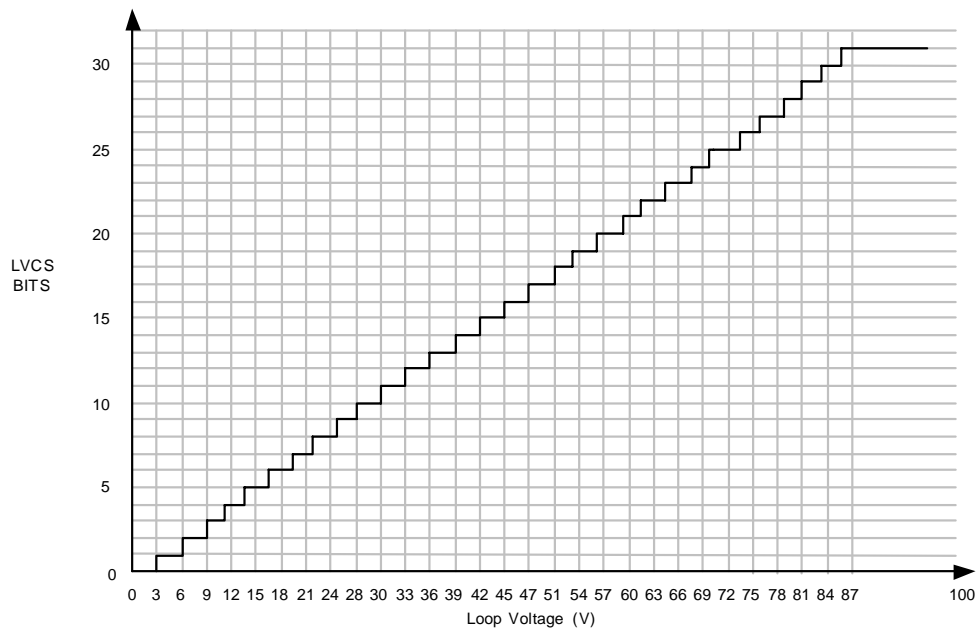
Figure 6. Loop Voltage
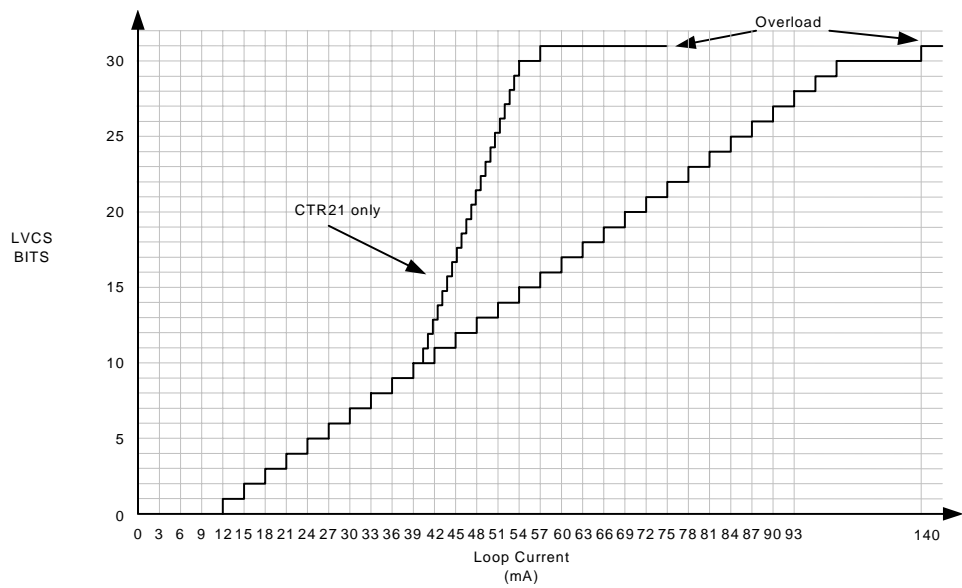
Figure 7. Loop Current

4.12. Overcurrent Detection

The ISOmodem® chipset includes an overcurrent detection feature that measures the loop current at a programmable time after the Si2403 goes off-hook. This allows the Si2403 to detect if it is connected to an improper telephone line. The overcurrent detection feature may be enabled by setting the OCDM bit (U70, bit 11). OHT (U77, bits 8:0) sets the delay after off-hook until the loop current is measured.

4.13. Global Operation

The ISOmodem chipset contains an integrated silicon direct-access arrangement (Silicon DAA) that provides a programmable line interface to meet international telephone line interface requirements. "AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer's Guide" gives the DAA register settings required to meet international PTT standards.

Additionally, the user-access registers (via the AT:U and AT:R commands) may be programmed for country-specific settings, such as dial tone, ring, ringback, and busy tone. See AN70 for complete details.

4.14. Firmware Upgrades

The ISOmodem chipset contains an on-chip program ROM that includes the firmware required for the features listed in this data sheet. In addition, the Si2403 contains on-chip program RAM to accommodate minor changes to the ROM firmware. This allows Silicon Labs to provide future firmware updates to optimize the characteristics of new modem designs and those already deployed in the field. See AN70 for further information.

4.15. EEPROM Interface

The ISOmodem chipset supports an optional serial peripheral interface (SPI) bus serial EEPROM. The EEPROM must support SPI mode 3 with a 16-bit (8 kbit – 64 kbit range) address. Upon powerup, if a pulldown resistor ≤10 kΩ is placed between D6 (Si2403, pin 4) and GND, the Si2403 attempts to detect an EEPROM. An installed EEPROM may contain custom default settings, firmware upgrades, and/or user-defined AT command macros for use in custom AT commands or country codes.

4.16. AT Commands

At powerup, the Si2403 is in the AT command mode. In command mode, the modem monitors the input (serial or parallel) checking constantly for a valid command. (AT commands are described in Table 8.)

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Table 8. Basic AT Command Set (Command Defaults in Bold)

Command	Action
$	Display AT command mode settings.
A	Answer incoming call.
A/	Re-execute last command. This is the only command not preceded by "AT" or followed by a <CR>.
Dn	Dial The dial command, which may be followed by one or more dial command modifiers, manually dials a phone number: | Modifier	Function
! or &	Flash hook switch for FHT (U4F) ms (default: 500 ms)
, or <	Pause before continuing for S8 seconds (default: 2 seconds)
;	Return to AT command mode after verifying dialtone and dialing any digits.
G	Telephone voting mode. This modifier, intended for use in Japan, enables a special dial-in voting mode that may be used with certain automated voting systems. When this modifier is placed anywhere in the dial string (e.g. ATDG), the Si2403 will dial the phone number and wait S7 seconds (60 by default) to detect a busy tone. When the busy tone is detected, the Si2403 will report whether or not a polarity reversal occurs between the time the last digit is dialed and the detection of the busy tone. The Si2403 will report either "POLARITY REVERSAL" or "NO POLARITY REVERSAL". It is not possible to establish a modem connection when using this command.
P	Pulse (rotary) dialing—pulse digits: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9
T	Tone (DTMF) dialing—DTMF digits: *, #, A, B, C, D, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.
W	Wait for dial tone before continuing for S14 seconds (default: 12 seconds). Blind dialing modes X0, X1, and X3 do not affect the W command. If the DOP bit (U7A, bit 7) is set, the "ATDTW" command will cause the Si2403 to pause dialing and either report an "OK" if a dialtone is detected or "NO DIALTONE" if a dial tone is not detected.	
En	Local DTE echo
E0	Disable
E1	**Enable**
Hn	Hook switch.
H0	Go on-hook (hang up modem).
H1	Go off-hook.
In	Identification and checksum.

Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action
I0	Display Si2403 revision code. B: Revision B C: Revision C, etc.
I1	Display Si2403 firmware revision code (numeric).
I3	Display line-side revision code. 15F = Si3015 Revision F
I6	Display the Si2403 model number. "2403" = Si2403
I7	Diagnostic Results 1. See "AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer's Guide" for details.
I8	Diagnostic Results 2. See AN70 for details.
Mn	Speaker operation (via AOUT).
M0	**Speaker is always off.**
M1	Speaker is on while dialing and handshaking; off in Data mode.
M2	Speaker is always on.
M3	Speaker is off while dialing; on during handshaking and retraining.
On	Return to Data mode from command mode operation.
O0	Return to Data mode.
O1	Return to Data mode and perform a full retrain (at any speed except 300 bps).
O2	Return to Data mode and perform rate renegotiation.
Qn	Response mode.
Q0	**Enable result codes (see Table 12 on page 32)**
Q1	Disable result codes (enable quiet mode).
R	Initiate V.23 reversal.
Sn	S-register operation (see Table 13 on page 33).
S$	List contents of all S registers.
Sn?	Display contents of S-register n.
Sn=x	Set S-register n to value x (where n and x are decimal values).
Vn	Result code type (see Table 12 on page 32).
V0	Numeric result codes.
V1	**Verbal result codes**
Xn	Call Progress Monitor (CPM)—This command controls which CPM signals are monitored and reported to the host from the Si2403. (See Table 12 on page 32.)
X0	Basic results; disable CPM—Blind dial (does not wait for dial tone). CONNECT message does not include speed.
X1	Extended results; disable CPM—Blind dial. CONNECT message includes speed.
X2	Extended results and detect dial tone only—Add dial tone detection to X1 mode. Does not blind dial.
X3	Extended results and detect busy only—Add busy tone detection to X1 mode.
X4	**Extended results, full CPM—Full CPM enabled, CONNECT message includes speed.**

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Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action
X5	Extended results—Full CPM enabled including ringback detection. Adds ringback detection to X4 mode.
Yn	Long space disconnect—Modem hangs up after 1.5 seconds or more of continuous space while on-line.
Y0	**Disable.**
Y1	Enable.
Z	Hard Reset—This command is functionally equivalent to pulsing the $\overline{\text{RESET}}$ pin low. (See t_{AT} in Table 6 on page 8.)
:E	Read from serial EEPROM.
:I	Interrupt Read—This command causes the Si2403 to report the lower 8 bits of the interrupt register I/O Control 0 (U70). The CID, OCD, PPD, and RI bits are also cleared, and the $\overline{\text{INT}}$ pin (INT bit in parallel mode) is deactivated on this read.
:M	Write to serial EEPROM.
:P	Program RAM Write—This command is used to upload firmware supplied by Silicon Labs to the Si2403. The format for this command is AT:Paaaa,xxxx,yyyy,.... where aaaa is the first address in hexadecimal, and xxxx,yyyy,.... is data in hexadecimal. Only one :P command is allowed per AT command line. No other commands can be concatenated in the :P command line. This command is only for use with special files provided by Silicon Laboratories. Do not attempt to use this command for any other purpose. Use &T6 to display checksum for patch verification.
:R	User-Access Register Read—This command allows the user to read from the user-access registers. (See pages 35–53.) The format is "AT:Raa", where aa = user-access address in hexadecimal. The "AT:R" command causes all the U- registers to be displayed.
:U	User-Access Register Write—This command allows the user to write to the 16-bit user-access registers. (See page 35.) The format is "AT:Uaa,xxxx,yyyy,zzzz,..." where aa = user-access address in hexadecimal. xxxx = data in hexadecimal to be written to location aa. yyyy = data in hexadecimal to be written to location (aa + 1). zzzz = data in hexadecimal to be written to location (aa + 2). etc.

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Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action
+GCI = X	Country settings - Automatically configure all registers for a particular country. X Country 0 Japan 9 Australia A Austria F Belgium 16 Brazil 1B Bulgaria 20 Canada 26 China 27 Columbia 2E Czech Republic 31 Denmark 35 Ecuador 3C Finland 3D France 42 Germany 46 Greece 50 Hong Kong 51 Hungary 53 India 57 Ireland 58 Israel 59 Italy 61 South Korea 69 Luxembourg 6C Malaysia 73 Mexico 7B Netherlands 7E New Zealand 82 Norway 87 Paraguay 89 Philippines 8A Poland 8B Portugal 9C Singapore 9F South Africa A0 Spain A5 Sweden A6 Switzerland B8 Russia B4 United Kingdom **B5** **United States** FE Taiwan **Note:** U-registers are configured to Silicon Laboratories' recommended values. Changes may be made by writing individual registers after sending the AT+GCI command. Several countries use the same configurations as the United Kingdom and the United States. Refer to "AN93: Modem Designer's Guide" for details.
+GCI = ?	List all possible country code settings.
+GCI?	List current country code setting (response is: + GCI:<setting>)

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Table 8. Basic AT Command Set (Command Defaults in Bold) (Continued)

Command	Action
+VCDT = X	Caller ID Type. X̲ <u>Mode</u> **0** **After ring only** 1 Always on 2 UK 3 Japan
+VCID = X	Caller ID Enable. X̲ <u>Mode</u> **0** **Off** 1 On—formatted 2 On—raw data format

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4.17. Extended AT Commands

The extended AT commands are supported by the Si2403 and are described in Tables 9 through 11.

Table 9. Extended AT& Command Set (Command Defaults in Bold)

Command	Action
&$	Display AT& current settings.
&D0	ESC (pin 22) is not used.
&D1	**ESC (pin 22) escapes to command mode from data mode if also enabled by HES U70, bit 15.**
&D2	ESC (pin 22) assertion during a modem connection causes the modem to go on-hook and return to command mode.
&D3	ESC (pin 22) assertion causes ATZ command (reset and return OK result code).
&Gn	Line connection rate limit—This command sets an upper limit on the line speed that the Si2403 can connect. Note that the &Hn commands may limit the line speed as well (&Gn not used for &H0 or &H1). Not all modulations support rates given by &G. Any improper setting will be ignored.
&G3	1200 bps max
&G4	2400 bps max
&Hn	Switched network handshake mode—&Hn commands must be on a separate command line from ATD, ATA, or ATO commands.
&H6	ITU-T V.22bis only (2400 bps or 1200 bps)
&H7	ITU-T V.22 only (1200 bps)
&H8	Bell 212 only (1200 bps)
&H9	Bell 103 only (300 bps)
&H10	ITU-T V.21 only (300 bps)
&H11	V.23 (1200/75 bps)
&Pn	Japan pulse dialing
&P0	Configure Si2403 for 10 pulse-per-second pulse dialing. For Japan.
&P1	Configure Si2403 for 20 pulse-per-second pulse dialing. For Japan.
&Tn	Test Mode
&T0	Cancel Test Mode (Escape to command mode to issue AT&T0). This command will also report the number of bit errors encountered on the previous &T4 test.
&T2	Initiate ITU-T V.54 (ANALOOP) test. Modulation set by &H AT command. Test loop is through the DSP (Si2403 device) only. The Si2403 echoes data from TX pin (Register 0 in parallel mode) back to RX pin (Register 0 in parallel mode).
&T3	Initiate ITU-T V.54 (ANALOOP) test. Modulation set by &H AT command. Test loop is through the DSP (Si2403), DAA interface section (Si2403), isolation interface (Si3015), and analog hybrid circuit (Si3015). Si2403 echoes data from TX pin (Register 0 in parallel mode) back to RX pin (Register 0 in parallel mode). Phone line termination required as in Figure 1. To test only the link operation, the hybrid and AFE codec can be removed from the test loop by setting the DL bit (U62, bit 1).
&T4	Initiate transmit as originating modem with automatic data generation. Modulation, data rate, and symbol rate are set by &H, &G, and S41. Data pattern is set by the S40 register. Continues until the ATH command is sent after an escape into command mode. Data is also demodulated as in ANALOOP, and any bit errors are counted to be displayed after the test using &T0.

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Table 9. Extended AT& Command Set (Command Defaults in Bold) (Continued)

Command	Action
&T5	Initiate transmit as answering modem with automatic data generation. Modulation, data rate, and symbol rate are set by &H, &G, and S41. Data pattern is set by the S40 register. Continues until the ATH command is sent after an escape into command mode. Data is also demodulated as in ANALOOP, and any bit errors are counted to be displayed after the test using &T0.
&T6	Compute checksum for firmware-upgradeable section of program memory. If no firmware upgrade is installed, &T6 returns 0xDE5C.
&Xn	Automatic determination of telephone line type.
&X0	Abort &x1 or &x2 command.

&X1	Automatic determination of telephone line type.
	Result code: WXYZn
	W: 0 = line supports DTMF dialing.
	          1 = line is pulse dial only.
	X: 0 = line supports 20 pps dialing.
	          1 = line supports 10 pps dialing only.
	Y: 0 = extension network present (PBX).
	          1 = outside line (PSTN) connected directly.
	Z: 0 = continuous dialtone.
	          1 = make-break dialtone.
	n: 0–9 (number required for outside line if Y = 0).

&X2	Same as &X1, but Y result (PBX) is not tested.
*Y2A	Produce a constant answer tone (ITU-T) and return to command mode. The answer tone continues until the ATH command is received or the S7 timer expires.

Table 10. Extended AT% Command Set (Command Defaults in Bold)

Command	Action
%$	Display AT% command settings.
%B	Report blacklist. See also S42 register.
%On	Answer mode
%O1	**Si2403 will auto-answer a call in answer mode**
%O2	Si2403 will auto-answer a call in originate mode
%Vn	Automatic Line Status Detection. After the %V1 and %V2 commands are issued, the Si2403 will automatically check the telephone connection for whether or not a line is present. If a line is present, the Si2403 will automatically check if the line is already in use. Finally, the Si2403 will check line status both before going off-hook and again before dialing. %V1 uses the fixed method, and %V2 uses the adaptive method. %V0 (default) disables this feature.
%V0	**Disable automatic line-in-use detection.**
%V1	Automatic Line Status Detection - Fixed Method. Description: Before going off-hook with the ATD, ATO, or ATA commands, the Si2403 compares the line voltage (via LVCS) to registers NOLN (U83) and LIUS (U84): Loop Voltage Action $0 \leq \text{LVCS} \leq \text{NOLN}$Report "NO LINE" and remain on-hook. $\text{NOLN} \leq \text{LVCS} \leq \text{LIUS}$Report "LINE IN USE" and remain on-hook. $\text{LIUS} \leq \text{LCVS}$ Go off-hook and establish a modem connection. Once the call has begun, the off-hook intrusion algorithm (described in "Off-Hook Intrusion Detection" on page 18) operates normally. In addition, the Si2403 will report "NO LINE" if the telephone line is completely disconnected. If the HOI bit (U77, bit 11) is set, "LINE IN USE" is reported upon intrusion.
%V2	Automatic Line Status Detection - Adaptive Method. Description: Before going off-hook with the ATD, ATO, or ATA commands, the Si2403 compares the line voltage (via LVCS) to the NLIU (U85) register: Loop Voltage Action $0 \leq \text{LVCS} \leq (0.0625 \times \text{NLIU})$Report "NO LINE" and remain on-hook. $(0.0625 \times \text{NLIU}) < \text{LVCS} \leq (0.85 \times \text{NLIU})$Report "LINE IN USE" and remain on-hook. $(0.85 \times \text{NLIU}) < \text{LCVS}$Go off-hook and establish a modem connection. The NLIU register is updated every 1 ms with the minimum non-zero value of LVCS in the last 30 ms. This allows the Si2403 to eliminate errors due to 50/60 Hz interference and also adapt to relatively slow change in the on-hook dc reference value on the telephone line. This algorithm does not allow any non-zero values for NLIU below 0x0007. The host may also initialize NLIU prior to issuing the %V2 command. Once the call has begun, the off-hook intrusion algorithm (described in "Off-Hook Intrusion Detection" on page 18) operates normally. In addition, the Si2403 will report "NO LINE" if the telephone line is completely disconnected. If the HOI (U77, bit 11) bit is set, "LINE IN USE" is reported upon intrusion.

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Table 11. Extended AT\ Command Set (Command Defaults in Bold)

Command	Action
\$	Display AT\ command settings.
\Bn	Character length will be automatically set in autobaud mode.
\B0	6N1—six data bits, no parity, one stop bit, one start bit, eight bits total (\N0 only)[1]
\B1	7N1—seven data bits, no parity, one stop bit, one start bit, nine bits total (\N0 only)[1]
\B2	7P1—seven data bits, parity optioned by \P, one stop bit, one start bit, 10 bits total
\B3	**8N1—eight data bits, no parity, one stop bit, one start bit, 10 bits total**
\B5	8P1—eight data bits, parity optioned by \P, one stop bit, one start bit, 11 bits total (\N0 only)
\B6	8X1—eight data bits, one escape bit, one stop bit, one start bit, 11 bits total (enables ninth-bit escape mode)
\Nn	Asynchronous protocol
\N0	Wire mode (no error correction)
\N2	MNP reliable mode. The Si2403 attempts to connect with the MNP protocol. If unsuccessful, the call is dropped.
\N3	**V.42 auto-reliable—The Si2403 attempts to connect with the V.42 protocol. If unsuccessful, the MNP protocol is attempted. If unsuccessful, wire mode is attempted.**
\N4	V.42 (LAPM) reliable mode (or drop call)—Same as \N3 except that the Si2403 drops the call instead of connecting in MNP or wire mode.
\N5	V.42 and MNP reliable mode - The Si2403 attempts to connect with V.42. If unsuccessful, MNP is attempted. If MNP is unsuccessful, the call is dropped.
\Pn	Parity type will be automatically set in autobaud mode.
\P0	**Even**
\P1	Space[1]
\P2	Odd
\P3	Mark[1]
\Qn	Modem-to-DTE flow control
\Q0	Disable all flow control—Note that this may only be used if the DTE speed and the VF speed are guaranteed to match throughout the call.
\Q2	**Use CTS only**

Notes:
1. When in autobaud mode, \B0, \B1, and \P1 will not be detected automatically. The combination of \B2 and \P3 will be detected. This is compatible with seven data bits, no parity, two stop bits. Seven data bits, no parity, one stop bit may be forced by sending AT\T17\B1.
2. The autobaud feature does not detect this rate.
3. Default is \T16 if a pulldown is connected to pin 16; otherwise, the default is \T9.

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Table 11. Extended AT\ Command Set (Command Defaults in Bold) (Continued)

Command	Action
\Q3	Use RTS/CTS
\Q4	Use XON/XOFF flow control for modem-to-DTE interface. Does not enable modem-to-modem flow control.
\Tn	DTE rate - Change DTE rate. When changing rates, the result code "OK" is sent at the old DTE rate. All options except \T16 lock the DTE to the given rate, and subsequent commands must be sent at this rate. When \T16 is used (or at reset when pin 16 is pulled down), automatic bandrate detection is used for subsequent commands.
\T0	300 bps
\T1	600 bps
\T2	1200 bps
\T3	2400 bps
\T4	4800 bps
\T5	7200 bps
\T6	9600 bps
\T7	12.0 kbps[2]
\T8	14.4 kbps
\T9	**19.2 kbps[3]**
\T10	38.4 kbps
\T11	57.6 kbps
\T12	115.2 kbps
\T13	230.4 kbps
\T14	245.760 kbps[2]
\T15	307.200 kbps
\T16	**Autobaud on[3]**
\T17	Autobaud off; lock at current baud rate.

Notes:
1. When in autobaud mode, \B0, \B1, and \P1 will not be detected automatically. The combination of \B2 and \P3 will be detected. This is compatible with seven data bits, no parity, two stop bits. Seven data bits, no parity, one stop bit may be forced by sending AT\T17\B1.
2. The autobaud feature does not detect this rate.
3. Default is \T16 if a pulldown is connected to pin 16; otherwise, the default is \T9.

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Table 11. Extended AT\ Command Set (Command Defaults in Bold) (Continued)

Command	Action
\U	Serial mode—causes a low pulse (25 ms) on $\overline{\text{RI}}$ and $\overline{\text{DCD}}$. $\overline{\text{INT}}$ to be the inverse of ESC. $\overline{\text{RTS}}$ to be the inverse of $\overline{\text{CTS}}$. Parallel mode—causes a low pulse (25 ms) on $\overline{\text{INT}}$. This command terminates with a $\overline{\text{RESET}}$.
\Vn	Connect message type
\V0	**Report connect message and protocol message**
\V2	Report connect message only (exclude protocol message)
\V4	Report connect and protocol message with both upstream and downstream connect rates.
*Note:	
Notes:	

Notes:
1. When in autobaud mode, \B0, \B1, and \P1 will not be detected automatically. The combination of \B2 and \P3 will be detected. This is compatible with seven data bits, no parity, two stop bits. Seven data bits, no parity, one stop bit may be forced by sending AT\T17\B1.
2. The autobaud feature does not detect this rate.
3. Default is \T16 if a pulldown is connected to pin 16; otherwise, the default is \T9.

Table 12. Result Codes[1]

Numeric[2]	Meaning	Verbal Response	X0	X1	X2	X3	X4	X5
0	Command was successful	OK	X	X	X	X	X	X
1	Link established at 300 bps or higher	CONNECT	X	X	X	X	X	X
2	Incoming ring detected	RING	X	X	X	X	X	X
3	Link dropped	NO CARRIER	X	X	X	X	X	X
4	Command failed	ERROR	X	X	X	X	X	X
5	Link establish at 1200	CONNECT 1200		X	X	X	X	X
6	Dial tone not present	NO DIALTONE			X		X	X
7	Line busy	BUSY				X	X	X
9	Ringback detected	RINGING						X
10	Link established at 2400	CONNECT 2400		X	X	X	X	X
30	Caller ID mark detected	CIDM	X	X	X	X	X	X
31	Hookswitch flash detected	FLASH	X	X	X	X	X	X
32	UK CID State Tone Alert Signal detected	STAS	X	X	X	X	X	X
33	Overcurrent condition	X[3]	X	X	X	X	X	X
40	Blacklist is full	BLACKLIST FULL (enabled via S42 register)	X	X	X	X	X	X
41	Attempted number is black-listed.	BLACKLISTED (enabled via S42 register)	X	X	X	X	X	X
42	No phone line present	NO LINE (enabled via %Vn commands)	X	X	X	X	X	X
43	Telephone line is in use	LINE IN USE (enabled via %Vn commands)	X	X	X	X	X	X
44	A polarity reversal was detected	POLARITY REVERSAL (enabled via G modifier)	X	X	X	X	X	X
45	A polarity reversal was NOT detected	NO POLARITY REVERSAL (enabled via G modifier)	X	X	X	X	X	X
70	No protocol	PROTOCOL: NONE	Set with \V command.					
75	Link established at 75	CONNECT 75		X	X	X	X	X
77	V.42 protocol	PROTOCOL: V42	Set with \V command.					
80	MNP2 protocol	PROTOCOL: ALTERNATE, + CLASS 2	Set with \V command.					
81	MNP3 protocol	PROTOCOL: ALTERNATE, + CLASS 3	Set with \V command.					
82	MNP4 protocol	PROTOCOL: ALTERNATE, + CLASS 4	Set with \V command.					
102	DTMF dial attempted on a pulse dial only line	UNOBTAINABLE NUMBER	X	X	X	X	X	X

Notes:
1. The connect messages shown in this table are sent when link negotiation is complete.
2. Numeric result codes are of the format: Result code <CR>.
3. X is the only verbal response code that does not follow the <CR><LF>Result Code<CR><LF> standard. There is no leading <CR><LF>.

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5. S-Registers

The S command allows reading (Sn?) or writing (Sn=x) the S-registers. The S-registers store values for functions that, typically, are rarely changed, such as timers or counters, and the ASCII values of control characters, such as carriage return. Table 13 summarizes the S-register set.

Table 13. S-Register Descriptions

S-Register (Decimal)	Function	Default (Decimal)	Range	Units
	Definition			
0	Automatic answer—Number of rings the Si2403 must detect before answering a call. 0 disables auto answer.	0	0–255	Rings
1	Ring counter.	0	0–255	Rings
2	ESC code character.	43 (+)	0–255	ASCII
3	Carriage return character.	13 (CR)	0–255	ASCII
4	Linefeed character.	10 (LF)	0–255	ASCII
5	Backspace character.	08 (BS)	0–255	ASCII
6	Dial tone wait timer—Number of seconds the Si2403 waits before blind dialing. Only applicable if blind dialing is enabled (X0, X1, X3).	02	0–255	seconds
7	Carrier wait timer—Number of seconds the Si2403 waits for carrier before timing out. This register also sets the number of seconds the modem waits for ring-back when originating a call before hanging up. This register also sets the number of seconds the answer tone will continue while using the AT*Y2A command.	80	0–255	seconds
8	Dial pause timer for , and < dial command modifiers.	02	0–255	seconds
9	Carrier presence timer—Time after a loss of carrier that a carrier must be detected before reactivating DCD. S9 is referred to as "carrier loss debounce time."	06	1–255	0.1 seconds
10	Carrier loss timer—Time the carrier must be lost before the Si2403 disconnects. Setting 255 disables disconnect entirely. If S10 is less than S9, even a momentary loss of carrier causes a disconnect.	14	1–255	0.1 seconds
12	Escape code guard timer—Minimum guard time required before and after "+++" for the Si2403 to recognize a valid escape sequence.	50	1–255	0.02 seconds
14	Wait for dial tone delay value (in relation to the W dial modifier). Starts when "W" is executed in the dial string.	12	0–255	seconds
24	Sleep Inactivity Time—Sets the time that the modem operates in normal power mode with no activity on the serial port, parallel port, or telephone line before entering low-power sleep mode. This feature is disabled if the timer is set to 0.	0	0–255	seconds

Table 13. S-Register Descriptions (Continued)

Definition				
S-Register (Decimal)	**Function**	**Default (Decimal)**	**Range**	**Units**
30	Disconnect Activity Timer—Sets the length of time that the modem stays online before disconnecting with no activity on the serial port, parallel port, or telephone line (Ring, hookswitch flash, or caller ID). This feature is disabled if set to 0.	0	0–255	minutes
38	Hang Up Delay Time—Maximum delay between receipt of ATH0 command and hang up. If time out occurs before all data can be sent, the NO CARRIER (3) result code is sent (operates in V.42 mode only). "OK" response is sent if all data is transmitted before timeout. S38 = 255 disables timeout and modem disconnects only if data is successfully sent or carrier is lost.	20	0–255	seconds
40	Data Pattern - Data pattern generated during &T4 and &T5 transmit tests. **0 – All spaces (0s)** 1 – All marks (1s) 2 – Random data	0	0–2	—
42	Blacklisting - The Si2403 will not dial the same number more than three times in three minutes. An attempt to dial a fourth time within three minutes will result in a "BLACKLISTED" result code. If the blacklist memory is full, any dial to a new number will result in a "BLACKLIST FULL" result code. Numbers are added to the blacklist only if the modem connection fails. The %B command will list the numbers on the blacklists. **0: disabled** 1: enabled	0 (disabled)	0–1	—
43	Dial Attempts to Blacklist. When blacklisting is enabled with S42, this value controls the number of dial attempts that will result in a number being blacklisted.	4	0–4	—
44	Blacklist Timer. Period during which blacklisting is active	180	0–255	seconds
50	Minimum On-Hook Time—Modem will remain on-hook for S50 seconds. Any attempt to go off-hook will be delayed until this timer expires.	3	0–255	seconds
51	Number to start checking for an outside line on a PBX.	1	0–9	—

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6. User-Access Registers (U-Registers)

The :U AT command is used to write these 16-bit U-registers, and the :R command is used to read them. U-registers are identified by a hexidecimal (hex) address.

Table 14. U-Register Descriptions

Register	Name	Description	Default
U00	DT1A0	DT1 registers set the coefficients for stage 1 of the Dial Tone Detect filter. Default is for FCC countries. See "AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer's Guide" for other country settings.	0x0800
U01	DT1B1		0x0000
U02	DT1B2		0x0000
U03	DT1A2		0x0000
U04	DT1A1		0x0000
U05	DT2A0	Dial tone detect filters stage 2 biquad coefficients.	0x00A0
U06	DT2B1		0x6EF1
U07	DT2B2		0xC4F4
U08	DT2A2		0xC000
U09	DT2A1		0x0000
U0A	DT3A0	Dial tone detect filters stage 3 biquad coefficients.	0x00A0
U0B	DT3B1		0x78B0
U0C	DT3B2		0xC305
U0D	DT3A2		0x4000
U0E	DT3A1		0xB50A
U0F	DT4A0	Dial tone detect filters stage 4 biquad coefficients.	0x0400
U10	DT4B1		0x70D2
U11	DT4B2		0xC830
U12	DT4A2		0x4000
U13	DT4A1		0x80E2
U14	DTK	Dial tone detect filter output scaler.	0x0009
U15	DTON	Dial tone detect ON threshold.	0x00A0
U16	DTOF	Dial tone detect OFF threshold.	0x0070

Table 14. U-Register Descriptions (Continued)

Register	Name	Description	Default
U17	BT1A0	BT1 registers set the coefficients for stage 1 of the Busy Tone Detect filter. Default is for FCC countries. See AN70 for other country settings.	0x0800
U18	BT1B1		0x0000
U19	BT1B2		0x0000
U1A	BT1A2		0x0000
U1B	BT1A1		0x0000
U1C	BT2A0	Busy tone detect filter stage 2 biquad coefficients.	0x00A0
U1D	BT2B1		0x6EF1
U1E	BT2B2		0xC4F4
U1F	BT2A2		0xC000
U20	BT2A1		0x0000
U21	BT3A0	Busy tone detect filter stage 3 biquad coefficients.	0x00A0
U22	BT3B1		0x78B0
U23	BT3B2		0xC305
U24	BT3A2		0x4000
U25	BT3A1		0xB50A
U26	BT4A0	Busy tone detect filter stage 4 biquad coefficients.	0x0400
U27	BT4B1		0x70D2
U28	BT4B2		0xC830
U29	BT4A2		0x4000
U2A	BT4A1		0x80E2
U2B	BTK	Busy tone detect filter output scaler.	0x0009
U2C	BTON	Busy tone detect ON threshold.	0x00A0
U2D	BTOF	Busy tone detect OFF threshold.	0x0070
U2E	BMTT	Busy cadence minimum total time in seconds multiplied by 7200.	0x0870
U2F	BDLT	Busy cadence delta in seconds multiplied by 7200.	0x25F8
U30	BMOT	Busy cadence minimum on time in seconds multiplied by 7200.	0x0438
U31	RMTT	Ringback cadence minimum total time in seconds multiplied by 7200.	0x4650
U32	RDLT	Ringback cadence delta in seconds multiplied by 7200.	0xEF10
U33	RMOT	Ringback cadence minimum on time in seconds multiplied by 7200.	0x1200
U34	DTWD	Window to look for dialtone in seconds multiplied by 1000.	0x1B58

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Table 14. U-Register Descriptions (Continued)

Register	Name	Description	Default
U35	DMOT	Minimum dialtone on time in seconds multiplied by 7200.	0x2D00
U37	PD0	Number of pulses to dial 0.	0x000A
U38	PD1	Number of pulses to dial 1.	0x0001
U39	PD2	Number of pulses to dial 2.	0x0002
U3A	PD3	Number of pulses to dial 3.	0x0003
U3B	PD4	Number of pulses to dial 4.	0x0004
U3C	PD5	Number of pulses to dial 5.	0x0005
U3D	PD6	Number of pulses to dial 6.	0x0006
U3E	PD7	Number of pulses to dial 7.	0x0007
U3F	PD8	Number of pulses to dial 8.	0x0008
U40	PD9	Number of pulses to dial 9.	0x0009
U42	PDBT	Pulse dial break time (ms units).	0x003D
U43	PDMT	Pulse dial make time (ms units).	0x0027
U45	PDIT	Pulse dial interdigit time (ms units).	0x0320
U46	DTPL	DTMF power level—16-bit format is 0x0(H)(L)0 where H is the (–)dBm level of the high-frequency DTMF tone, and L is the (–)dBm level of the low-frequency DTMF tone. Note that twist may be specified here.	0x09B0
U47	DTNT	DTMF on time (ms units).	0x0064
U48	DTFT	DTMF off time (ms units).	0x0064
U49	RGFH	Ring frequency high—Maximum frequency ring to be considered a valid ring. RGFH = 2400/(maximum ring frequency).	0x0022
U4A	RGFD	Ring delta $$RGFD \ = \ 2400Hz \times \left[\left(\frac{1}{\text{min ring freq (Hz)}}\right) - \left(\frac{1}{\text{max ring freq (Hz)}}\right)\right]$$	0x007A
U4B	RGMN	Ring cadence minimum ON time in seconds multiplied by 2400.	0x0258
U4C	RGNX	Ring cadence maximum total time in seconds multiplied by 2400.	0x6720
U4D	MOD1	This is a bit-mapped register.	0x0000
U4E	PRDD	Pre-dial delay-time after ATD command that modem waits to dial (ms units). The Si2403 stays on-hook during this time.	0x0000
U4F	FHT	Flash Hook Time. Time corresponding with "!" or "&" dial modifier that the Si2403 goes on-hook during a flash hook (ms units).	0x01F4
U50	LCDN	Loop current debounce on time (ms units).	0x015E

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Table 14. U-Register Descriptions (Continued)

Register	Name	Description	Default
U51	LCDF	Loop current debounce off time (ms units).	0x00C8
U52	XMTL	Transmit level (1 dB units)—Sets the modem data pump transmitter level. Default level of 0 corresponds to –9.85 dBm. Transmit level = –(9.85 + XMTL) dBm. Range = –9.85 to –48.	0x0000
U53	MOD2	This is a bit-mapped register.	0x0000
U62	DAAC1	This is a bit-mapped register.	0x0804
U65	DAAC4	This is a bit-mapped register.	0x00E0
U66	DAAC5	This is a bit-mapped register.	0x0049
U67	ITC1	This is a bit-mapped register.	0x0008
U68	ITC2	This is a bit-mapped register.	0x0000
U69	ITC3	This is a bit-mapped register.	0x0006
U6A	ITC4	This is a bit-mapped register.	n/a
U6E	CK1	This is a bit-mapped register.	0x1F20
U6F	PTMR	This is a bit-mapped register.	0x00FF
U70	IO0	This is a bit-mapped register.	0x2700
U76	GEN1	This is a bit-mapped register.	0x3240
U77	GEN2	This is a bit-mapped register.	0x401E
U78	GEN3	This is a bit-mapped register.	0x0000
U79	GEN4	This is a bit-mapped register.	
U7A	GENA	This is a bit-mapped register.	0x0000
U7C	GENC	This is a bit-mapped register.	0x0000
U7D	GEND	This is a bit-mapped register.	0x0000
U83	NOLN	No-Line threshold. If %V1 is set, NOLN sets the threshold for determination of line present vs. line not present.	0x0001
U84	LIUS	Line-in-use threshold. If %V1 is set, LIUS sets the threshold for determination of line in use vs. line not in use.	0x0007
U85	NLIU	Line-in-use/No line threshold. If %V2 is set, NLIU sets the threshold reference for the adaptive algorithm (see %V2).	0x0000

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Table 15. Bit-Mapped U-Register Summary

Reg.	Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
U4D	MOD1		TOCT		NHFP	NHFD	CLPD		FTP	SPDM		GT18	GT55	CTE		LLC	LCN
U53	MOD2	REV															
U62	DAAC1														FOH	DL	
U65	DAAC4	PWM	PWMG	PDN									PDL				
U66	DAAC5										FDT						
U67	ITC1									OFF	OHS	ACT		DCT[1:0]		RZ	RT
U68	ITC2											LIM			BTE	ROV	BTD
U69	ITC3										DIAL	FJM	VOL	FLVM	MODE		
U6A	ITC4														OVL		
U6E	CK1					R1[4:0]											
U6F	PTME								PTMR[7:0]								
U70	IO0	HES		TES	CIDM	OCDM	PPDM	RIM	DCDM				CID	OCD	PPD	RI	DCD
U76	GEN1	OHSR[6:0]							FACL	DCL[2:0]			ACL[4:0]				
U77	GEN2	IST[3:0]				HOI		AOC	OHT[8:0]								
U78	GEN3	IB[1:0]								IS[7:0]							
U79	GEN4												LVCS[4:0]				
U7A	GENA									DOP	ADD					HDLC	FAST
U7C	GENC												RIGPO				RIGPOEN
U7D	GEND			LVFF			LLV	AUSDC								ATZD	FDP

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6.1. Bit-Mapped U-Register Detail (Defaults in Bold)

U4D MOD1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		TOCT		NHFP	NHFD	CLPD		FTP	SPDM		GT18	GT55	CTE		LLC	LCN
Type		R/W		R/W	R/W	R/W		R/W	R/W		R/W	R/W	R/W		R/W	R/W

Reset settings = 0x0000

Bit	Name	Function
15	Reserved	Read returns zero.
14	TOCT	**Turn Off Calling Tone.** **0 = Disable.** 1 = Enable.
13	Reserved	Read returns zero.
12	NHFP	**No Hook Flash Pulse.** **0 = Disable.** 1 = Enable.
11	NHFD	**No Hook Flash Dial.** **0 = Disable.** 1 = Enable.
10	CLPD	**Check Loop Current Before Dialing.** **0 = Ignore.** 1 = Check.
9	Reserved	Read returns zero.
8	FTP	**Force Tone or Pulse.** **0 = Disable.** 1 = Enable.
7	SPDM	**Skip Pulse Dial Modifier.** **0 = No.** 1 = Yes.
6	Reserved	Read returns zero.
5	GT18	**1800 Hz Guard Tone Enable.** **0 = Disable.** 1 = Enable.
4	GT55	**550 Hz Guard Tone Enable.** **0 = Disable.** 1 = Enable.
3	CTE	**Calling Tone Enable.** **0 = Disable.** 1 = Enable.
2	Reserved	Read returns zero.

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Bit	Name	Function
1	LLC	**Low Loop Current Detect (required for CTR21).** **0 = Disabled.** 1 = Enabled.
0	LCN	**Loop Current Needed.** **0 = No.** 1 = Yes.

U53 MOD2

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	REV															
Type	R/W															

Reset settings = 0x0000

Bit	Name	Function
15	REV	**V.23 Reversing.** **0 = Disable.** 1 = Enable.
14:0	Reserved	Read returns zero.

U62 DAAC1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name														FOH	DL	
Type														R/W	R/W	

Reset settings = 0x0804

Bit	Name	Function
15:12	Reserved	Must be set to 0.
11	Reserved	Must be set to 1.
10:3	Reserved	Must be set to 0.
2	FOH	**Fast Off-Hook.** 0 = Automatic Calibration Time set to 426 ms **1 = Automatic Calibration Time set to 106 ms**
1	DL	**Isolation Digital Loopback (see the AT&T commands).** **0 = Loopback occurs beyond the isolation interface, out to and including the analog hybrid circuit.** 1 = Enables digital loopback mode across isolation barrier only.
0	Reserved	Must be set to 0.

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U65 DAAC4

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PWM	PWMG	PDN									PDL				
Type	R/W	R/W	R/W									R/W				

Reset settings = 0x00E0

Bit	Name	Function
15	PWM	**PWM Mode.** **0 = Normal. Classic PWM output waveform.** 1 = Scrambled mode. Low-distortion mode if used with output circuit shown in "AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer's Guide".
14	PWMG	**PWM Gain.** **0 = No gain.** 1 = 6 dB gain applied to AOUT.
13	PDN	**Powerdown.** Completely powerdown the Si2403 and Si3015. Once set to 1, the Si2403 must be reset to power on. **0 = Normal.** 1 = Powerdown.
12:8	Reserved	Read returns zero.
7:5	Reserved	Must not change in a read-modify-write.
4	PDL*	**Powerdown Line-Side Chip.** **0 = Normal operation.** 1 = Places the Si3015 in powerdown mode.
3:0	Reserved	Must not change in a read-modify-write.
*Note: Typically used only for board-level debug.		

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U66 DAAC5

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name										FDT						
Type	R															

Reset settings = 0x0049

Bit	Name	Function
15:7	Reserved	Read returns zero.
6	FDT*	**Frame Detect.** 0 = Indicates isolation link has not established frame lock. 1 = Indicates isolation link frame lock has been established.
5:4	Reserved	Read returns zero.
3:0	Reserved	Do not modify.
*Note: Typically used only for board-level debug.		

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Si2403

U67 ITC1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name									OFF	OHS	ACT		DCT[1:0]		RZ	RT
Type									R/W	R/W	R/W		R/W		R/W	R/W

Reset settings = 0x0008

Bit	Name	Function
15:8	Reserved	Read returns zero.
7	OFF	**DC Termination Off.** **0 = Normal operation.** The OFF bit must always be set to 0 when on-hook. 1 = DC termination disabled and the device presents an 800 Ω dc impedance to the line, which is used to enhance operation with an off-hook parallel phone.
6	OHS	**On-Hook Speed.** **0 = The Si2403 will execute a fast on-hook.** 1 = The Si2403 will execute a slow controlled on-hook.
5	ACT	**AC Termination Select.** **0 = Selects the real impedance.** 1 = Selects the complex impedance.
4	Reserved	Read returns zero.
3:2	DCT[1:0]	**DC Termination Select.** 00 = Low-voltage mode (Transmit level = −13.85 dBm). 01 = Japan mode (Transmit level = −11.85 dBm). **10 = FCC mode. Standard voltage mode (Transmit level = −9.85 dBm).** 11 = CTR21 mode. Current limiting mode (Transmit level = −9.85 dBm).
1	RZ	**Ringer Impedance.** **0 = Maximum (high) ringer impedance.** 1 = Synthesize ringer impedance. C15, R14, Z2, and Z3 must not be installed when setting this bit. See the "Ringer Impedance" section in "AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer's Guide".
0	RT	**Ringer Threshold Select.** Used to satisfy country requirements on ring detection. Signals below the lower level do not generate a ring detection; signals above the upper level are guaranteed to generate a ring detection. **0 = 11 to 22 V_{rms}.** 1 = 17 to 33 V_{rms}.

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U68 ITC2

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name												LIM		BTE	ROV	BTD
Type												R/W		R/W	R/W	R/W

Reset settings = 0x0000

Bit	Name	Function
15:8	Reserved	Read returns zero.
7:5	Reserved	Do not modify.
4	LIM	**Current Limit.** **0 = All other modes.** 1 = CTR21 mode.
3	Reserved	Do not modify.
2	BTE	**Billing Tone Protect Enable.** **0 = Disabled.** 1 = Enabled. When set, the DAA responds automatically to a collapse of the line-derived power supply during a billing tone event. When off-hook, if BTE = 1 and BTD goes high, the dc termination is released (800 Ω presented to line). If BTE and RIM (U70, bit 9) are set, an RI (U70, bit 1) interrupt also occurs when BTD goes high.
1	ROV	**Receive Overload.** The bit is set when the receive input (i.e., receive pin goes below ground) has an excessive input level. This bit is cleared by writing a 0 to this location. **0 = Normal receive input level.** 1 = Excessive receive input level.
0	BTD	**Billing Tone Detected.** This bit is set if a billing tone is detected. This bit is cleared by writing a 0 to this location. 0 = No billing tone. 1 = Billing tone detected.

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Si2403

U69 ITC3

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name										DIAL	FJM	VOL	FLVM	MODE		
Type										R/W	R/W	R/W	R/W	R/W		

Reset settings = 0x0006

Bit	Name	Function
15:8	Reserved	Read returns zero.
7	Reserved	Do not modify. Must be set to zero.
6	DIAL	**DTMF Dialing Mode.** This bit should be set during DTMF dialing in CTR21 mode if LVCS < 12. **0 = Normal operation.** 1 = Increase headroom for DTMF dialing.
5	FJM	**Force Japan DC Termination Mode.** **0 = Normal Gain.** 1 = When DCT = 2 (FCC mode), setting this bit forces Japan dc termination mode while allowing for a transmit level of –1 dBm. See the "DTMF Dialing" section in "AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer's Guide".
4	VOL	**Line Voltage Adjust.** When set, this bit adjusts the TIP-RING line voltage. Lowering this voltage improves margin in low-voltage countries. Raising this voltage may improve large-signal distortion performance. **0 = Normal operation.** 1 = Lower DCT voltage.
3	FLVM	**Force Low Voltage Mode.** When DCT (U67, bits 3:2) = 10 (FCC mode), setting FLVM forces the low-voltage mode (see DCT = 00) while allowing for a transmit level of –1 dBm. **0 = Disable.** 1 = Enable.
2	MODE	**Mode.** This bit enables on-hook line monitoring. It is automatically set while on-hook and cleared while off-hook.
1:0	Reserved	Do not modify.

U6A ITC4

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name														OVL		
Type														R		

Reset settings = N/A

Bit	Name	Function
15:3	Reserved	Read returns zero.
2	OVL	**Overload Detected.** This bit has the same function as ROV but clears itself after the overload has been removed. See the "Billing Tone Detection" section in "AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer's Guide". This bit is not affected by the BTE bit.
1:0	Reserved	Do not modify.

U6E CK1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name				R1[4:0]												
Type	R/W								R/W							

Reset settings = 0x1F20

Bit	Name	Function
15:13	Reserved	Do not modify.
12:8	R1*[4:0]	**R1** **CLKOUT Divider** 0 CLKOUT off. R1 R1 + 1 (default R1 = 31; 2.4576 MHz). R1 = 31 required for proper codec interface operation.
7:0	Reserved	Do not modify.
Note: See Figure 5 on page 17.		

SILICON LABORATORIES

U6F PTMR

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name									PTMR[7:0]							
Type									R/W							

Reset settings = 0x00FF

Bit	Name	Function
15:8	Reserved	Do not modify
7:0	PTMR[7:0]	Parallel Port Receive FIFO Interrupt Timer (msec units). See "AN70: Si2456/Si2433/Si2414/Si2403 Modem Designer's Guide" for more details.

SILICON LABORATORIES

U70 IO0

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	HES		TES	CIDM	OCDM	PPDM	RIM	DCDM				CID	OCD	PPD	RI	DCD
Type	R/W		R/W	R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W	R/W

Reset settings = 0x2700

Bit	Name	Function
15	HES	**Hardware Escape Pin.** **0 = Disable.** 1 = Enable.
14	Reserved	Read returns zero.
13	TES	**Enable "+++" Escape.** 0 = Disable. **1 = Enable.**
12	CIDM	**Caller ID Mask.** **0 = Change in CID will not affect INT.** 1 = A low-to-high transition in CID activates $\overline{\text{INT}}$.
11	OCDM	**Overcurrent Detect Mask.** **0 = Change in OCD does not affect INT.** ("X" result code is not generated in command mode.) 1 = A low-to-high transition in OCD will activate INT. ("X" result code is generated in command mode.)
10	PPDM	**Parallel Phone Detect Mask.** 0 = Change in PPD does not affect $\overline{\text{INT}}$. **1 = A low-to-high transition in PPD will activate INT.**
9	RIM	**Ring Indicator.** 0 = Change in RI does not affect $\overline{\text{INT}}$. **1 = A low-to-high transition in RI activates INT.**
8	DCDM	**Data Carrier Detect Mask.** 0 = Change in DCD does not affect $\overline{\text{INT}}$. **1 = A high-to-low transition in DCD (U70, bit 0), which indicates loss of carrier, activates INT.**
7	Reserved	Must be set to zero.
6:5	Reserved	Read returns zero.
4	CID	**Caller ID (sticky).** Caller ID preamble has been detected; data will soon follow. Clears on :I read.
3	OCD	**Overcurrent Detect (sticky).** Overcurrent condition has occurred. Clears on :I read.
2	PPD	**Parallel Phone Detect (sticky).** Parallel phone detected since last off-hook event. Clears on :I read.
1	RI	**Ring Indicator.** Active high bit when the Si2403 is on-hook indicates ring event has occurred. Clears on :I read.
0	DCD	**Data Carrier Detect (status).** Active high bit indicates carrier detected (equivalent to inverse of $\overline{\text{DCD}}$ pin).

SILICON LABORATORIES

Si2403

U76 GEN1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name				OHSR[6:0]				FACL		DCL[2:0]				ACL[4:0]		
Type				R/W				R/W		R/W				R/W		

Reset settings = 0x3240

Bit	Name	Function
15:9	OHSR[6:0]	**Off-Hook Sample Rate (40 ms units)** Sets the sample rate for the off-hook intrusion algorithms (1 second default).
8	FACL	**Force ACL.** **0 = While off-hook, ACL is automatically updated with LVCS.** 1 = While off-hook, ACL does not change from the value written to it while on-hook.
7:5	DCL[2:0]	**Differential Current Level (3 mA units).** Sets the differential level between ACL and LVCS that will trigger an off-hook PPD interrupt (default = 2).
4:0	ACL[4:0]	**Absolute Current Level (3 mA units, see Figure 7 on page 19).** ACL represents the value of LVCS current when the Si2403 is off-hook and all parallel phones are on-hook. If ACL = 0, it is ignored by the off-hook intrusion algorithm.The Si2403 will also write ACL with the contents of LVCS before an intrusion and before going on-hook (default = 0).

SILICON LABORATORIES

U77 GEN2

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	IST[3:0]				HOI		AOC		OHT[8:0]							
Type	R/W				R/W		R/W		R/W							

Reset settings = 0x401E

Bit	Name	Function
15:12	IST[3:0]	**Intrusion Settling Time (250 ms units).** Delay between the time the Si2403 goes off-hook and the time the off-hook intrusion algorithm begins. Default is 1 s.
11	HOI	**Hang-Up On Intrusion.** **0 = Si2403 will not automatically hang up when an off-hook PPD interrupt occurs.** 1 = Si2403 automatically hangs up on a PPD interrupt. If %Vn commands are set, HOI also causes the "LINE IN USE" result code upon PPD interrupt.
10	Reserved	Read returns zero.
9	AOC	**Overcurrent Detection.** Enable Overcurrent Detection. **0 = Disable.** 1 = Enable. **Note:** AOC may falsely detect an overcurrent condition in the presence of line reversals or other transients. Therefore, this feature should not be used in applications or locations, such as Japan, where line reversals are common or may be expected.
8:0	OHT[8:0]	**Off-Hook Time (1 ms units).** Time before LVCS is checked for overcurrent condition after going off-hook (30 ms default).

SILICON LABORATORIES

U78 GEN3

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	IB[1:0]								IS[7:0]							
Type	R/W								R/W							

Reset settings = 0x0000

Bit	Name	Function
15:14	IB[1:0]	**Intrusion Blocking.** Defines the method used to block the off-hook intrusion algorithm from operation after dialing has begun. **0 = No intrusion blocking.** 1 = Intrusion disabled from start of dial to end of dial. 2 = Intrusion disabled from start of dial to IS register time-out. 3 = Intrusion disabled from start of dial to connect ("CONNECT XXX", "NO DIALTONE", or "NO CARRIER").
13:8	Reserved	Read returns zero.
7:0	IS[7:0]	**Intrusion Suspend (500 ms units).** When IB = 2, this register sets the length of time, starting when dialing begins, that the off-hook intrusion algorithm is blocked (suspended) (default = 00000000$_b$).

SILICON LABORATORIES

U79 GEN4

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name													LVCS[4:0]			
Type													R			

Bit	Name	Function
15:5	Reserved	Read returns zero.
4:0	LVCS[4:0]	**Line Voltage Current Sense.** Represents either the line voltage, loop current, or on-hook line monitor depending on the state of the MODE, OFHK, and ONHM bits. **On-Hook Voltage Monitor (2.75 V/bit ±20%) (see Figure 6 on page 19).** 00000 = No line connected. 00001 = Minimum line voltage (V_{MIN} = 3.0 V ± 0.5 V). 11111 = Maximum line voltage (87 V ± 20%). The line voltage monitor full scale may be modified by changing R5 as follows: $V_{MAX} = V_{MIN} + 4.2$ (10M + R5 + 1.6k)/(R5 +1.6k)/5 U69[2] (MODE) must be set to 1_b before reading LVCS while the Si2403 is on-hook. See MODE on page 46. U69[2] (MODE) must be disabled (MODE = 0_b) before the Si2403 can go off-hook, dial, or answer a call. **Off-Hook Loop Current Monitor (3 mA/bit) (see Figure 7 on page 19).** 00000 = No loop current. 00001 = Minimum loop current. 11110 = Maximum loop current. 11111 = Loop current is excessive (overload). Overload > 140 mA in all modes except CTR21 Overload > 54 mA in CTR21 mode

SILICON LABORATORIES

Si2403

U7A GENA

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name									DOP	ADD					HDLC	FAST
Type									R/W	R/W					R/W	R/W

Reset settings = 0x0000

Bit	Name	Function
15:8	Reserved	Read returns to zero.
7	DOP	**Dial or Pulse.** **0 = Normal ATDTW operation** 1 = Use ATDTW for Pulse/Tone Dial Detection (see also ATDW command)
6	ADD	**Adaptive Dialing.** 1 = Enable **0 = Disable** Attempt DTMF dial, then fall back to pulse dialing if unsuccessful. First digit is dialed as DTMF. If a dialtone is still present after two seconds, the Si2403 will redial the first digit and remaining digits as pulse. If a dialtone is not present after two seconds, the Si2403 will dial the remaining digits as DTMF.
5:2	Reserved	Read returns to zero.
1	HDLC	**Synchronous Mode.*** **0 = Normal asynchronous mode.** 1 = Transparent HDLC mode.
0	FAST	**Fast Connect.*** **0 = Normal modem handshake timing per ITU/Bellcore standards.** 1 = Fast connect modem handshake timing.
*Note: When V22HD, HDLC, or FAST bits are set, \N0 (wire mode) must be used.		

SILICON LABORATORIES

U7C GENC

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name												RIGPO				RIGPOEN
Type												R				R/W

Reset settings = 0x0000

Bit	Name	Function
15:5	Reserved	Reads returns to zero.
4	RIGPO	**RI.** RI (pin 15), follows this bit when RIGPIOEN = 1_b.
3:1	Reserved	Reads returns to zero.
0	RIGPOEN	**0 = RI indicates valid ring signal (Normal ring-indicator mode).** 1 = RI (Pin 15) can be used as a general-purpose output and follows U7C[4] (RIGPO).

SILICON LABORATORIES

U7D GEND

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name			LVFE			LLV	AUSDC								ATZD	FDP
Type			R/W			R/W	R/W								R/W	R/W

Reset settings = 0x0000

Bit	Name	Function
15:14	Reserved	Reads returns to zero.
13	LVFE	**LVCS Filter Enable.** **0 = Normal operation** 1 = Enables optional filtering on LVCS to mitigate the effect of 50/60 Hz noise on tip/ring voltage.
12:11	Reserved	Read returns zero.
10	LLV	**0 = Normal operation.** 1 = Enables an optional algorithm for countries, such as Japan and Malaysia, with low loop voltage. Also set U67[3:2] (DCT) = 00_b, U69[4] VOL = 1_b, and U52 = 0x0002 before going off-hook. When the modem goes off-hook, it samples LVCS and changes DCT and VOL as necessary to maximize transmit levels and optimize distortion.
9	AUSDC	**0 = Normal operation.** 1 = Causes the modem to go off-hook in Japan mode and then revert to FCC mode after 500 ms. This allows the modem to meet the Australian line seizure requirements while allowing the maximum transmit power (optional for Australia and when DCT = 01_b).
8:2	Reserved	Reads returns to zero.
1	ATZD	**ATZ Disable.** **0 = ATZ functions normally.** 1 = Disable ATZ command. This may be used to ensure modem settings are not lost in some systems.
0	FDP	**FSK Data Processing.** **0 = FSK data processing stops when carrier is lost.** 1 = FSK data processing continued for 2 bytes after carrier is lost.

SILICON LABORATORIES

7. Parallel Interface Registers

Parallel Interface 0 (0x00)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TX/RX							
Type	R/W							

Reset settings = 0x00

Bit	Name	Function
7:0	TX/RX	**Parallel Interface Transmit/Receive.** This register functions similarly to the serial port TX pin on writes to the parallel port, and similarly to the serial port RX pin on reads from the parallel port.

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Parallel Interface 1 (0x01)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RXF	TXE	REM	INTM	INT	ESC	$\overline{\text{RTS}}$	$\overline{\text{CTS}}$
Type	R	R	R	R/W	R	R/W	R/W	R

Reset settings = 0110_0011

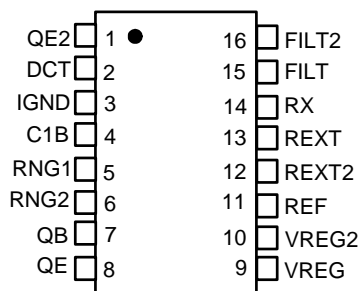| Bit	Name	Function
7	RXF	**Receive FIFO Almost Full (status).** 0 = Receive FIFO (12 deep) contains three or more empty locations (RXF ≤ 9). The host can clear the RXF interrupt without emptying the RX FIFO by writing a 0 to the RXF bit. This will disable the RXF interrupt until the host has emptied the FIFO. 1 = Receive FIFO contains two or fewer empty locations (RXF ≥ 10).
6	TXE	**Transmit FIFO Almost Empty (status).** 0 = Transmit FIFO (14 deep) contains three or more characters (TXF ≥ 3). 1 = Transmit FIFO contains two or fewer characters (TXF ≤ 2). TXE interrupt will not trigger if the CTS bit is inactive. Therefore, the host does not need to poll CTS while waiting for transmit FIFO to empty. TXE can be cleared by writing it to 0.
5	REM	**Receive FIFO Empty.** 0 = Receive FIFO has valid data. 1 = Receive FIFO empty. **Note:** If the interim timer (see PTMR - U6F, bits 7:0) set by PTMR expires, it will cause an interrupt. This interrupt will not set RXF, TXE, or INT. The interrupt handler on the host should then verify that REM = 0 and begin to empty the receive FIFO (Parallel Interface 0 register) until REM = 1.
4	INTM	**Interrupt Mask.** 0 = In parallel mode, the $\overline{\text{INT}}$ pin is triggered by a rising edge on RXF or TXE only (default). 1 = In parallel mode, the $\overline{\text{INT}}$ pin is triggered by a rising edge on RXF, TXE, or INT.
3	INT	**Interrupt.** 0 = No interrupt has occurred. 1 = Indicates that an interrupt (CID, OCD, PPD, RI, or DCD from U70) has occurred. This bit is cleared via the AT:I command.
2	ESC	**Escape.** Operation of this bit in parallel mode is functionally-equivalent to the ESC pin in serial mode.
1	$\overline{\text{RTS}}$	**Request-to-Send.** Operation of this bit in parallel mode is functionally equivalent to the $\overline{\text{RTS}}$ pin in serial mode. Use of the $\overline{\text{CTS}}$ and $\overline{\text{RTS}}$ bits (as opposed to the TXE and RXF bits) allows the flow control between the host and the Si2403 to operate 1 byte at a time rather than in blocks.
0	$\overline{\text{CTS}}$	**Clear-to-Send.** Operation of this bit in parallel mode is functionally-equivalent to the $\overline{\text{CTS}}$ pin in serial mode. Use of the $\overline{\text{CTS}}$ and $\overline{\text{RTS}}$ bits (as opposed to the TXE and RXF bits) allows the flow control between the host and the Si2403 to operate 1 byte at a time, rather than in blocks.

SILICON LABORATORIES

8. Pin Descriptions: Si2403

```
        CLKIN/XTALI ☐ 1 ●      24 ☐ EECLK/D5
              XTALO ☐ 2         23 ☐ DCD/D4
     CLKOUT/EECS/A0 ☐ 3         22 ☐ ESC/D3
                 D6 ☐ 4         21 ☐ C1A
              VD3.3 ☐ 5         20 ☐ ISOB
                GND ☐ 6         19 ☐ VD3.3
                VDA ☐ 7         18 ☐ GND
             RTS/D7 ☐ 8         17 ☐ VDB
             RXD/RD ☐ 9         16 ☐ EESD/D2
             TXD/WR ☐ 10        15 ☐ RI/D1
             CTS/CS ☐ 11        14 ☐ INT/D0
              RESET ☐ 12        13 ☐ AOUT/INT
```
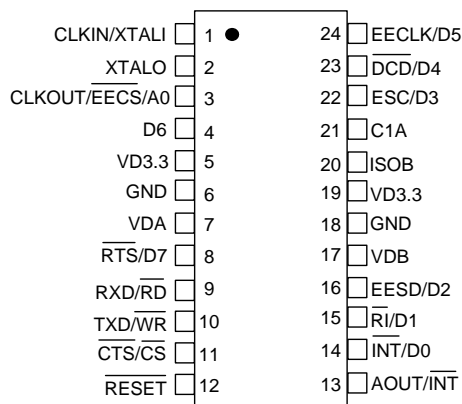
Pin #	Pin Name	Description
1	CLKIN/XTALI	**Clock Input/Crystal Oscillator Pin.** This pin provides support for parallel-resonant, AT-cut crystals. XTALI also acts as an input in the event that an external clock source is used in place of a crystal. A 4.9152 MHz crystal or 4.9152 MHz clock is required.
2	XTALO	**Crystal Oscillator Pin.** This pin provides support for parallel-resonant AT-cut crystals. XTALO serves as the output of the crystal amplifier.
3	CLKOUT/EECS/A0	**Clock Output/EEPROM Chip Select/Address Bit 0.** Clock output in serial mode. Active low read/write enable for SPI EEPROM in serial mode when pin 4 is pulled low during powerup. Address Enable in parallel mode.
4	D6	**Data Bit.** Bidirectional parallel bus data bit 6 in parallel mode.
5, 19	VD3.3	**Digital Supply Voltage.** Provides the 3.3 V digital supply voltage to the Si2403.
6, 18	GND	**Ground.** Connects to the system digital ground.
7,17	VDA, VDB	**Digital Rail.** Pin provides decoupling for the internal power supplies.
8	RTS/D7	**Request-to-Send/Data Bit.** Request-to-send (for flow control) in serial mode. Bidirectional parallel bus data bit 7 in parallel mode.
9	RXD/RD	**Receive Data/Read Enable.** Data output to DTE RXD pin in serial mode. Active low read enable pin in parallel mode.

SILICON LABORATORIES

Pin #	Pin Name	Description
10	TXD/$\overline{\text{WR}}$	**Transmit Data/Write Enable.** Data input from DTE TXD pin in serial mode. Active low write-enable pin in parallel mode.
11	$\overline{\text{CTS}}$/$\overline{\text{CS}}$	**Clear-to-Send/Chip Select.** Active low clear-to-send (for flow control) in serial mode. Active low chip select in parallel mode.
12	$\overline{\text{RESET}}$	**Reset Input.** An active low input that is used to reset all control registers to a defined initialized state.
13	AOUT/$\overline{\text{INT}}$	**Analog Output/Interrupt Output.** Analog output in serial mode. Active low interrupt output in parallel mode.
14	$\overline{\text{INT}}$/D0	**Interrupt Output/Data Bit.** Active low interrupt output in serial mode. Bidirectional parallel bus data bit 0 in parallel mode.
15	$\overline{\text{RI}}$/D1	**Ring Indicator/Data Bit.** The $\overline{\text{RI}}$ on (active low) indicates the presence of an ON segment of a ring signal on the telephone line. Bidirectional parallel bus data bit 1 in parallel mode.
16	EESD/D2	**EEPROM Serial Data Input/Output/Data Bit.** Bidirectional Input/Output to SPI EEPROM in serial mode. Bidirectional parallel bus data bit 2 in parallel mode.
20	ISOB	**Bias Voltage.** This pin provides decoupling for the power supply.
21	C1A	**Isolation Capacitor 1A.** Connects to one side of the isolation capacitor, C1.
22	ESC/D3	**Escape/Data Bit.** Hardware escape in serial mode. Bidirectional parallel bus data bit 3 in parallel mode.
23	$\overline{\text{DCD}}$/D4	**Carrier Detect/Data Bit.** Active low-carrier detect in serial mode. Bidirectional parallel bus data bit 4 in parallel mode.
24	EECLK/D5	**EEPROM Clock/Data Bit.** Clock output for SPI EEPROM in serial mode. Bidirectional parallel bus data bit 5 in parallel mode.

SILICON LABORATORIES

9. Pin Descriptions: Si3015

```
          QE2  1 ●    16  FILT2
          DCT  2       15  FILT
         IGND  3       14  RX
          C1B  4       13  REXT
         RNG1  5       12  REXT2
         RNG2  6       11  REF
           QB  7       10  VREG2
           QE  8        9  VREG
```

Pin #	Pin Name	Description
1	QE2	**Transistor Emitter 2.** Connects to the emitter of Q4.
2	DCT	**DC Termination.** Provides dc termination to the telephone network.
3	IGND	**Isolated Ground.** Connects to ground on the line-side interface. Also connects to capacitor C2.
4	C1B	**Isolation Capacitor 1B.** Connects to one side of isolation capacitor C1.
5	RNG1	**Ring 1.** Connects through a capacitor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the modem.
6	RNG2	**Ring 2.** Connects through a capacitor to the RING lead of the telephone line. Provides the ring and caller ID signals to the modem.
7	QB	**Transistor Base.** Connects to the base of transistor Q3.
8	QE	**Transistor Emitter.** Connects to the emitter of transistor Q3.
9	VREG	**Voltage Regulator.** Connects to an external capacitor to provide bypassing for an internal power supply.
10	VREG2	**Voltage Regulator 2.** Connects to an external capacitor to provide bypassing for an internal power supply.
11	REF	**Reference.** Connects to an external resistor to provide a high-accuracy reference current.
12	REXT2	**External Resistor 2.** Sets the complex ac termination impedance.

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Si2403

Pin #	Pin Name	Description
13	REXT	**External Resistor.** Sets the real ac termination impedance.
14	$\overline{\text{RX}}$	**Receive Input.** Serves as the receive side input from the telephone network.
15	FILT	**Filter.** Provides filtering for the dc termination circuits.
16	FILT2	**Filter 2.** Provides filtering for the bias circuits.

SILICON LABORATORIES

10. Ordering Guide

Chipset	Description	Digital	Line	Temperature
Si2403	Commercial	Si2403-KT	Si3015-KS	0 to 70 °C
Si2403	Commercial Pb-free	Si2403-FT	Si3015-F-FS	0 to 70 °C

11. Package Outline: 24-Pin TSSOP

Figure 8 illustrates the package details for the Si2403. Table 16 lists the values for the dimensions shown in the illustration.
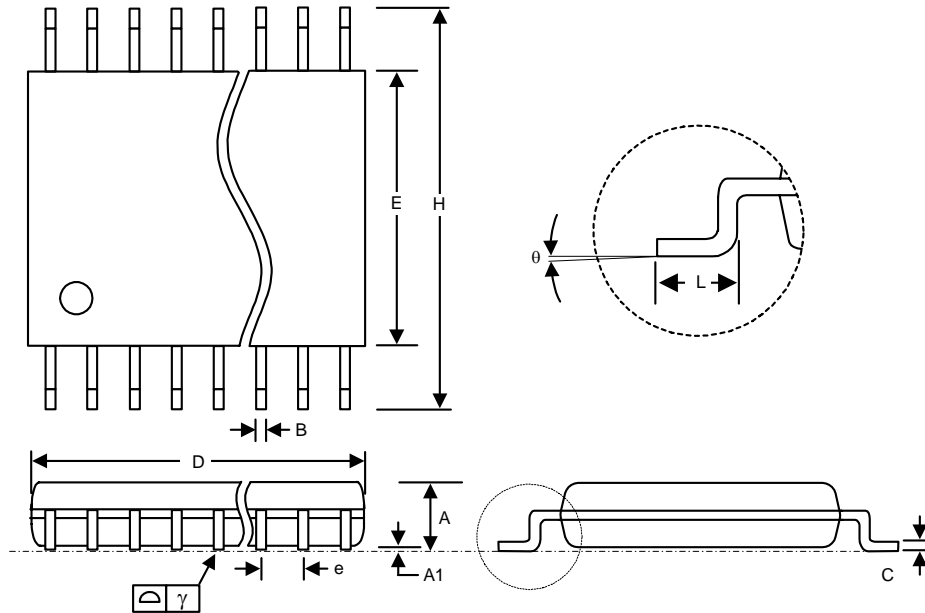
Approximate device weight is 115.7 mg.

Figure 8. 24-Pin Thin Shrink Small Outline Package (TSSOP)

Table 16. Package Diagram Dimensions

| Symbol | Millimeters | | Typical* |
	Min	Max	
A	—	1.20	✓
A1	0.05	0.15	✓
B	0.19	0.30	
C	0.09	0.20	✓
D	7.70	7.90	
E	4.30	4.50	
e	0.65 BSC		
H	6.40 BSC		
L	0.45	0.75	
θ	0°	8°	✓
γ		0.10	
*Note: To guarantee coplanarity (γ), the parameters marked "Typical" may be exceeded.			

SILICON LABORATORIES

12. Package Outline: 16-Pin SOIC

Figure 9 illustrates the package details for the Si3015. Table 17 lists the values for the dimensions shown in the illustration.
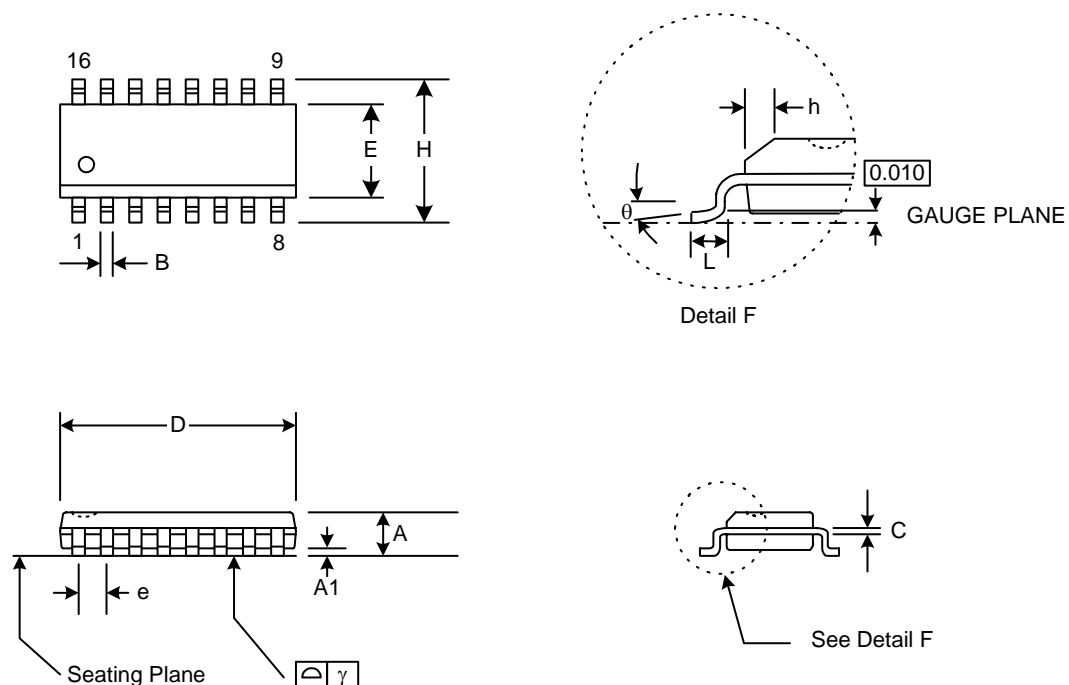
Figure 9. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 17. Package Diagram Dimensions

Symbol	Millimeters		Typical*
	Min	Max	
A	1.35	1.75	✓
A1	.10	.25	✓
B	.33	.51	
C	.19	.25	✓
D	9.80	10.00	
E	3.80	4.00	
e	1.27 BSC	—	
H	5.80	6.20	
h	.25	.50	
L	.40	1.27	
γ	—	0.10	
θ	0º	8º	✓
*Note: Typical parameters are for information purposes only.			

Si2403

DOCUMENT CHANGE LIST

Revision 1.0 to Revision 1.1

- Updated "Functional Block Diagram" on page 1.
- Updated Table 6 on page 8.
- Expanded "+GCI country codes" in Table 8 on page 21.
- Updated S-registers S43 and S44 in Table 13 on page 33.
- Updated default register value for U66.
- Updated U-register U7D.

Revision 1.1 to Revision 1.2

- Updated "Ordering Guide" on page 63.
- Updated Table 8 on page 21.
  - Updated description of I3 command.

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NOTES:

SILICON LABORATORIES

Si2403

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