

TSM052N06PQ56 60V N-Channel MOSFET



PDFN56

8

Pin Definition:

1. Source	B. Drain
2. Source	7. Drain
3. Source	6. Drain
4. Gate	5. Drain

Key Parameter Performance

Parameter	Value	Unit
V_{DS}	60	V
R _{DS(on)} (max)	5.2	mΩ
Q_g	50	nC

Features

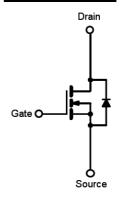
- Low On-Resistance
- Low Input Capacitance
- Low Gate Charge

Ordering Information

Part No.	Package	Packing		
TSM052N06PQ56 RLG	PDFN56	2.5kpcs / 13" Reel		

Note: "G" denotes for Halogen- and Antimony-free as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Block Diagram



N-Channel MOSFET

Absolute Maximum Ratings (Tc=25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V_{DS}	60	V	
Gate-Source Voltage		V_{GS}	±25	V	
Continuous Drain Current (Note 3)	T _C =25°C		100	А	
	T _A =25°C	I _D	17		
Drain Current-Pulsed (Note 1)		I _{DM}	350	А	
Single Pulse Avalanche Energy L=0.5mH		E _{AS}	169	mJ	
Maximum Power Dissipation (Note 2)	T _C =25°C	Б	83	W	
	T _A =25°C	- P _D	3.6		
Storage Temperature Range		T _{STG}	-55 to +150	°C	
Operating Junction Temperature Range		T _J	-55 to +150	°C	

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	R _{eJC}	1.5	°C/W
Thermal Resistance - Junction to Ambient	$R_{\Theta JA}$	35	°C/W



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Electrical Specifications (T_J=25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Тур	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV _{DSS}	60			V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 20A$	R _{DS(ON)}		4.2	5.2	mΩ
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	V _{GS(TH)}	2	3	4	V
Zero Gate Voltage Drain Current	$V_{DS} = 48V, V_{GS} = 0V$	I _{DSS}			1	μA
Gate Body Leakage	$V_{GS} = \pm 25V, V_{DS} = 0V$	I _{GSS}			±100	nA
Dynamic						
Total Gate Charge		Q_g		50		nC
Gate-Source Charge	$V_{DS} = 30V, I_{D} = 20A,$	Q _{gs}		15		
Gate-Drain Charge	$V_{GS} = 10V$	Q_{gd}		2.5		
Input Capacitance		C _{iss}		3686		
Output Capacitance	$V_{DS} = 30V, V_{GS} = 0V,$	C _{oss}		357		pF
Reverse Transfer Capacitance	f = 1.0MHz	C _{rss}		124		
Switching						•
Turn-On Delay Time		t _{d(on)}		12		
Turn-On Rise Time	$V_{GS} = 10V, V_{DS} = 30V,$	t _r		4		
Turn-Off Delay Time	$R_G = 3\Omega$, $I_D = 20A$	t _{d(off)}		50		ns
Turn-Off Fall Time		t _f		6		
Drain-Source Diode Characteristic	s and Maximum Rating				•	ľ
Drain-Source Diode Forward Voltage	V _{GS} =0V, I _S =20A	V_{SD}		0.8	1.3	V
Reverse Recovery Time	I _S = 20A, dI/dt = 100A/μs	t _{rr}		22		ns
Reverse Recovery Charge		Q_{rr}	1	120		nC

Notes:

- 1. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 2. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design. $R_{\Theta JA}$ shown below for single device operation on FR-4 PCB in still air.
- 3. The maximum current rating is limited by package.

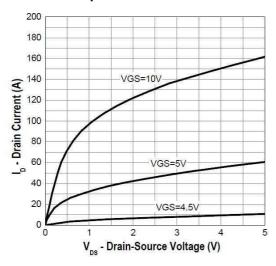


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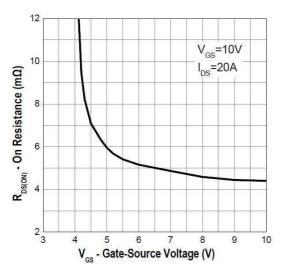
Pb ROHS COMPLIANT

Electrical Characteristics Curves

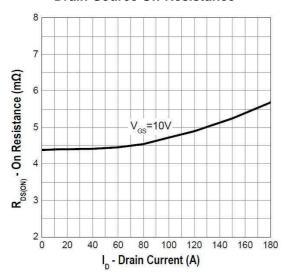
Output Characteristics



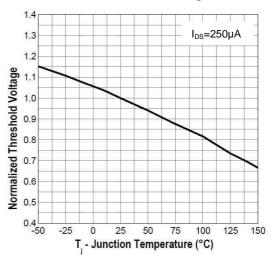
Gate Source On Resistance



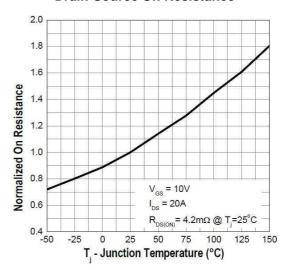
Drain-Source On-Resistance



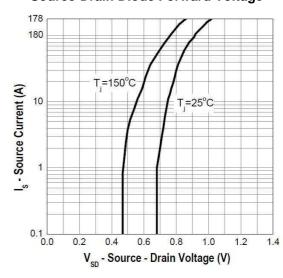
Gate Threshold Voltage



Drain-Source On Resistance



Source-Drain Diode Forward Voltage



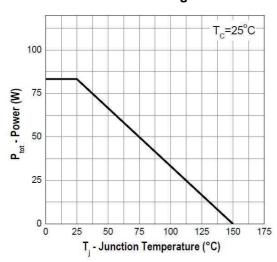


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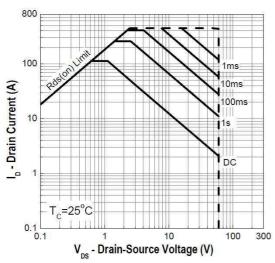
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Electrical Characteristics Curves

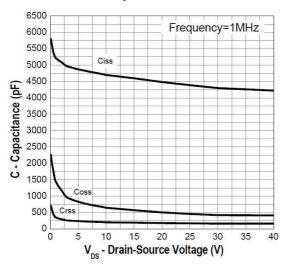
Power Derating



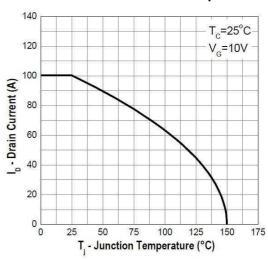
Safe Operation Area



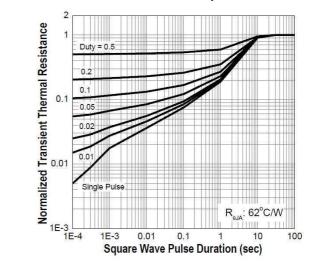
Capacitance



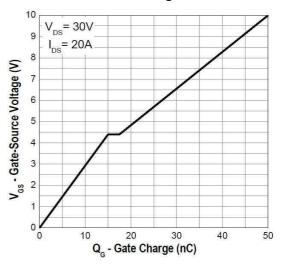
Drain Current vs. Junction Temperature



Transient Thermal Impedance



Gate Charge

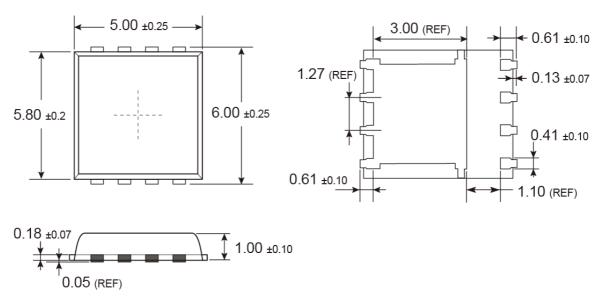




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PDFN56 Mechanical Drawing



Unit: Millimeters

Marking Diagram



Y = Year Code

M = Month Code for Halogen Free Product
(O=Jan, P=Feb, Q=Mar, R=Apl, S=May, T=Jun, U=Jul, V=Aug, W=Sep, X=Oct, Y=Nov, Z=Dec)

L = Lot Code



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