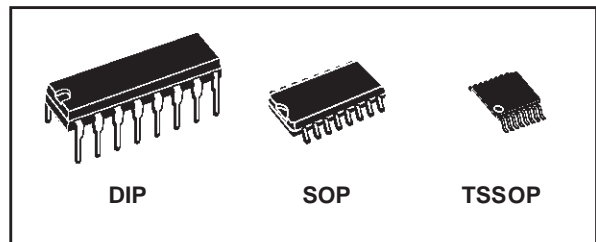# M74HC166

8 BIT PISO SHIFT REGISTER

- **HIGH SPEED :**
  f_{MAX} = 63 MHz (TYP.) at V_{CC} = 6V
- **LOW POWER DISSIPATION:**
  I_{CC} =4µA(MAX.) at T_A=25°C
- **HIGH NOISE IMMUNITY:**
  V_{NIH} = V_{NIL} = 28 % V_{CC} (MIN.)
- **SYMMETRICAL OUTPUT IMPEDANCE:**
  $|I_{OH}|$ = I_{OL} = 4mA (MIN)
- **BALANCED PROPAGATION DELAYS:**
  $t_{PLH} \cong t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE:**
  V_{CC} (OPR) = 2V to 6V
- **PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 166**

DIP   SOP   TSSOP

ORDER CODES

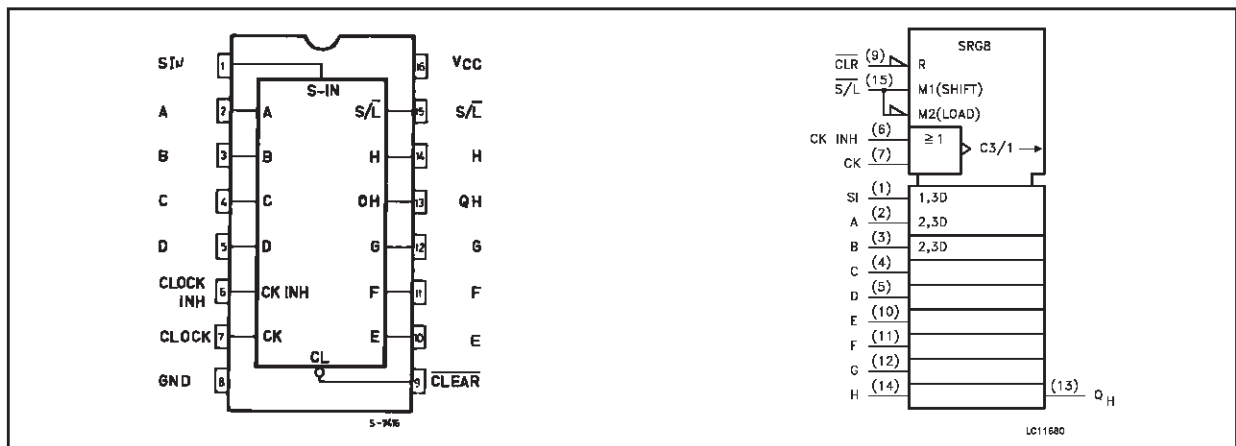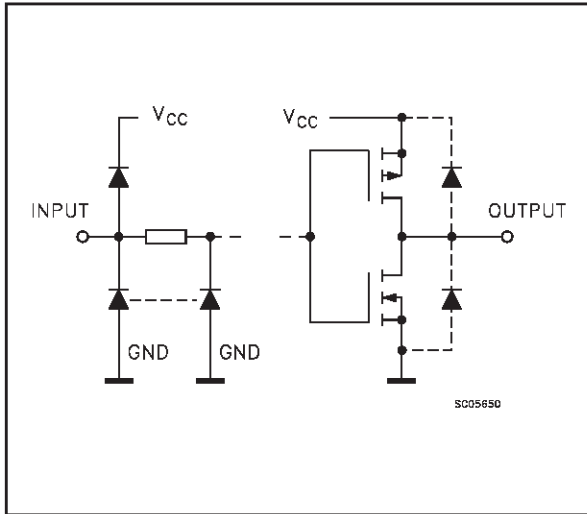| PACKAGE	TUBE	T & R
DIP	M74HC166B1R	
SOP	M74HC166M1R	M74HC166RM13TR
TSSOP		M74HC166TTR

DESCRIPTION

The M74HC166 is an high speed CMOS 8 BIT PISO SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

It consists of parallel or serial inputs and a serial-out 8 bit shift register with gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/LOAD input. When the SHIFT/LOAD input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse; when held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high level edge of the clock pulse. The CLOCK-INHIBIT input should be changed to the high only while the clock input is held high. A direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. Functional details are shown in the truth table and the timing chart. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS

INPUT AND OUTPUT EQUIVALENT CIRCUIT
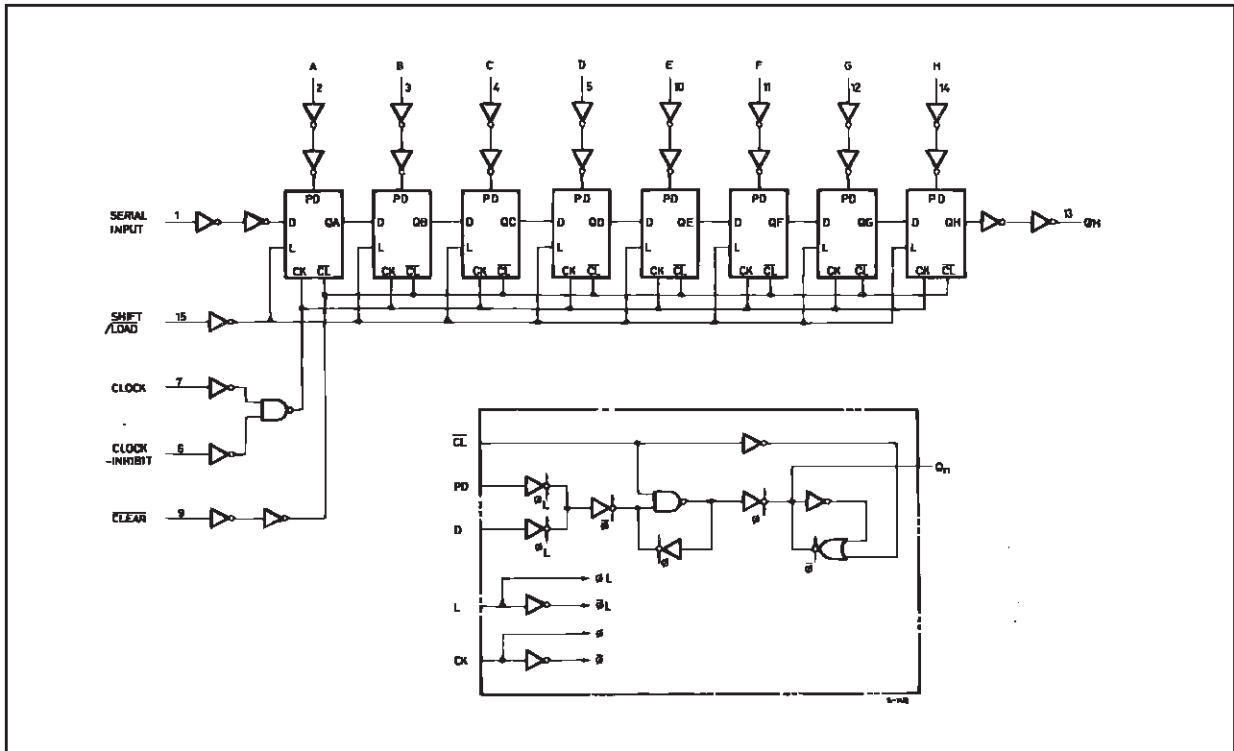

PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	SI	Serial Data Inputs
2, 3, 4, 5, 10, 11, 12, 14	A to H	Parallel Data Inputs
6	CLOCK INH	Clock Enable Input (Active Low)
7	CLOCK	Clock Input (LOW to HIGH, Edge Triggered
9	$\overline{\text{CLEAR}}$	Asynchronous Master Reset Input (Active Low)
13	Q_H	Serial Output from the Last Stage
15	SHIFT/$\overline{\text{LOAD}}$	Parallel Enable Input (Active Low)
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

TRUTH TABLE

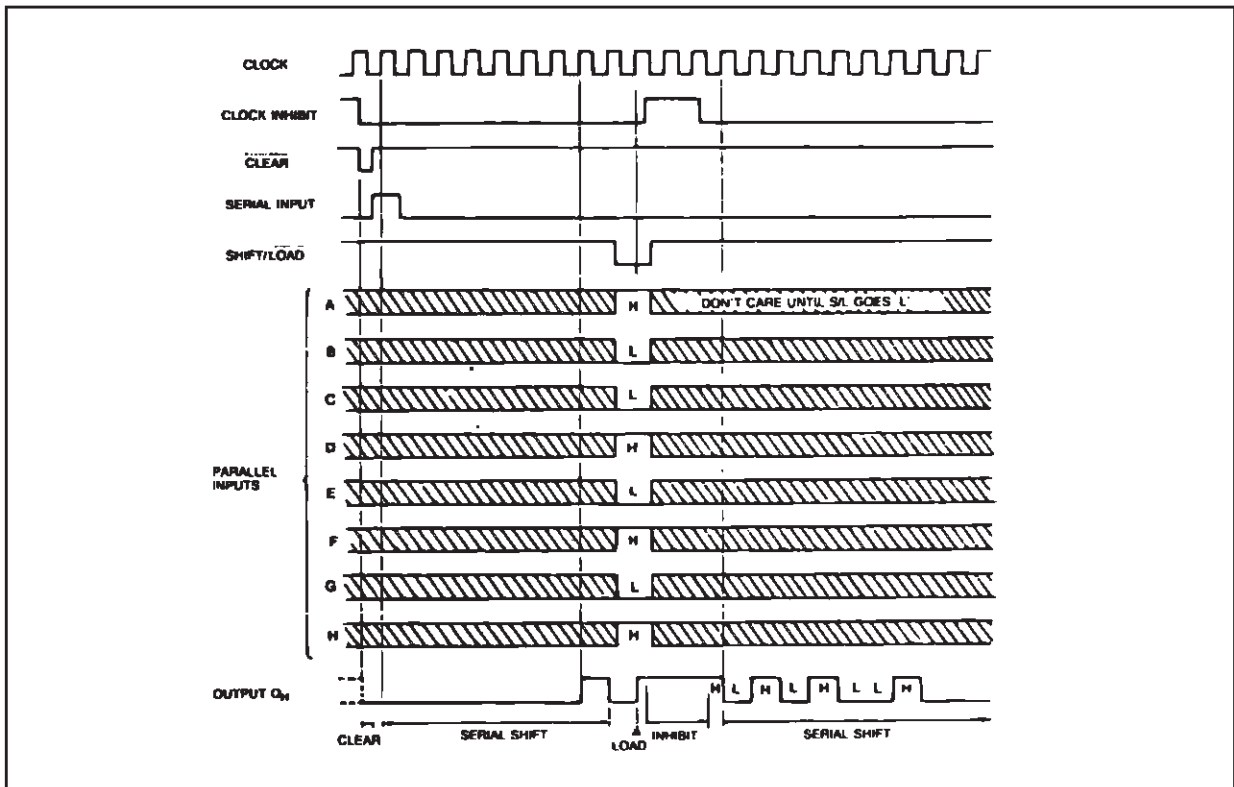| INPUTS						INTERNAL OUTPUTS		OUTPUTS
$\overline{\text{CLEAR}}$	SHIFT/$\overline{\text{LOAD}}$	CLOCK INH	CLOCK	SERIAL IN	PARALLEL A.....….H	QA	QB	QH
L	X	X	X	X	X	L	L	L
L	X	X	⌐_	X	X	NO CHANGE		
H	L	L	_⌐	X	a.......….h	a	b	h
H	H	L	_⌐	H	X	H	QAn	QGn
H	H	L	_⌐	L	X	L	QAn	QGn
H	X	H	X	X	X	NO CHANGE		

X : Don't Care
a........h : The level of steady input voltage at inputs a through H respectively

LOGIC DIAGRAM

This logic diagram has not be used to estimate propagation delays

TIMING CHART

M74HC166

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		$T_A = 25°C$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND			4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6ns)

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QH)	2.0			70	150		190		225	ns
		4.5			20	30		38		45	
		6.0			16	26		32		38	
t_{PHL}	Propagation Delay Time ($\overline{\text{CLEAR}}$ - QH)	2.0			60	135		170		205	ns
		4.5			18	27		34		41	
		6.0			14	23		29		35	
f_{MAX}	Maximum Clock Frequency	2.0		6.2	14		5.0		4.2		MHz
		4.5		31	50		25		21		
		6.0		37	63		30		25		
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0			28	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
$t_{W(L)}$	Minimum Pulse Width ($\overline{\text{CLEAR}}$)	2.0			28	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
t_s	Minimum Set-up Time (SI, PI)	2.0			20	75		95		110	ns
		4.5			4	15		19		22	
		6.0			3	13		16		19	
t_s	Minimum Set-up Time ($\overline{\text{SHIFT/}}$ LOAD)	2.0			25	75		95		110	ns
		4.5			5	15		19		22	
		6.0			3	13		16		19	
t_h	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t_{REM}	Minimum Removal Time	2.0			12	50		65		75	ns
		4.5			3	10		13		15	
		6.0			3	9		11		13	

CAPACITIVE CHARACTERISTICS

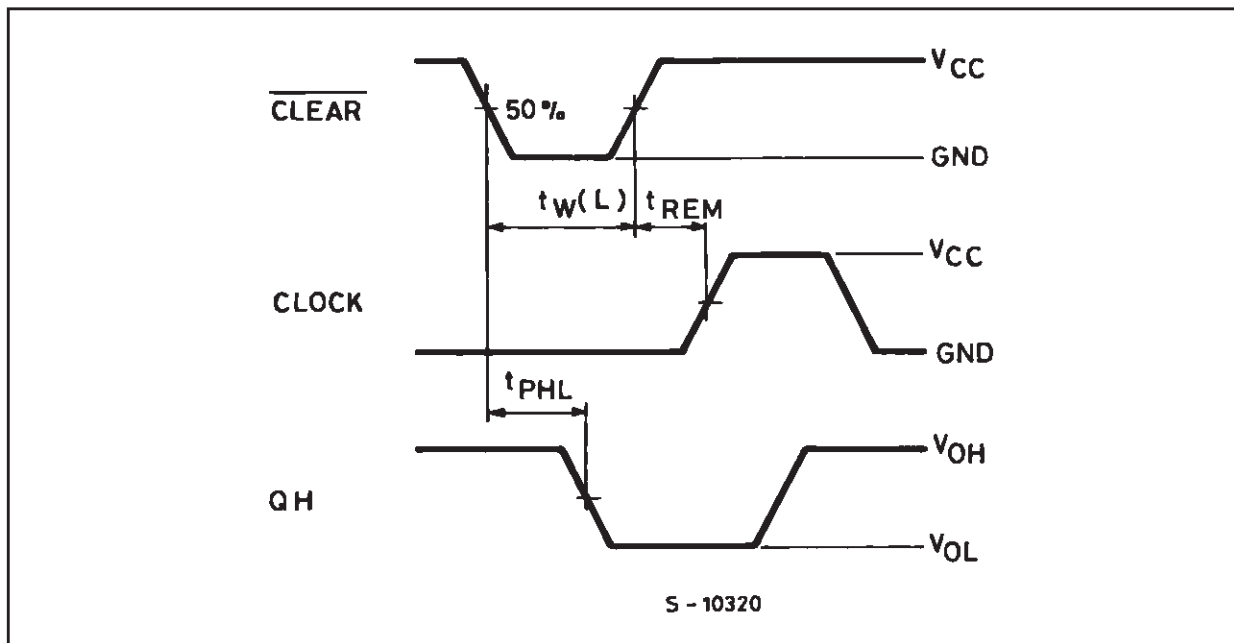| Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			60						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)}$ = C_{PD} x V_{CC} x f_{IN} + I_{CC}

TEST CIRCUIT
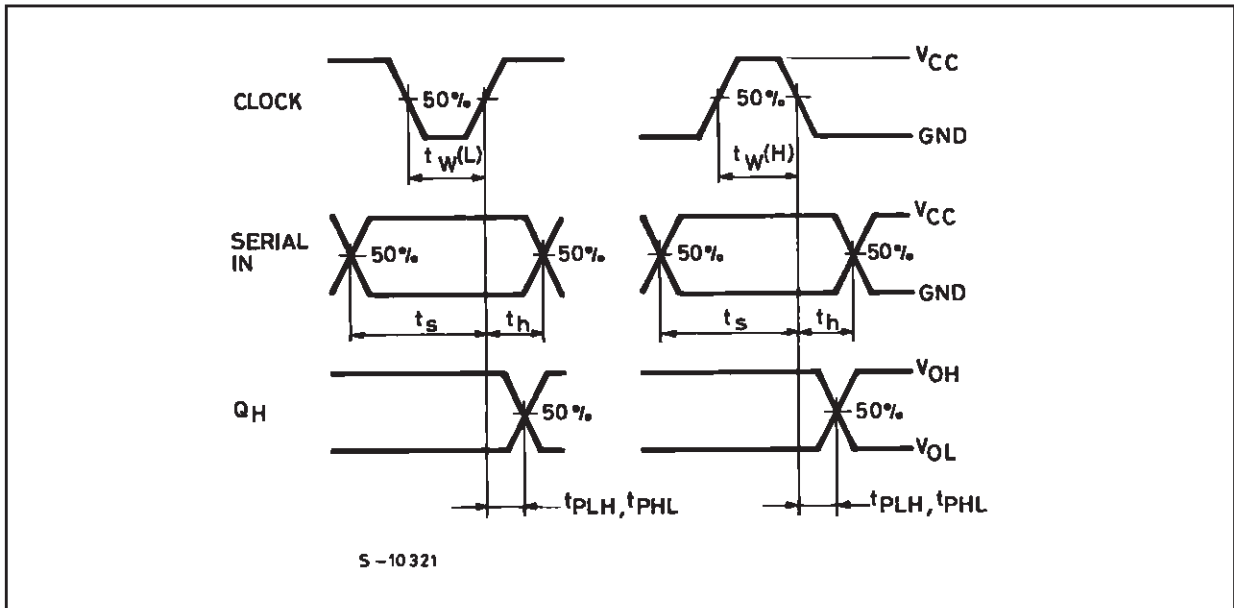

C_L = 50pF or equivalent (includes jig and probe capacitance)
R_T = Z_{OUT} of pulse generator (typically 50Ω)

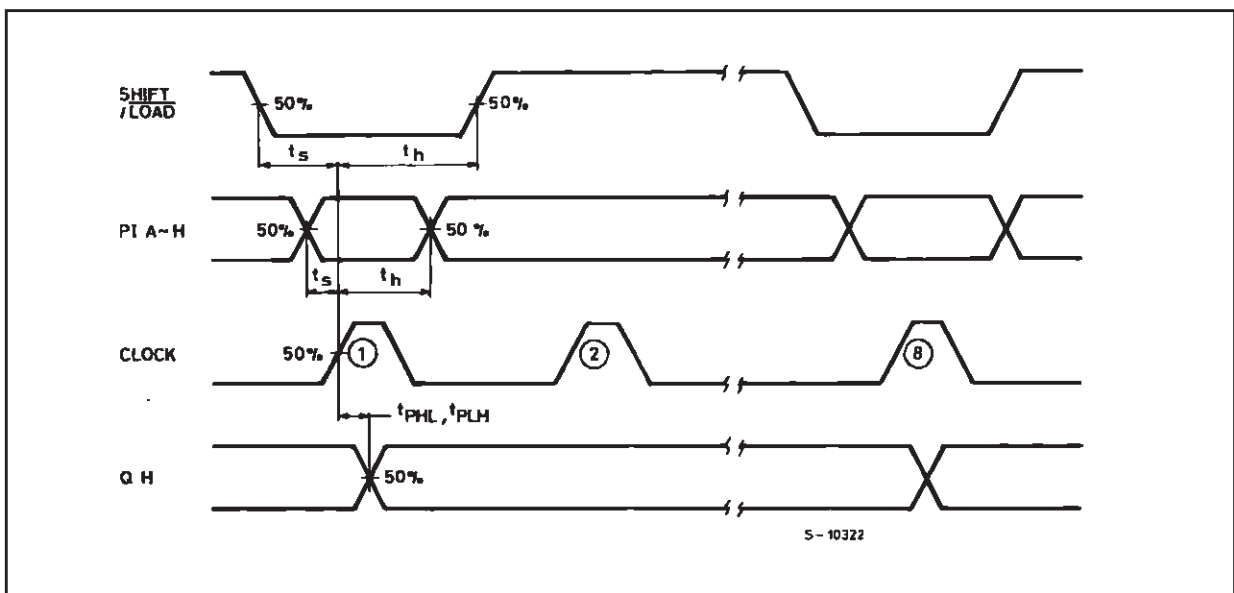**WAVEFORM 1 : MINIMUM PULSE WIDTH ($\overline{\text{CLEAR}}$), REMOVAL TIME ($\overline{\text{CLEAR}}$ TO CLOCK)**
(f=1MHz; 50% duty cycle)

WAVEFORM 2 : PROPAGATION DELAY TIME, MINIMUM PULSE WIDTH (CLOCK), SETUP AND HOLD TIME (SI to CLOCK) (f=1MHz; 50% duty cycle)
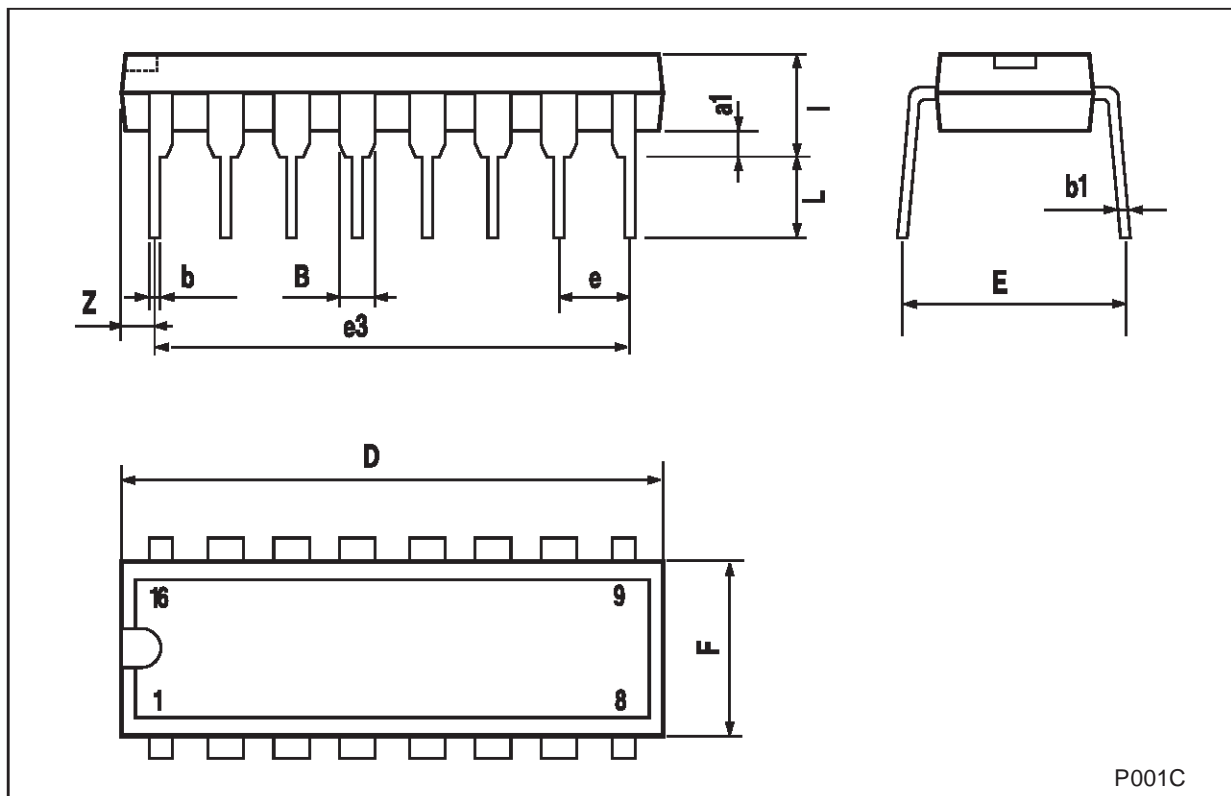

WAVEFORM 3 : PROPAGATION DELAY TIME, SETUP AND HOLD TIME (PI, $\overline{\text{S/L}}$ to CLOCK)
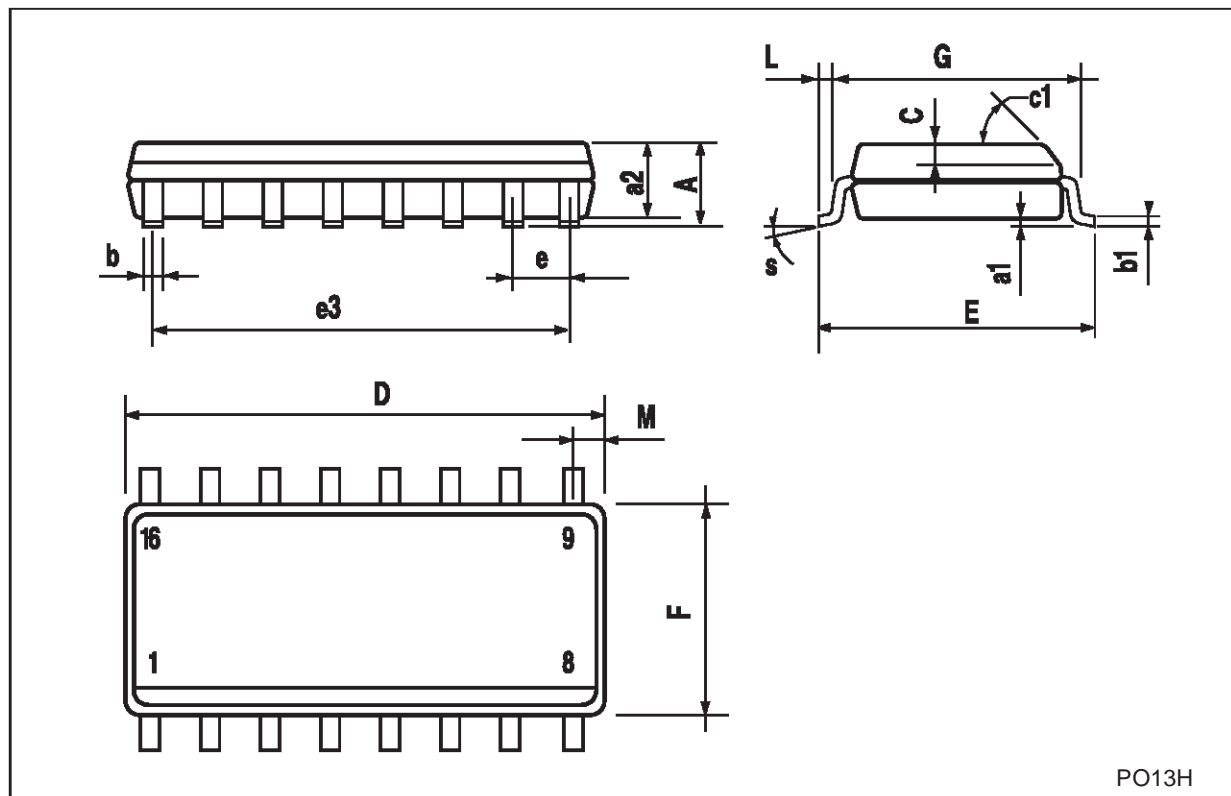(f=1MHz; 50% duty cycle)

Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050

P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					

PO13H

TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

PIN 1 IDENTIFICATION

0080338D