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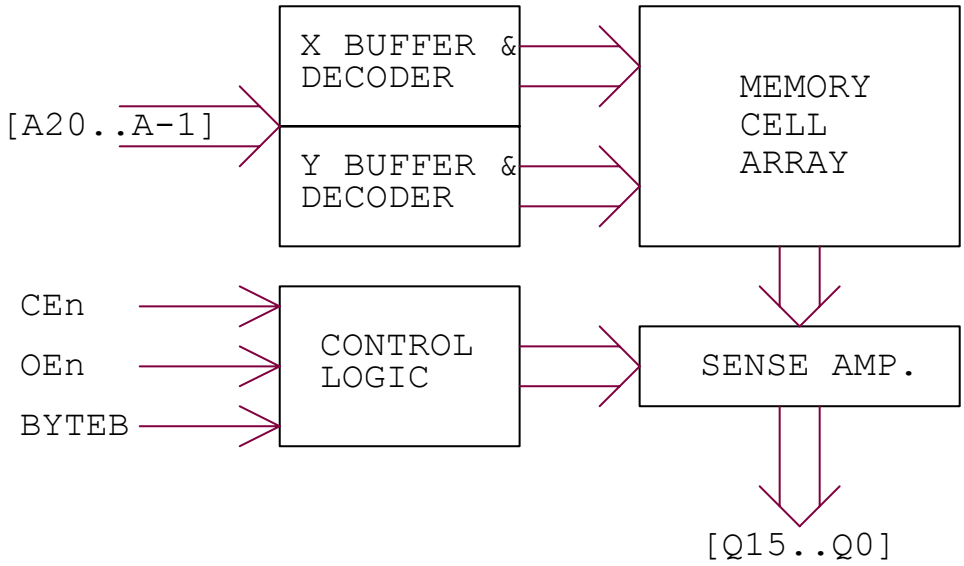
1. General Description

The SF23C3200B is a fully static, 32 Mbit CMOS Mask Programmable ROM. This device operates in wide operating range. It requires no external clock for its operation and suitable for use with microprocessor program memory, and data memory (speech, graphic, etc).

2. Features

- ✓ Operating range: 2.4V ~ 3.6V
- ✓ Organization
  - Memory Cell Array: 4M x 8 or 2M x 16 selectable by BYTEB pin
- ✓ Low Operation Current (Typical)
  - 10 μA standby mode current.
  - 30 mA active read current at 100 ns cycle time.
- ✓ Fully static operation
- ✓ Tri-state outputs
- ✓ Package: bare chip

3. Functional block diagram



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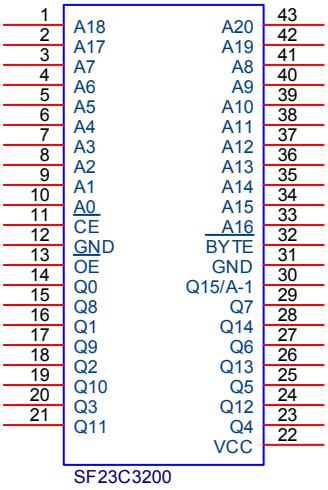
4. Pin Description



Symbol	Pin No.	I/O	Description
A18, A17	1, 2	I	Mask ROM Address input pins.
A7 ~ A0	3 ~ 10	I	Mask ROM Address input pins.
CEn	11	I	The CEn (Chip Enable) input is the device selection and power control for internal Mask ROM array. Whenever CEn goes high, the internal Mask ROM will enter standby (power saving) mode. Otherwise, it is in active mode and the contents of the ROM can be accessed.
GND	12	P	Negative power supply input pin.
OEn	13	I	OEn (Output Enable) is the output control which gates ROM array data onto the data output pins Q7 ~ Q0 in Byte mode (BYTEB pin is at "low" state) or Q15A-1, Q14 ~ Q0 in Word mode (BYTEB pin is at "high" state).
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7,	14, 16, 18, 20, 23, 25, 27, 29	O, O, O, O, O, O, O, O,	Mask ROM array Data lower byte outputs drive Q7 ~ Q0 pins during read operations (CEn and OEn are "low"). The Q7 ~ Q0 pins stay in high-Z when the chip is deselected (CEn high) or when the outputs are disabled (OEn high).
Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15A-1,	15, 17, 19, 21, 24, 26, 28, 30	O, O, O, O, O, O, O, O/I,	Mask ROM data higher byte output pins when Word mode is selected (BYTEB is at "high" level) during read operations (CEn and OEn are "low"). They will be tri-stated when Byte mode is selected (BYTEB at "low" level), the chip is deselected (CEn high), the outputs are disabled (OEn high). Q15A-1 is Mask ROM MSB Data output pin in Word mode and LSB address pin in Byte mode.
VCC	22	P	Positive power supply input pin.

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GND	31	P	Negative power supply input pin.
BYTEB	32	I	Byte/Word mode selection input pin. Byte mode is selected when it is at "low" state, otherwise Word mode is selected.
A16 ~ A8	33 ~ 41	I	Mask ROM Address input pins.
A19, A20	42, 43	I	Mask ROM Address input pins.

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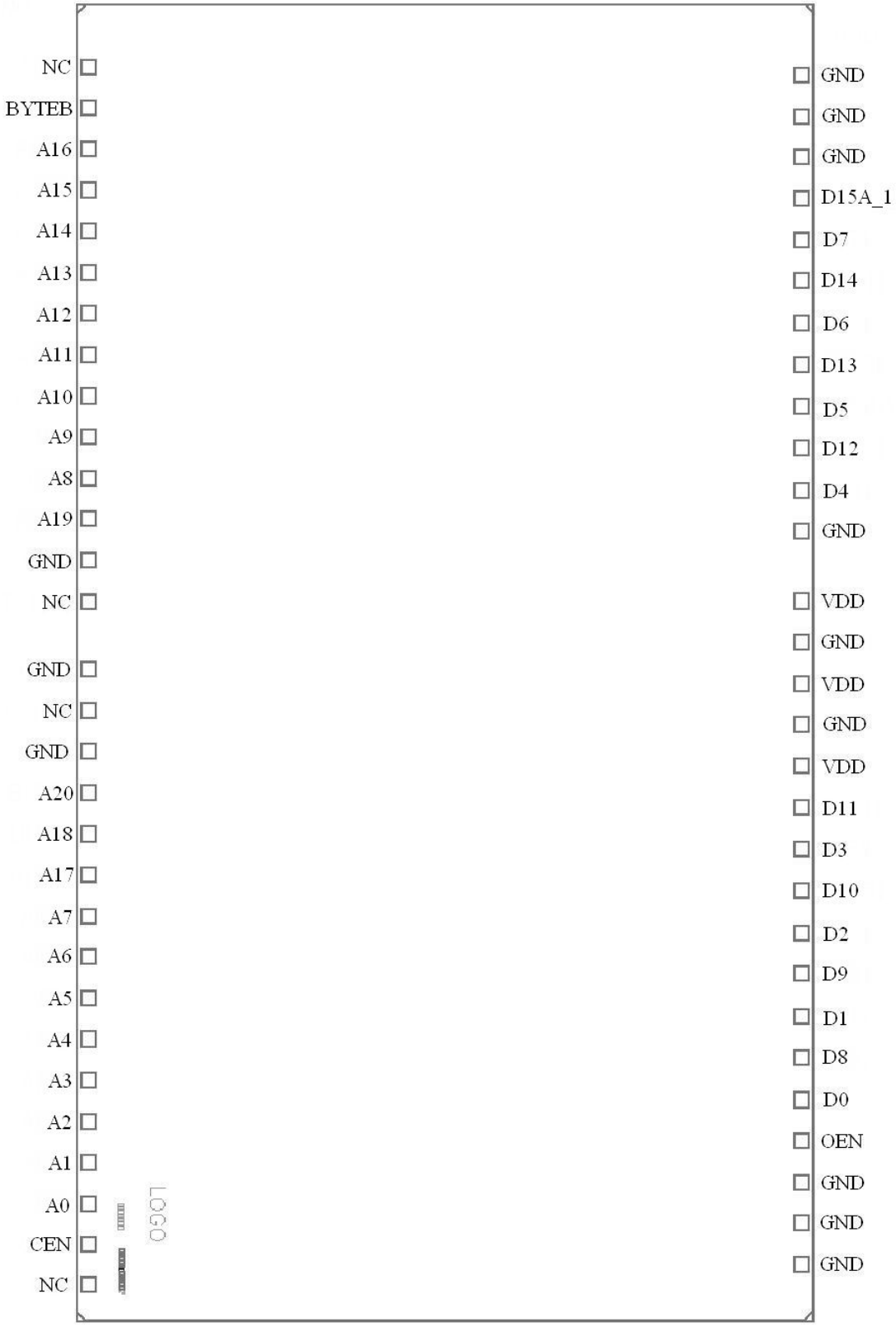
5. Pad Location



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Pad No.	Pad Name	X Coord.	Y Coord.	Pad No.	Pad Name	X Coord.	Y Coord.
1	NC	-1941.5	3231.86	31	GND	1941.5	-3262.78
2	BYTEB	-1941.5	3008.86	32	GND	1941.5	-3039.78
3	A16	-1941.5	2785.86	33	GND	1941.5	-2816.78
4	A15	-1941.5	2562.86	34	OEN	1941.5	-2593.78
5	A14	-1941.5	2339.86	35	D0	1941.5	-2370.78
6	A13	-1941.5	2116.86	36	D8	1941.5	-2140.78
7	A12	-1941.5	1893.86	37	D1	1941.5	-1917.78
8	A11	-1941.5	1670.86	38	D9	1941.5	-1687.78
9	A10	-1941.5	1447.86	39	D2	1941.5	-1464.78
10	A9	-1941.5	1224.86	40	D10	1941.5	-1234.78
11	A8	-1941.5	1001.86	41	D3	1941.5	-1011.78
12	A19	-1941.5	778.86	42	D11	1941.5	-781.78
13	GND	-1941.5	555.86	43	VDD	1941.5	-558.78
14	NC	-1941.5	332.86	44	GND	1941.5	-335.78
15	GND	-1941.5	-34.78	45	VDD	1941.5	-112.78
16	NC	-1941.5	-257.78	46	GND	1941.5	110.22
17	GND	-1941.5	-480.78	47	VDD	1941.5	333.22
18	A20	-1941.5	-703.78	48	GND	1941.5	712.16
19	A18	-1941.5	-926.78	49	D4	1941.5	935.16
20	A17	-1941.5	-1149.78	50	D12	1941.5	1165.16
21	A7	-1941.5	-1372.78	51	D5	1941.5	1388.16
22	A6	-1941.5	-1595.78	52	D13	1941.5	1618.16
23	A5	-1941.5	-1818.78	53	D6	1941.5	1841.16
24	A4	-1941.5	-2041.78	54	D14	1941.5	2071.16
25	A3	-1941.5	-2264.78	55	D7	1941.5	2294.16
26	A2	-1941.5	-2487.78	56	D15A_1	1941.5	2517.16
27	A1	-1941.5	-2710.78	57	GND	1941.5	2740.16
28	A0	-1941.5	-2931.48	58	GND	1941.5	2963.16
29	CEN	-1941.5	-3152.18	59	GND	1941.5	3186.16
30	NC	-1941.5	-3372.88				

6. Absolute Maximum Rating

Items	Symbol	Rating
Supply Voltage	V_{CC}	2.4 to 3.6 V
Input Voltage	V_{IN}	-0.3 to Vdd+0.3 V
Operating Temperature	T_{OPR}	-0 to 70 °C
Storage Temperature	T_{STR}	-55 to 125 °C

7. AC Electrical Characteristics

READ CYCLE:

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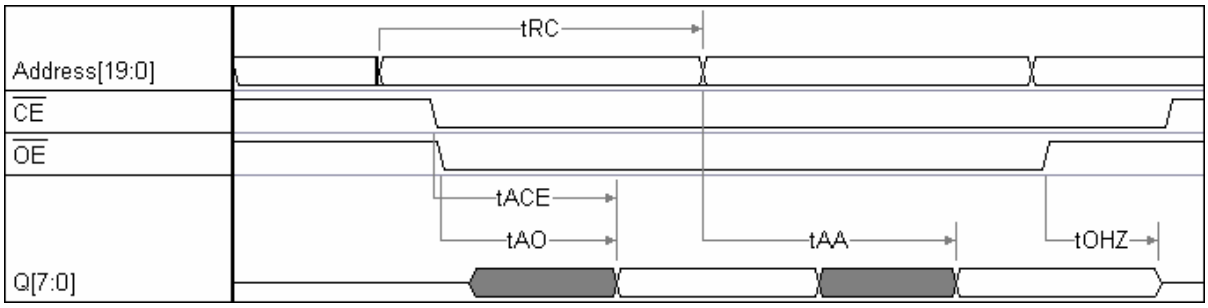
There are two ways of accessing the ROM data. The first one is to assert the valid address on the Address Bus, then assert CEn "low" to enable the ROM array. The access time in this mode is specified as t_{ACE}. The advantage of this access mode is that power consumption can be lowered. The second access mode keeps the CEn "low" while changes the addresses to access the contents of ROM data. The access time in this way is specified as t_{AA}.

Item	Symbol	Min	Max	Unit	Condition
Read Cycle Time	t_{RC}	100		ns	V_{DD} = 3.0 V, no load
		120			V_{DD} = 2.4V, no load
Chip Enable Access Time	t_{ACE}		100	ns	V_{DD} = 3.0 V, no load
			120		V_{DD} = 2.4V, no load
Address Access Time	t_{AA}		100	ns	V_{DD} = 3.0 V, no load
			120		V_{DD} = 2.4V, no load
Output Enable Time	t_{OE}		50	ns	
Output or Chip Disable to Output High-Z	t_{DF}		20	ns	
Output Hold from Address Change	t_{OH}	0		ns	



8. DC Electrical Characteristics

(GND = 0V, V_{CC} = 3.0 V, T_{OPR} = 25°C unless otherwise noted)

Parameter	Symbol	Min.	Typical	Max.	Unit	Condition
Supply Voltage	V_{CC}	2.4	-	3.6	V	
Operating Current	I_{CC}	-	30	-	mA	No load, t_{RC}@ 100 ns
Standby Current	I_{STBY}	-	10	-	μA	No load
Input voltage	V_{IH}	2/3	-	1	V_{DD}	V_{DD} = 2.4V ~ 3.6V
	V_{IL}	0	-	1/3		
Input current leakage	I_{IL}	-	-	± 10	μA	
P0, P1 Output High Voltage	V_{OH}	2.4	-	-	V	I_{OH} = 0.4 mA
P0, P1 Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
D Output High Voltage	V_{OH}	2.4	-	-	V	I_{OH} = 1.4 mA
D Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 3 mA

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