19-5031; Rev 0; 11/09

EVALUATION KIT AVAILABLE

Single-Phase Power-Measurement IC with I²C Interface

MAXQ314

General Description

The MAXQ314 is a dedicated power-measurement IC that collects and calculates voltage, current, power, and power factor for a single-phase load. The results can be retrieved by an external master through the internal I²C bus. This bus is also used by the external master to configure the operation of the MAXQ314 and monitor the status of operations.

The MAXQ314 performs voltage and current measurements using an integrated ADC that can measure voltage and current. Other values such as power are calculated from that data. The MAXQ314 also has an integrated temperature sensor that provides the die temperature on demand. The internal current amplifier produces up to 32x gain and the voltage amplifier gain is 1x.

Applications

Single-Phase AC Power Monitoring

Features

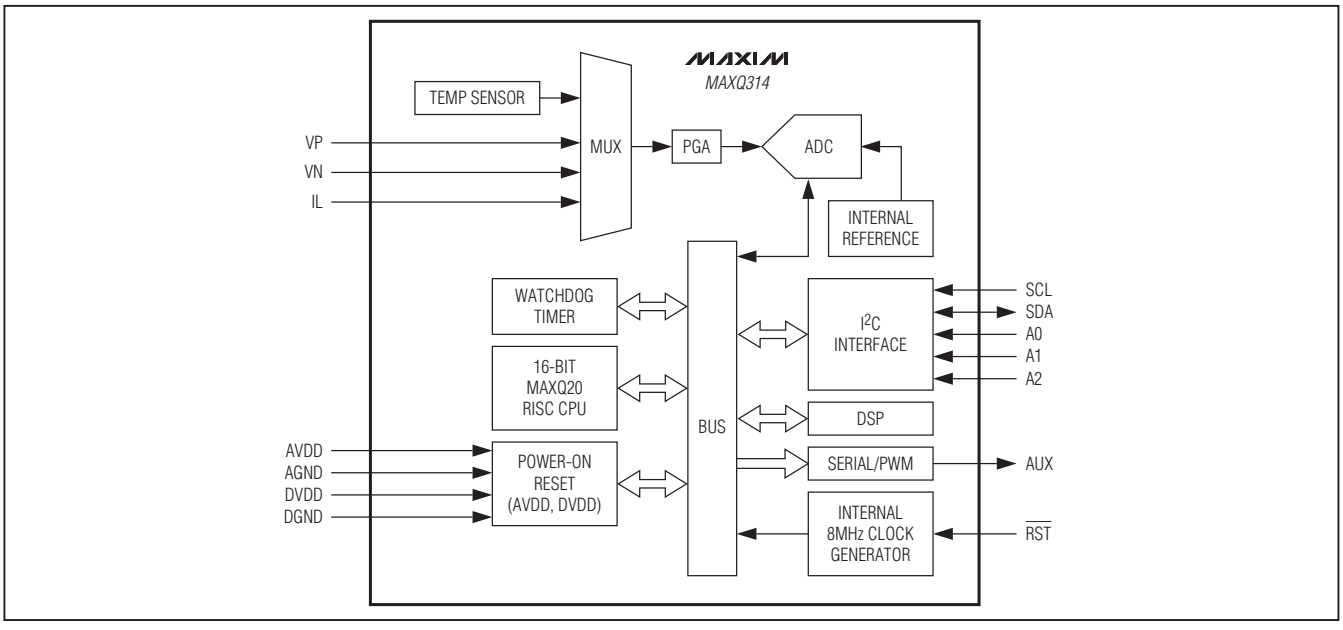
- **High-Performance, Low-Power DSP Core**
- **On-Chip Digital Temperature Sensor**
- **Precision Internal Voltage Reference**
- **Active Power (W), < ±0.5% Error**
- **Reactive Power (VAR), < ±0.7% Error**
- **Apparent Power (VA), < ±0.7% Error**
- **Power Factor, < ±1% Error**
- **Voltage RMS, < ±0.2% Error**
- **Current RMS, < ±0.5% Error**
- **I²C-Compatible Serial Interface**
- **Continuous Output of IRMS in Serial or PWM**

Ordering Information

PART	OPERATING VOLTAGE (V)	TEMP RANGE	PIN-PACKAGE
MAXQ314+	3.0 to 3.6	-40°C to +85°C	20 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Block Diagram



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Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: **www.maxim-ic.com/errata**.*

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on DVDD with Respect to DGND ..... -0.3V to +4.0V
Voltage Range on AVDD with Respect to AGND ..... -0.3V to +4.0V
Voltage Range on AGND with Respect to DGND ..... -0.3V to +0.3V
Voltage Range on AVDD with Respect to DVDD ..... -0.3V to +0.3V
Voltage Range on Any Lead with Respect to (DGND = AGND) ..... -0.3V to +4V
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Continuous Power Dissipation (T_A = +70°C)
20-Pin TQFN (derate 20.8mW/°C above +70°C) 1667mW
ESD Protection (Human Body Model) ..... ±2kV
Soldering Temperature ..... Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

POWER-MONITORING SPECIFICATIONS

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Active-Power Error	Current input DR 500:1		0.5		%
Reactive-Power Error	Current input DR 500:1		0.7		%
Apparent-Power Error	Current input DR 500:1		0.7		%
Power-Factor Error	Current input DR 500:1		0.1		%
RMS Voltage Error	Current input DR 30:1		0.2		%
RMS Current Error	Current input DR 500:1		0.5		%

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Digital Supply Voltage	V_{DVDD}		3.0		3.6	V
Supply Current	I_{DVDD}	I_{DVDD} + I_{AVDD}, f_{CLK} = 8MHz		6.5	15.0	mA
Analog Supply Voltage	V_{AVDD}		3.0		3.6	V
Supply Voltage Power-Fail Trip Point	UVLO	Rising, V_{DVDD} = V_{AVDD}	2.75	2.8	2.95	V
		Hysteresis		100		mV
DIGITAL I/O						
Input High Voltage ($\overline{RST}$)	V_{IH}		2.1			V
Input High Voltage (A0, A1, A2)	V_{IH2}		V_{DVDD} - 0.3			V
Input Low Voltage ($\overline{RST}$)	V_{IL}				0.8	V
Input Low Voltage (A0, A1, A2)	V_{IL2}				0.3	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage (AUX)	V_{OL}	I_{OL} = 6mA		0.4		V
Input Leakage (A0, A1, A2)	I_L		-12		+12	µA
Input Capacitance ($\overline{RST}$, A0, A1, A2)	C_{IN}			10		pF
$\overline{RST}$ Pullup Resistance	R_{RST}		50	150	200	kΩ
INTERNAL OSCILLATOR						
Oscillator Frequency	f_{SCLK}		7.2	8	8.8	MHz
AFE AND ANALOG-TO-DIGITAL CONVERTER						
Voltage Range (VP)			0		1.5	V
Voltage Range (VN)			0		1.5	V
Slow Current Channel (IL)			0		1.5	V
Input Capacitance Single-Ended				10		pF
ADC Sampling Rate		Per channel		5		ksps
INTERNAL VOLTAGE REFERENCE						
Reference Accuracy		T_A = -40°C to +85°C	1.8	2.07	2.3	V
TEMPERATURE SENSOR						
Temperature Accuracy		T_{EP} = -40°C to +85°C		3		°C

I²C ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, T_A = -40°C to +85°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Low Voltage	V_{IL_I2C}			0.3 x V_{DVDD}	V
Input High Voltage	V_{IH_I2C}		0.7 x V_{DVDD}		V
Input Hysteresis (Schmitt)	V_{IHYS_I2C}	V_{DVDD} > 2V (Note 1)	0.05 x V_{DVDD}		V
Output Logic-Low (Open Drain or Open Collector)	V_{OL_I2C}	V_{DVDD} > 2V, 6mA sink current	0	0.4	V
Input Current on I/O	I_{IN_I2C}	Input voltage from 0.1 x V_{DVDD} to 0.9 x V_{DVDD}	-10	+10	µA
I/O Capacitance	C_{IO_I2C}	(Note 1)		10	pF

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I²C BUS CONTROLLER TIMING

(V_{DVDD} = 3.0V to 3.6V, T_A = +25°C, unless otherwise noted. Typical values are at V_{DVDD} = 3.3V, T_A = +25°C.) (Note 1, Figure 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Note 3)			0.9	µs
Data Setup Time	$t_{SU:DAT}$		120			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.6			µs
Rise Time of Both SDA and SCL Signals Receiving	t_{R_I2C}	(Notes 4, 5)		$20 + 0.1C_B$	300	ns
Fall Time of Both SDA and SCL Signals Receiving	t_{F_I2C}	(Notes 4, 5)		$20 + 0.1C_B$	300	ns
Fall Time of SDA Transmitting	t_{F_TX}	(Notes 4, 5)		$20 + 0.1C_B$	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Note 6)			50	ns
Capacitive Load for Each Bus Line	C_B	(Note 5)			400	pF

Note 1: Specifications guaranteed, but not production tested.
Note 2: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 3: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.
Note 4: $I_{SINK} \le 6mA$. t_{R_I2C} and t_{F_I2C} measured between 0.3 x V_{DVDD} and 0.7 x V_{DVDD}.
Note 5: C_B = Total capacitance of one bus line in pF.
Note 6: Guaranteed by design. Input filters on the SDA and SCL pins suppress noise spikes less than 50ns.

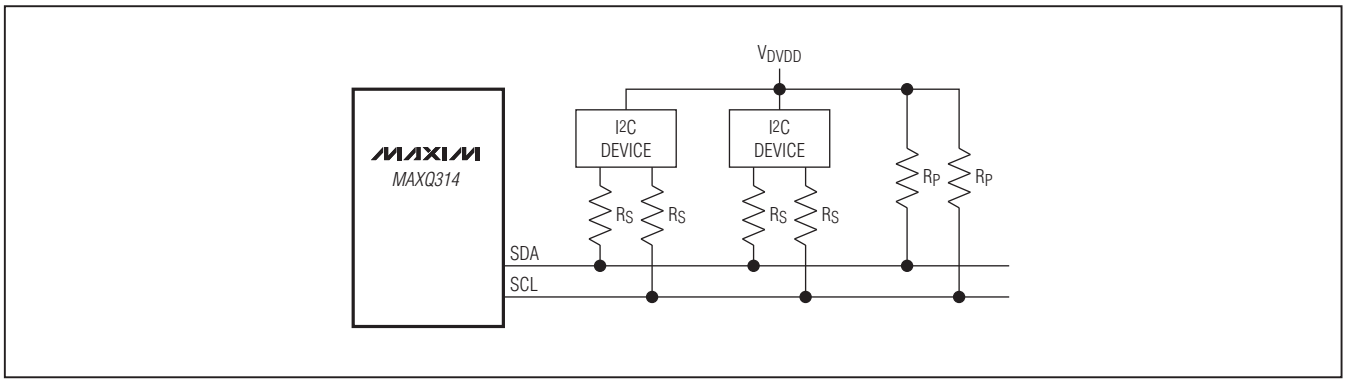

Figure 1. Series Resistors (R_S) for Protecting Against High-Voltage Spikes

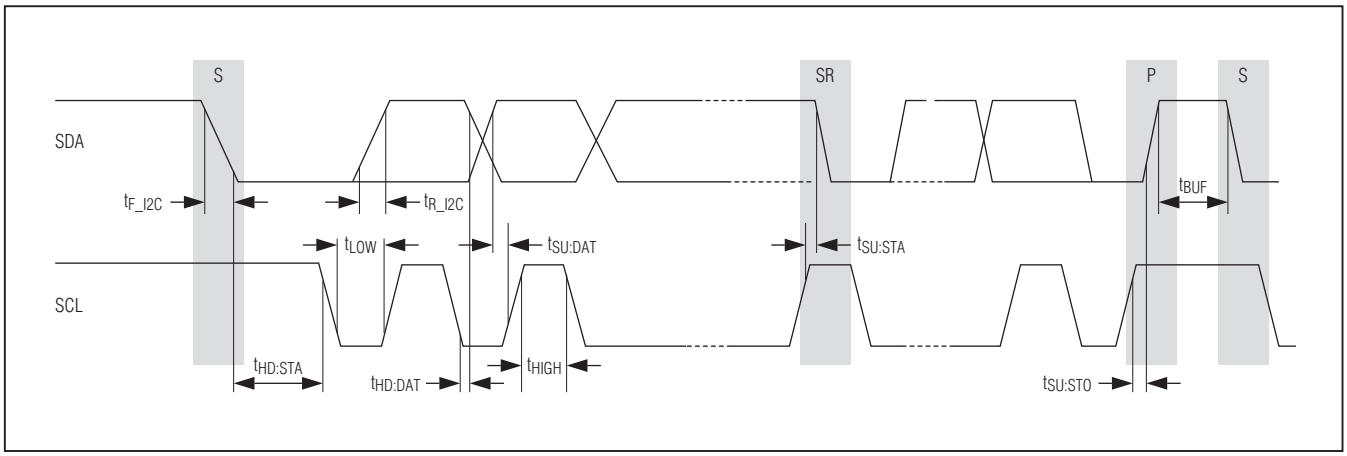

Figure 2. I²C Bus Controller Timing Diagram

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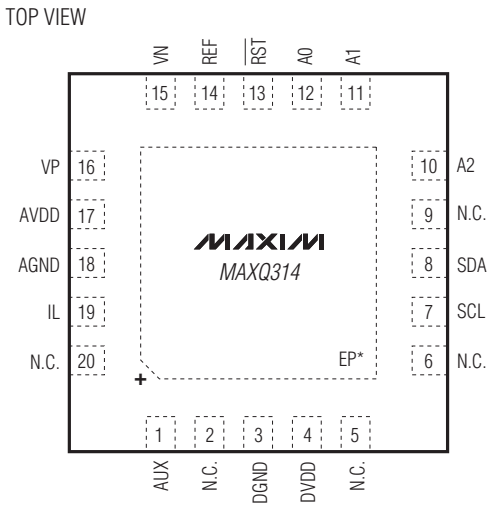
Pin Configuration



TQFN
(5mm × 5mm)

*EXPOSED PAD.

Pin Description

PIN	NAME	FUNCTION
		POWER PINS
3	DGND	Digital Ground. AGND and DGND should be connected externally through a single point connection.
4	DVDD	Digital Supply Voltage. Connect AVDD to DVDD externally. Connect a 0.1µF capacitor to DGND.
14	REF	Buffered Reference Output. Connect this pin to AGND through a 1µF capacitor. No other signals should be connected to this pin.
17	AVDD	Analog Supply Voltage. Connect AVDD to DVDD externally. Connect a 0.1µF capacitor to AGND.
18	AGND	Analog Ground. AGND and DGND should be connected externally through a single point connection.
—	EP	Exposed Pad. Connect to AGND.
		COMMUNICATION AND CONTROL PINS
1	AUX	RMS Current Continuous Output. This open-drain pin continuously outputs the value of the most recent 16-bit RMS current measurement. If the SPCFG.PWMOUT bit is set, the value is instead output in PWM format.
7	SCL	I²C Clock Line I/O
8	SDA	I²C Data Line I/O
10	A2	Device Selection Address Bits, Input. These bits select the slave address shown in Table 1.
11	A1	
12	A0	
13	$\overline{RST}$	Active-Low Reset Input. The CPU is held in reset when this pin is low. The pin includes pullup current source and should be driven by an open-drain external source capable of sinking in excess of 4mA.

Pin Description (continued)

PIN	NAME	FUNCTION
VOLTAGE AND CURRENT MEASUREMENT PINS		
15	VN	Differential Voltage Negative Input
16	VP	Differential Voltage Positive Input
19	IL	Single-Ended Current Input, Low Frequency
NO CONNECTION PINS		
2, 5, 6, 9, 20	N.C.	No Connection. Do not connect any signal to this pin.

Detailed Description

The MAXQ314 is a dedicated analog front-end (AFE) that measures voltage, current, and temperature. The internal DSP then derives calculated values. It communicates with a master device using the I²C communication protocol, and continuously executes the following operations:

- Scans AFE channels and collects raw voltage and current samples
- Calculates power (real, reactive, apparent)
- Responds to register write and read commands from the master

It is the master device's responsibility to ensure that all configuration registers have been set to their correct values in order to achieve the specified accuracy.

Clock Source

An internal oscillator supplies a system clock of approximately 8MHz, varying slightly over temperature and voltage. No external components are needed.

Reset Sources

External Reset

An external reset is generated by driving the $\overline{RST}$ pin low for at least 1µs and remains as long as $\overline{RST}$ is held low. Once the external reset has been released, all registers are cleared to their default states, and the device resumes execution.

Voltage Monitor

The device is held in reset any time the power supply AVDD drops below the supply voltage power-fail threshold. Once the power supply rises above the supply voltage power-fail level, the device exits reset, and all registers are reset to their defaults and execution resumes.

I²C Slave Operation

The MAXQ314 operates as an I²C slave peripheral and requires an external I²C master. All communications between the two are performed over a standard I²C bus, using commands to read and write values to internal registers. These registers contain:

- Operating mode settings
- Calibration parameters (supplied by the master)
- Read-only registers containing power, current, and voltage data

During operation, voltage and current measurements are taken, filtered, and the collected data is processed. The output results then can be read by the master from read-only registers in parallel with the ongoing measurement and processing operations.

The device must be initialized by the master with configuration and calibration parameters following every power-up or reset cycle.

Single-Phase Power-Measurement IC with I²C Interface

I²C Rate and Resets

The I²C bus is dedicated to communications with the master device. The master device initiates all communications. During an I²C transfer, data is transmitted and received over the serial data line (SDA) with respect to a serial shift clock (SCL). I²C transfers always start with the most significant bit and end with the least significant bit. All I²C transfers are 8 bits in length, followed by an ACK/NACK bit.

The clock rate used for the I²C interface is determined by the bus master, but can be at most 400kHz. The MAXQ314 can hold the SCL line low while processing commands to delay reception of further data. For frequencies at or below 100kHz, the delay can be transparent, but at 400kHz delays can be noticeable.

A timeout provision resets the I²C controller if a low level is detected on the SCL pin for a period of 30ms. The I²C controller returns to its default state, and the SDA and SCL pins go their idle state.

Table 1. Slave Address Determination

A2	A1	A0	SLAVE ADDRESS :7
L	L	L	60h (1100 000b)
L	L	Z	61h (1100 001b)
L	L	H	62h (1100 010b)
L	Z	L	63h (1100 011b)
L	Z	Z	64h (1100 100b)
L	Z	H	65h (1100 101b)
L	H	L	66h (1100 110b)
L	H	Z	67h (1100 111b)
L	H	H	68h (1101 000b)
Z	L	L	69h (1101 001b)
Z	L	Z	6Ah (1101 010b)
Z	L	H	6Bh (1101 011b)
Z	Z	L	6Ch (1101 100b)
Z	Z	Z	6Dh (1101 101b)
Z	Z	H	6Eh (1101 110b)
Z	H	L	6Fh (1101 111b)
Z	H	Z	70h (1110 000b)
Z	H	H	71h (1110 001b)
H	L	L	72h (1110 010b)
H	L	Z	73h (1110 011b)
H	L	H	74h (1110 100b)
H	Z	L	75h (1110 101b)
H	Z	Z	76h (1110 110b)
H	Z	H	77h (1110 111b)
H	H	L	78h (1111 000b)
H	H	Z	79h (1111 001b)
H	H	H	7Ah (1111 010b)

I²C Slave Address Generation

The A2, A1, and A0 pins are latched following every reset and used to construct the 7-bit slave address as shown in Table 1. The pin states are represented by L for logic 0, H for logic 1, and Z for high impedance.

I²C Protocol

The I²C protocol supports bus timeout and optionally packet-error checking. When packet-error checking is enabled by setting the PECEN bit (DSPCFG.3) to 1, a packet-error code (PEC) byte is appended at the end of each transaction. The byte is calculated as CRC-8 checksum, calculated over the entire message including the address and read/write bit. The polynomial used is $x^8 + x^2 + x + 1$ (the CRC-8-ATM HEC algorithm, initialized to zero).

Commands are read and write, the command code byte being an address of a register to read/write. Data length is 2 bytes for most registers, both read and write; 3 bytes for power (P, Q, S, PAVG), VRMS, and IRMS read commands. The MAXQ314 could be unable to report data like power, IRMS, VRMS, etc., immediately if the read command is received while the requested data is being calculated. In such a case, the clock line is held low until the calculation completes or a bus timeout occurs. The firmware does not support ARA address or address broadcast features.

Data and Control Registers

All transactions consist of the master writing to or reading from data, configuration, or control registers. Each register has an 8-bit address. There are several categories of internal registers; read-only registers return measurement values taken by the device. All the read/write registers are calculation coefficients set by the master. The only exceptions are the DSPCFG register, which configures operating features of the device, and the ADC_AZ register, which resets the internal ADC when it is written to.

READ WORD

S	ADDR:7	W	A	CMD:8	A	SR	ADDR:7	R	A	D0:8	A	D1:8	N	P

READ LONG

S	ADDR:7	W	A	CMD:8	A	SR	ADDR:7	R	A	D0:8	A	D1:8	A	D2:8	N	P

WRITE WORD

S	ADDR:7	W	A	CMD:8	A	D0:8	A	D1:8	A	P

READ WORD WITH PEC

S	ADDR:7	W	A	CMD:8	A	SR	ADDR:7	R	A	D0:8	A	D1:8	A	PEC:8	N	P

READ LONG WITH PEC

S	ADDR:7	W	A	CMD:8	A	SR	ADDR:7	R	A	D0:8	A	D1:8	A	D2:8	A	PEC:8	N	P

WRITE WORD WITH PEC

S	ADDR:7	W	A	CMD:8	A	D0:8	A	D1:8	A	PEC:8	A	P

A = ACKNOWLEDGE (ACK) BIT
ADDR:7 = 7-BIT DEVICE ADDRESS; MUST MATCH THE ADDRESS SELECTED BY A[2:0]
CMD:8 = REGISTER/COMMAND SELECTED IN TABLE 2
D0:8 = 8-BIT DATA; MULTIBYTE COMMANDS CAN REQUIRE D0, D1, D2, ETC.
PEC:8 = 8-BIT PEC DATA
N = NEGATIVE ACKNOWLEDGE (NACK) BIT
P = STOP BIT
S = START BIT
SR = REPEATED START BIT
W = WRITE BIT

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Table 2. Register Set

NAME	DESCRIPTION	ACCESS	BITS	CMD CODE
P	Active power	R	23:0	0100 0010b (0x42)
Q	Reactive power	R	23:0	0011 0010b (0x32)
S	Apparent power	R	23:0	0011 1010b (0x3A)
PAVG	Average power	R	23:0	0101 1010b (0x5A)
VRMS	RMS-voltage	R	23:0	0100 1010b (0x4A)
IRMS	RMS-current	R	23:0	0101 0010b (0x52)
PF	Power factor; LSB = 2^{-16}	R	23:0	0011 1100b (0x3C)
RAWTEMP	Temperature sample	R	15:0	0000 0111b (0x07)
PA	Phase-angle compensation coefficient	R/W	15:0	0010 0100b (0x24)
I_GAIN	Current gain coefficient	R/W	15:0	0010 1011b (0x2B)
V_GAIN	Voltage gain coefficient	R/W	15:0	0010 1010b (0x2A)
DSPCFG	DSP configuration	R/W	15:0	0010 0010b (0x22)
LPFC	Lowpass filter compensation	R/W	15:0	0010 0011b (0x23)
SUMCNT	Number of sampling frames per DSP cycle	R/W	15:0	0011 0100b (0x34)
ADC_AZ	ADC autozero operation. The master issues this command only when it is initializing the MAXQ314. Any value written to this register initiates a reset of the ADC, which takes approximately 1.5ms to complete.	W	7:0	0000 1111b (0x0F)
P_OFFS	Offset added to the P register	R/W	15:0	84
P_GAIN	Gain added to the P register	R/W	15:0	8c
IK	Correction factor for IRMS calculation	R/W	15:0	B2
IGV	Voltage-dependent gain correction factor for IRMS calculation	R/W	15:0	ba
I_OFFS	Offset for IRMS calculation	R/W	15:0	ac
I_OV	Voltage-dependent offset for IRMS calculation	R/W	15:0	ac

Table 3. DSPCFG Register Detail

BIT	NAME	DESCRIPTION
0	DISIL	1 = disable IL measurements 0 = enable IL measurements (default)
1	RESERVED	Must be set to 1
2	RESERVED	Must be set to 0
3	PECEN	1 = PEC enabled for I²C transmission 0 = PEC disabled for I²C transmission (default)
4	AVGP	1 = Begin accumulating PAVG 0 = Stop accumulating PAVG (default)
5	AVGRD	1 = PAVG calculation complete 0 = PAVG calculation in progress, following AVGP 1 ≥ 0 (This bit is automatically cleared the next time the master sets AVGP to 1.)
6	PWMOUT	1 = AUX pin outputs in PWM format 0 = AUX pin outputs in digital format (default)
7	DISPGA	1 = Disable gain switching 0 = Enable gain switching (recommended, default)
8	ILPGA	1 = PGA for IL = x4 (default) 0 = PGA for IL = x1
9	ACMODE	1 = AC mode 0 = DC mode (default)
10:11	RESERVED	—
12:15	RESET_STATUS	Reset Status Indicator. These bits allow the master to determine if the MAXQ314 has performed a reset since the last time these bits were cleared. When these bits are 1111, the MAXQ314 has performed a reset. After the bits have been read, the master must write 0000 to these bits to clear the reset indicator. Writing to and reading from these bits does not affect processor operation or cause a reset; they are only status bits.

Single-Phase Power-Measurement IC with I²C Interface

Calibration

Four parameters can be calibrated to optimize system performance.

Conversion to Physical Units

The output registers are in "meter" units, and need to be scaled with the input circuits to yield meaningful physical values. Two conversion coefficients are needed: the voltage transducer ratio (VTR) and the current transducer ratio (ITR), each specifying the ratio between the input and output of the corresponding transducer. The VTR represents the input voltage that would produce a 1V signal on the VP or VN pin. The ITR represents the input current that would produce a 1V signal on the IL pin.

For example, if the voltage-sensing circuit consists of a 749kΩ and 1kΩ resistor-divider, then VTR = 750(V/V). If the current-sensing circuit is a 20mΩ shunt, then 50A current would produce 1V signal on the IL pin, so ITR = 50(A/V).

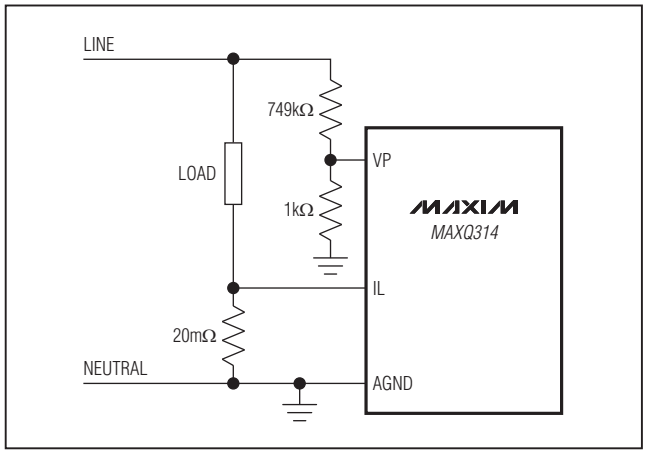

Figure 3. Calibration Circuit Example

The following equations convert "meter" units into physical units:

Voltage (V) = VRMS x VTR x $V_{REF}/2^{24}$

Current (A) = IRMS x ITR x $V_{REF}/2^{24}$

Active Power (kW) = P x VTR x ITR x V_{REF} x $V_{REF}/(10^3 \times 2^{24})$

Reactive Power (kVAR) = Q x VTR x ITR x V_{REF} x $V_{REF}/(10^3 \times 2^{24})$

Apparent Power (kVA) = S x VTR x ITR x V_{REF} x $V_{REF}/(10^3 \times 2^{24})$

where V_{REF} is the reference voltage on the REF pin in volts.

The current RMS correction is:

$$IRMS = I\_OFFS + I\_OV \times VRMS + [(I\_GAIN + IGV \times VRMS)I_{MU} + I_K/I_{MU}]$$

where I_{MU} is the current measured in meter units before correction.

Voltage RMS correction is:

$$VRMS = V\_GAIN \times V_{MU}$$

where V_{MU} is the voltage measured in meter units before correction.

Active power correction is:

$$P = V\_GAIN \times I\_GAIN \times P\_GAIN \times (P\_OFFS + P_{MU})$$

where P_{MU} is the active power measured in meter units before correction.

Apparent power is computer from the corrected voltage and current:

$$S = VRMS \times IRMS$$

Reactive power is computer from corrected S and P:

$$Q = \sqrt{S^2 - P^2}$$

Table 4. Calibration Parameters

REGISTER	DESCRIPTION
V_GAIN	Voltage Gain Factor. This factor affects the voltage RMS output and power output. The VRMS output is scaled by (1 + V_GAIN/2^{16}). V_GAIN is a signed integer and defaults to 0x0000h.
I_GAIN	Current Gain Factor. This factor affects the current RMS output and power output. The IRMS output is scaled by (1 + I_GAIN/2^{16}). I_GAIN is a signed integer and defaults to 0x0000h.
PA	Phase-Angle Compensation
LPFC	Lowpass Filter Coefficient. This factor affects the lowpass filtering. It can be left unchanged for typical configurations. It is defined as: LPFC ~ π x f_C x t_{FR} x 2^{16}, where f_C is the corner frequency Default value ~ 3.14 x 1.82 (Hz) x 200 x E - 6 (s) x 2^{16} = 75 = 0x004B

19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
SYNC				SAMPLE DATA																FRAME GAP				SYNC				SAMPLE DATA																FRAME GAP			
1	1	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	L	L	L	L	1	1	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	L	L	L	L

RMS Current Continuous Output (AUX Pin)

The AUX pin can be configured to output a 16-bit RMS current value. Bit time is 2000 system clocks, or a typical data rate of 4kbps. The bit format is pulse-width modulation, in which each bit cell is divided into four time slices. At the first time slice, the data line switches from a zero state to a one state. Then, if the bit to be transmitted is a zero, the data line switches back to zero after one time slice. If the bit to be transmitted is a one, the data line switches back to zero after three time slices.

A data frame consists of one complete 20-bit sample word and a frame delimiter. The frame delimiter consists of the data line idling in a low state for nominally four bit times (t_{BIT}).

The receiver detects the first rising edge of the sync field and synchronizes on the 1100 pattern. The receiver should be synchronized by the time the first data bit is available. After 16 data bits, the data line becomes idle for four t_{BIT} periods, after which the next synchronization bit begins.

The AUX pin can output continuous PWM as well by setting the PWMOUT (DSPCFG.6) bit. The PWM output period is 65,535 system clocks, or 8.19ms.

Applications Information

Grounds and Bypassing

Careful PCB layout significantly minimizes system-level digital noise that could interact with the microcontroller or peripheral components. The use of multilayer boards is essential to allow the use of dedicated power planes. The area under any digital components should be a continuous ground plane if possible. Keep any bypass capacitor leads short for best noise rejection and place the capacitors as close to the leads of the devices as possible.

CMOS design guidelines for any semiconductor require that no pin be taken above supply voltage or below ground. Violation of this guideline can result in a hard failure (damage to the silicon inside the device) or a soft failure (unintentional modification of memory contents). Voltage spikes above or below the device's absolute maximum ratings can potentially cause a devastating IC latchup.

Microcontrollers commonly experience negative voltage spikes through either their power pins or general-purpose I/O pins. Negative voltage spikes on power pins are especially problematic as they directly couple to the internal power buses. Devices such as keypads can conduct electrostatic discharges directly into the microcontroller and seriously damage the device. System designers must protect components against these transients that can corrupt system memory.

Specific Design Considerations for MAXQ314-Based Systems

To reduce the possibility of coupling noise into the microcontroller, the systems that use an external crystal should be designed with a crystal in a metal case that is grounded to the digital plane. Doing so reduces the susceptibility of the design to fast transient noise.

Because the MAXQ314 is used in systems where high voltages are present, care must be taken to route all signal paths, both analog and digital, as far away as possible from the high-voltage components. It is possible to construct more elaborate metering designs using multiple MAXQ314 devices. This can be accomplished by using a single I²C bus, but with a different slave address for each device.

Additional Documentation

Designers must have the following documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications.

- MAXQ314 data sheet, which contains electrical/timing specifications and pin descriptions
- MAXQ314 revision-specific errata sheet (**www.maxim-ic.com/errata**)

Single-Phase Power-Measurement IC with I²C Interface

Development and Technical Support

Maxim offers the MAXQ314 evaluation kit (EV kit) as an aid in developing and prototyping applications based on the MAXQ314. The EV kit is a reference design from which a developer can begin designing their own system. The EV kit data sheet contains a schematic of the board that can be reviewed by engineers who want to perform a preliminary investigation of the device uses before purchasing the EV kit.

Technical support is available at **https://support.maxim-ic.com/micro**.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 TQFN-EP	T2055+4	21-0140