

## 20V P-Channel Enhancement-Mode MOSFET

LP2501DT1G

### FEATURES

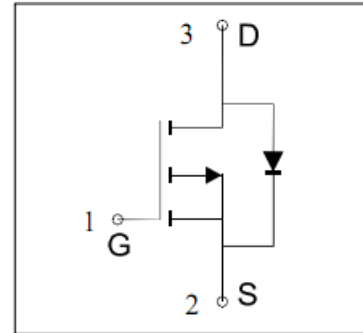
- $R_{DS(ON)} \leq 110m\Omega @ V_{GS} = -4.5V$
- $R_{DS(ON)} \leq 150m\Omega @ V_{GS} = -2.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$

### APPLICATIONS

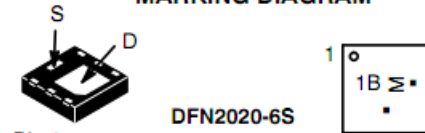
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC
- We declare that the material of product are Halogen Free and compliance with RoHS requirements.

### Ordering Information

Device	Marking	Shipping
LP2501DT1G	1B	4000/Tape&Reel



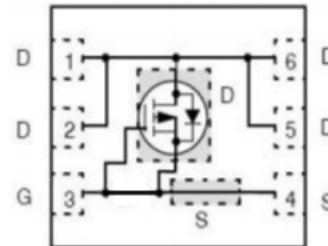
### MARKING DIAGRAM



1B = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(\*Note: Microdot may be in either location)

### PIN CONNECTIONS



(Top View)

### Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DSS}$	-20	V
Gate-Source Voltage		$V_{GSS}$	$\pm 8$	V
Continuous Drain Current (Tj=150°C)*	TA=25°C	$I_D$	-4	A
	TA=70°C		-2.4	
Pulsed Drain Current		$I_{DM}$	-14	A
Maximum Power Dissipation	TA=25°C	$P_D$	0.7	W
	TA=70°C		0.45	
Operating Junction Temperature		$T_J$	-55 to 150	°C
Storage Temperature Range		$T_{stg}$	-55 to 150	°C
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	Typical	Maximum	°C/W
		100	175	

\* The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper

## LP2501DT1G

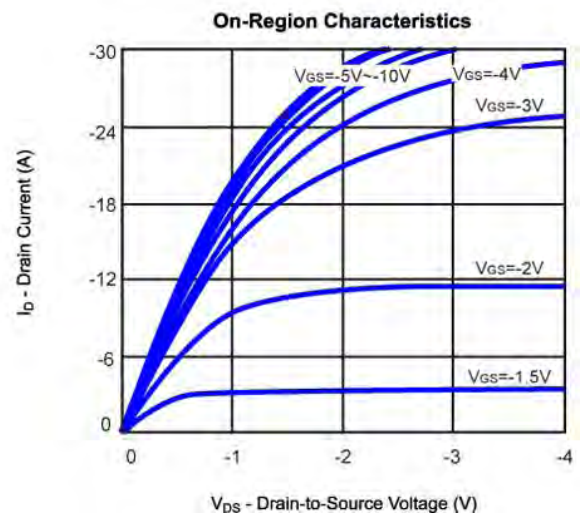
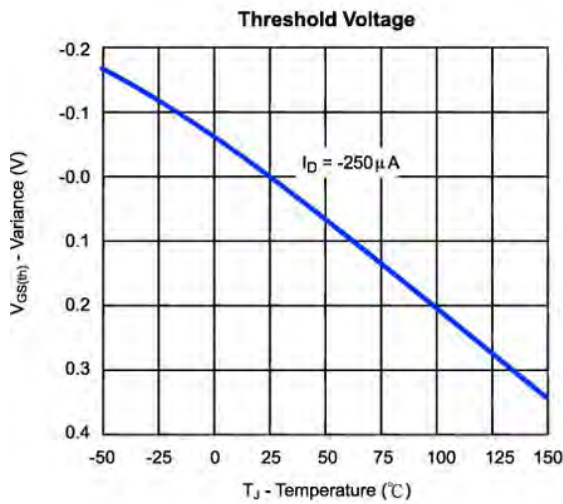
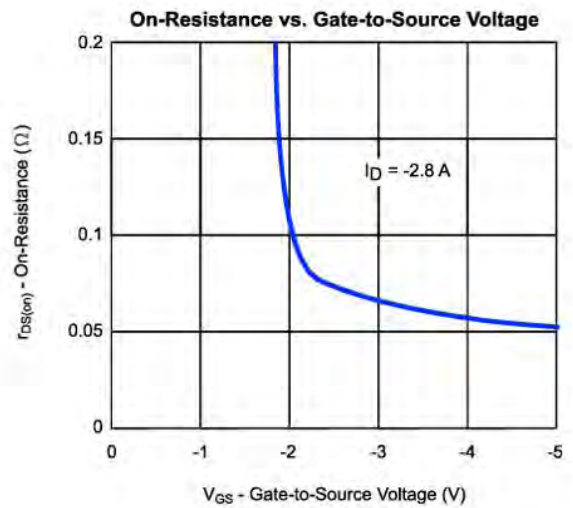
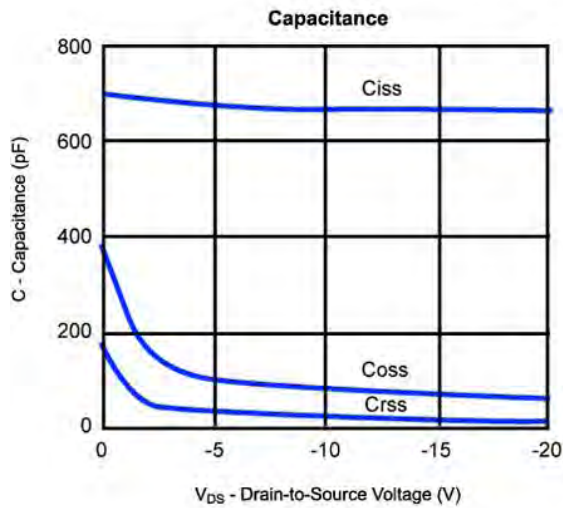
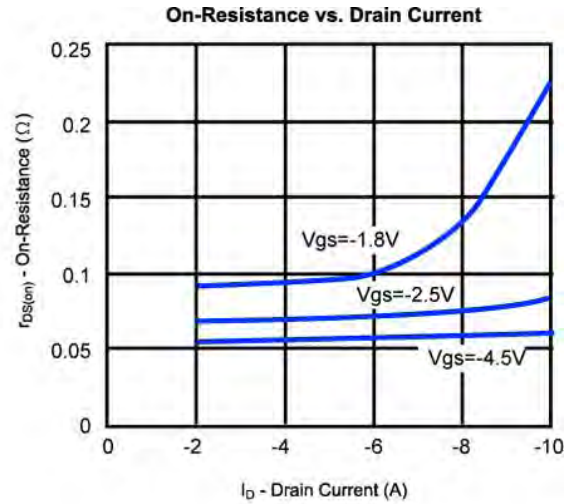
## ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250 \mu A$	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250 \mu A$	-0.4	-0.6	-1	V
$I_{GSS}$	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 8V$			$\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-20V, V_{GS}=0V$			-1	$\mu A$
$R_{DS(ON)}$	Drain-Source On-Resistance <sup>a</sup>	$V_{GS}=-4.5V, I_D=-2.8A$		90	110	m $\Omega$
		$V_{GS}=-2.5V, I_D=-2.0A$		110	150	
$V_{SD}$	Diode Forward Voltage	$I_S=-1A, V_{GS}=0V$		-0.7	-1.4	V
<b>DYNAMIC</b>						
$Q_g$	Total Gate Charge	$V_{DS}=-6V, V_{GS}=-4.5V,$ $I_D=-2.8A$		7.2		nC
$Q_{gs}$	Gate-Source Charge			2.2		
$Q_{gd}$	Gate-Drain Charge			1.2		
$R_g$	Gate resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$		7.5		$\Omega$
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V,$ $f=1MHz$		480		pF
$C_{oss}$	Output Capacitance			46		
$C_{rss}$	Reverse Transfer Capacitance			10		
$t_{d(on)}$	Turn-On Delay Time	$V_{DS}=-6V, R_L=6\Omega$ $R_{GEN}=6\Omega, V_{GS}=-4.5V$		50		ns
$t_r$	Turn-On Rise Time			30		
$t_{d(off)}$	Turn-Off Delay Time			40		
$t_f$	Turn-Off Fall time			11		

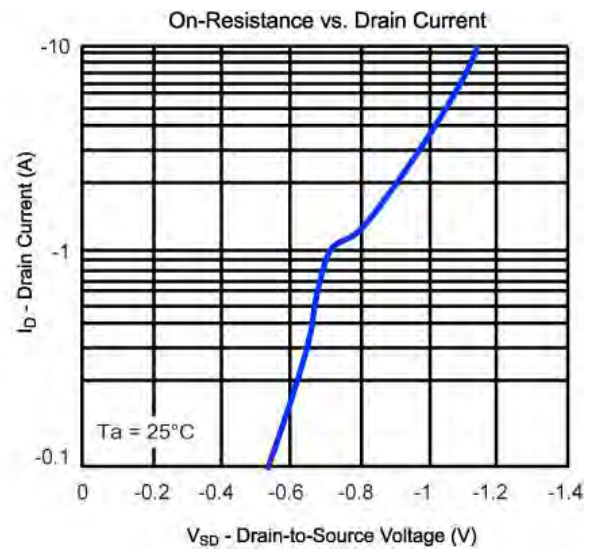
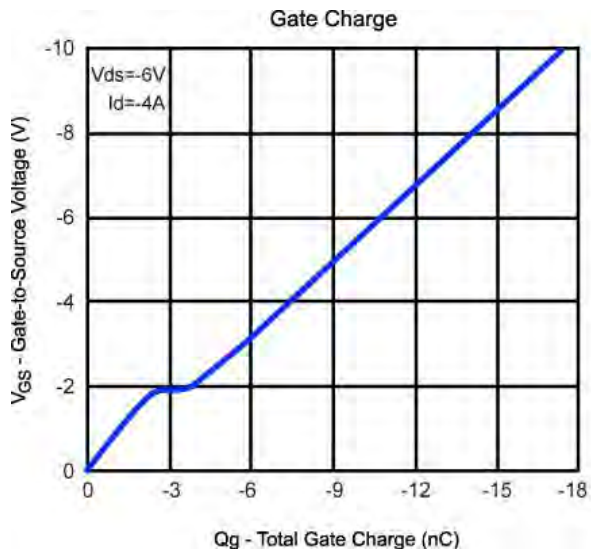
 Notes: a. Pulse test; pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$

LP2501DT1G

Typical Characteristics (T<sub>J</sub> =25°C Noted)



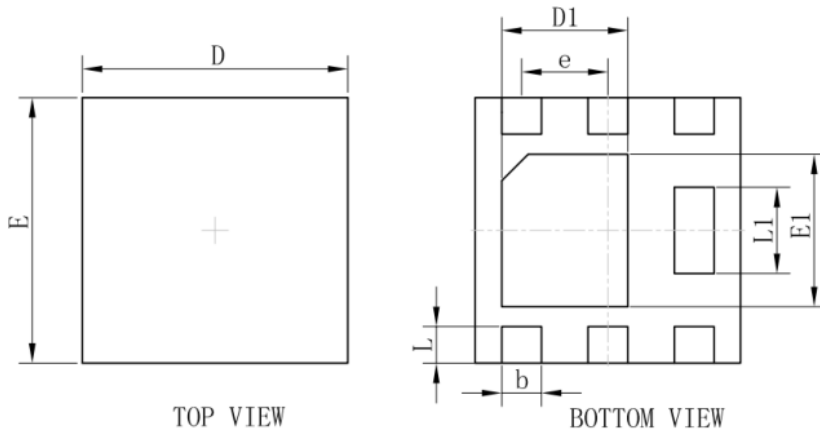
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Typical Characteristics ( $T_J = 25^\circ\text{C}$  Noted)

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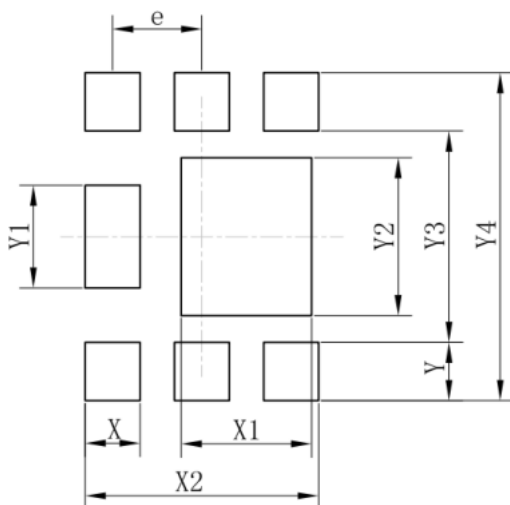
OUTLINE AND DIMENSIONS

DFN2020-6S



DFN2020-6S			
DIM	MIN	NOR	MAX
A	0.60	0.65	0.70
A1	0.01	0.03	0.05
b	0.25	0.30	0.35
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e	0.65TYP.		
L	0.23	0.28	0.33
L1	0.60	0.65	0.65
D1	0.90	0.95	1.00
E1	1.10	1.15	1.20
A3	0.152REF.		
All Dimensions in mm			

SOLDERING FOOTPRINT



DFN2020-6S	
DIM	(mm)
X	0.40
X1	0.95
X2	1.70
e	0.65
Y	0.43
Y1	0.75
Y2	1.15
Y3	1.54
Y4	2.39