

# NSDEMP11XV6T1, NSDEMP11XV6T5

## Common Anode Quad Array Switching Diode

These Common Anode Epitaxial Planar QUAD Diodes are designed for use in ultra high speed switching applications. The NSDEMP11XV6T1 device is housed in the SOT-563 package which is designed for low power surface mount applications, where board space is at a premium.

- Fast  $t_{rr}$
- Low  $C_D$
- Available in 8 mm; 7 inch Tape and Reel

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Rating	Symbol	Value	Unit
Reverse Voltage	$V_R$	80	Vdc
Peak Reverse Voltage	$V_{RM}$	80	Vdc
Forward Current	$I_F$	100	mAdc
Peak Forward Current	$I_{FM}$	300	mAdc
Peak Forward Surge Current	$I_{FSM}$ (Note 1)	2.0	Adc

1.  $t = 1 \mu\text{s}$

### THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	357 (Note 2) 2.9 (Note 2)	mW mW/ $^\circ\text{C}$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	350 (Note 2)	$^\circ\text{C}/\text{W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	500 (Note 2) 4.0 (Note 2)	mW mW/ $^\circ\text{C}$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	250 (Note 2)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	$T_J, T_{stg}$	- 55 to +150	$^\circ\text{C}$

2. FR-4 @ Minimum Pad

### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

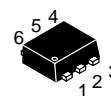
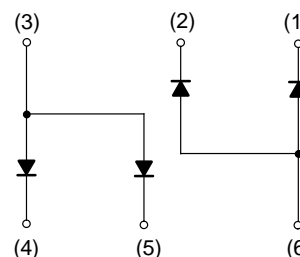
Characteristic	Symbol	Condition	Min	Max	Unit
Reverse Voltage Leakage Current	$I_R$	$V_R = 70 \text{ V}$	-	0.1	$\mu\text{Adc}$
Forward Voltage	$V_F$	$I_F = 100 \text{ mA}$	-	1.2	Vdc
Reverse Breakdown Voltage	$V_R$	$I_R = 100 \mu\text{A}$	-0	—	Vdc
Diode Capacitance	$C_D$	$V_R = 6.0 \text{ V}, f = 1.0 \text{ MHz}$	-	3.5	pF
Reverse Recovery Time	$t_{rr}$ (Note 2)	$I_F = 5.0 \text{ mA}, V_R = 6.0 \text{ V}, R_L = 100 \Omega, I_{rr} = 0.1 I_R$	-	4.0	ns

3.  $t_{rr}$  Test Circuit for NSDEMP11XV6T1 in Figure 4.



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SOT-563  
CASE 463A  
PLASTIC

### MARKING DIAGRAM



P9 = Specific Device Code  
D = Date Code

### ORDERING INFORMATION

Device	Package	Shipping
NSDEMP11XV6T1	SOT-563	4 mm pitch 4000/Tape & Reel
NSDEMP11XV6T5	SOT-563	2 mm pitch 8000/Tape & Reel

# NSDEMP11XV6T1, NSDEMP11XV6T5

## TYPICAL ELECTRICAL CHARACTERISTICS

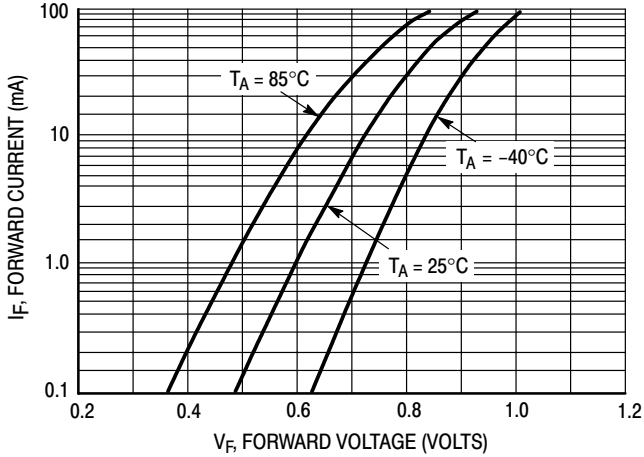


Figure 1. Forward Voltage

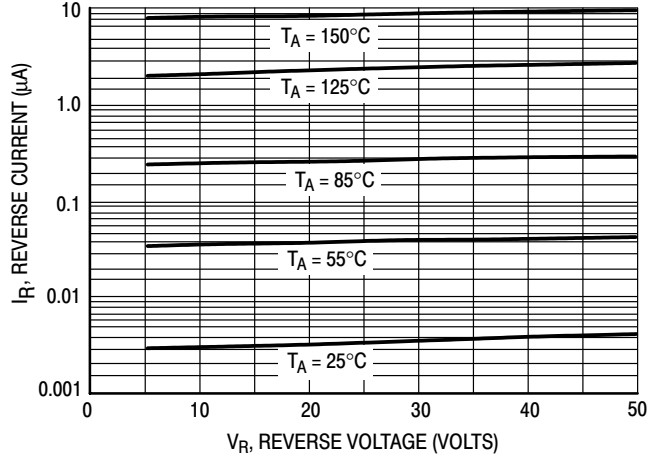


Figure 2. Reverse Current

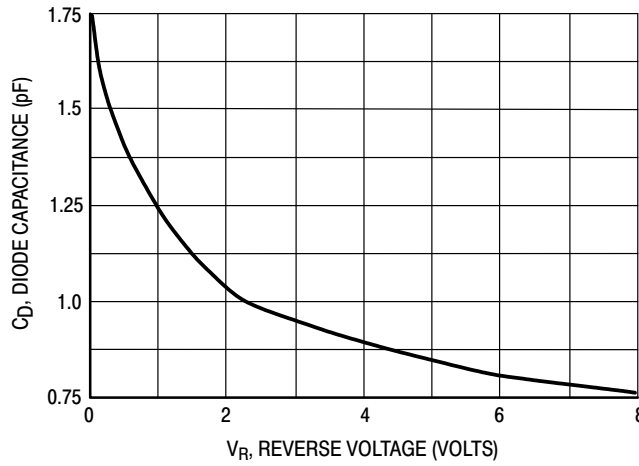
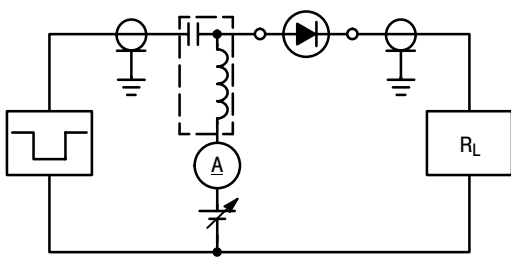
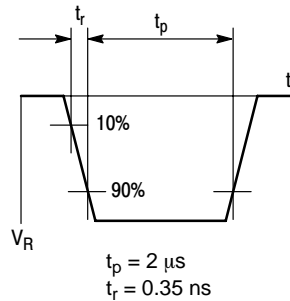


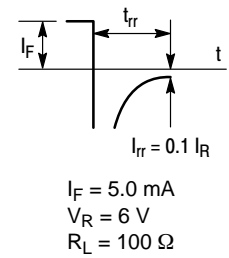
Figure 3. Diode Capacitance



RECOVERY TIME EQUIVALENT TEST CIRCUIT



INPUT PULSE



OUTPUT PULSE

$I_F = 5.0 \text{ mA}$   
 $V_R = 6 \text{ V}$   
 $R_L = 100 \Omega$

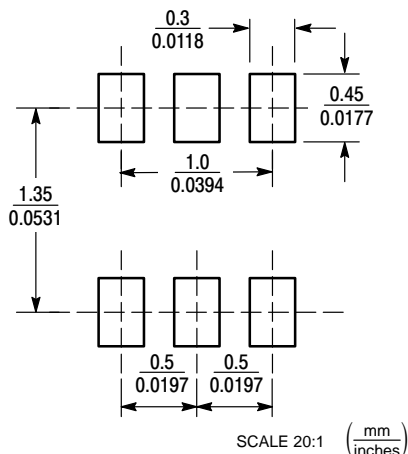
$t_p = 2 \mu\text{s}$   
 $t_r = 0.35 \text{ ns}$

Figure 4. Reverse Recovery Time Test Circuit for the NSDEMP11XV6T1

**INFORMATION FOR USING THE SOT-563 SURFACE MOUNT PACKAGE**  
**MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS**

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



**SOT-563**

**SOT-563 POWER DISSIPATION**

The power dissipation of the SOT-563 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by  $T_{J(max)}$ , the maximum rated junction temperature of the die,  $R_{\theta JA}$ , the thermal resistance from the device junction to ambient, and the operating temperature,  $T_A$ . Using the values provided on the data sheet for the SOT-563 package,  $P_D$  can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature  $T_A$  of 25°C, one can calculate the power dissipation of the device which in this case is 150 milliwatts.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{833^\circ\text{C/W}} = 150 \text{ milliwatts}$$

The 833°C/W for the SOT-563 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-563 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

**SOLDERING PRECAUTIONS**

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

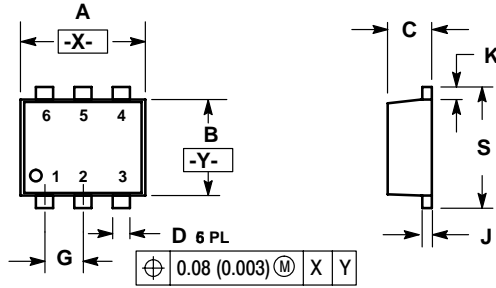
- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

\* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# NSDEMP11XV6T1, NSDEMP11XV6T5

## PACKAGE DIMENSIONS

### SOT-563, 6 LEAD CASE 463A-01 ISSUE O



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

#### STYLE 1:

- PIN 1. EMITTER 1
- 2. BASE 1
- 3. COLLECTOR 2
- 4. EMITTER 2
- 5. BASE 2
- 6. COLLECTOR 1

#### STYLE 2:

- PIN 1. EMITTER 1
- 2. EMITTER2
- 3. BASE 2
- 4. COLLECTOR 2
- 5. BASE 1
- 6. COLLECTOR 1


#### STYLE 3:

- PIN 1. CATHODE 1
- 2. CATHODE 1
- 3. ANODE/ANODE 2
- 4. CATHODE 2
- 5. CATHODE 2
- 6. ANODE/ANODE 1

#### STYLE 4:

- PIN 1. COLLECTOR
- 2. COLLECTOR
- 3. BASE
- 4. EMITTER
- 5. COLLECTOR
- 6. COLLECTOR

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