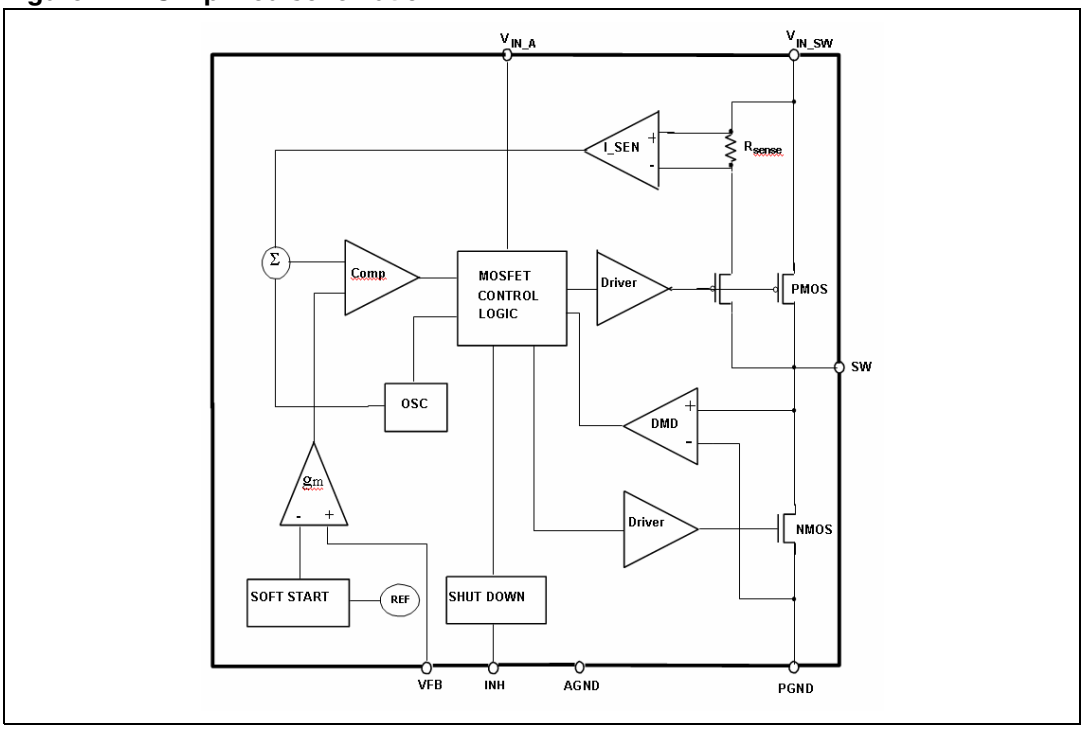
AN2620
Application note

3 A high-frequency synchronous 900 kHz step-down converter based on the ST1S10

Introduction

The ST1S10 is a step-down DC-DC converter with an optimized inhibit function for powering high-voltage LCD applications and low-voltage digital core HDD applications. Generally, it replaces the high current linear solution when high power dissipation is a problem. It provides up to 3 A over an input voltage range of 2.5 V to 18 V and synchronous rectification saves the external Schottky diode. A high internal switching frequency (0.9 MHz) allows it to use tiny surface-mount components, as well as the resistor divider, to set the output voltage value. Only an inductor and 3 capacitors are required. The current PWM mode architecture and stable operation with low E.S.R SMD ceramic capacitors results in low, predictable output ripple. To maximize the power conversion efficiency in light load, the regulator can work in burst mode automatically. The device can operate in PWM mode at a fixed frequency or synchronized to an external frequency. It switches at a frequency of 900 kHz when SYNC is connected to ground or a fixed voltage (less than 5.5 V) and synchronizes the switching frequency between 400 kHz to 1.2 MHz from the external clock that is applied to SYNC. A thermal shutdown circuit is integrated and activates at 150 °C. Cycle-by-cycle current limitation provides protection against shorted outputs. The on-chip 260 µs power-on reset ensures the proper operation when switching on the power supply. The quiescent current is less than 6 µA in the inhibit state. The device is available in MLP4x4 and SO-8 ePad packages.

Figure 1. Simplified schematic



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1 Application information component selection

1.1 Input capacitor

The ST1S10 features two V_{IN} pins: V_{IN_SW} for the power supply input voltage where the switching peak current is drawn, and V_{IN_A} to supply the ST1S10 internal circuitry and drivers. The V_{IN_SW} input capacitor reduces the current peaks drawn from the input power supply and reduces switching noise in the IC. High power supply source impedance requires larger input capacitance.

For the V_{IN_SW} input capacitor the RMS current rating is a critical parameter that must be higher than the RMS input current. The maximum RMS input current can be calculated using the following equation:

Equation 1

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta}}$$

where η is the expected system efficiency, D is the duty cycle and I_O the output DC current. This function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to IO divided by 2 (considering η= 1).

The maximum and minimum duty cycles are:

Equation 2

$$D_{MAX} = \frac{V_{out} + V_F}{V_{inMIN} - V_{SW}}$$

Equation 3

$$D_{MIN} = \frac{V_{out} + V_F}{V_{inMAX} - V_{SW}}$$

where V_F is the voltage drop across the internal NMOS and V_{SW} the voltage drop across the internal PDMOS. Considering the range D_{MIN} to D_{MAX} it is possible to determine the max I_{RMS} following through the input capacitor.

A minimum value of 4.7 µF for the V_{IN_SW} and a 0.1 µF ceramic capacitor for the V_{IN_A} are suitable in most application conditions. A 10 µF or higher ceramic capacitor for the V_{IN_SW} and a 1 µF (V_{IN_A}) are advisable in case of higher power supply source impedance or where it is needed to have long wires between the power supply source and the V_{IN} pins. The above suggested higher input capacitors values are also advisable in case of high output capacitive load which can impact the switching peak current drawn from the input capacitor during the startup transient.

It is also advisable to use ceramic capacitors with a voltage rating in the range of 1.5 times the maximum input voltage. The input capacitors should be located as close as possible to the V_{IN} pins.

Different capacitors can be considered:

- Electrolytic capacitors. These are the most commonly used because they are the least expensive and are available with a wide range of RMS current ratings. The only

drawback is that, considering a requested ripple current rating, they are physically larger than other capacitors.

- Ceramic capacitors. If available for the requested value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to the very low ESR). The drawback is the quite high cost.
- Tantalum capacitor. Very good tantalum capacitors are becoming available, with very low ESR and small size. The only problem is that they occasionally can burn if subjected to very high current during the charge. So, it is better to avoid this type of capacitor for the input filter of the device. In fact, they can be subjected to high surge current when connected to the power supply.

1.2 Output capacitor

The output capacitor is very important in satisfying the output voltage ripple requirement. Using a small inductor value to reduce the size of the choke is useful, but increases the current ripple. So, to reduce the output voltage ripple, a low ESR capacitor is required.

The most important parameters for the output capacitor are the capacitance, the ESR and the voltage rating.

The capacitance and the ESR affect the control loop stability, the output ripple voltage, and transient response of the regulator. The ripple due to the capacitance can be calculated by the following formula:

Equation 4

$$V_{ripple(C)} = \frac{0.125 \cdot \Delta I_{SW}}{F_S \cdot C_{out}}$$

where F_S is the PWM switching frequency and ΔI_{SW} is the inductor peak-to-peak switching current that can be calculated as:

Equation 5

$$\Delta I_{SW} = \frac{(V_{in} - V_{out})}{F_S \cdot L} \cdot D$$

where D is the duty cycle while the ripple due to the ESR is given by:

Equation 6

$$V_{ripple(ESR)} = \Delta I_{Sw} \cdot ESR$$

Use the above equations to define capacitor selection range, but final values should be verified by testing an evaluation circuit.

Lower ESR ceramic capacitors are usually advisable to reduce the output ripple voltage. Capacitors with higher voltage ratings have lower ESR values, providing lower output ripple voltage.

Also the capacitor ESL value impacts the output ripple voltage, but ceramic capacitors usually have very low ESL, making ripple voltages due to the ESL negligible. In order to reduce ripple voltages due to a parasitic inductive effect, keep the output capacitor connection paths as short as possible.

The ST1S10 has been designed to have the best performances with ceramic capacitors. In typical application conditions a minimum value of 22 µF ceramic capacitor is suggested on the output, but higher values are suitable considering that the control loop has been designed to properly work with a natural output LC frequency given by a 3.3 µH inductor and 22 µF output capacitor in the typical application (V_{in}=12 V, V_{out}=5 V).

It is advisable to use ceramic capacitors with a voltage rating in the range of 1.5 times the maximum output voltage.

1.3 Inductor

The inductor value is very important because it fixes the ripple current flowing through the output capacitor. The ripple current is usually fixed at 20-40% of I_{Omax}, that is 0.6-1.2 A with I_{Omax} = 3 A. The inductor value is approximately obtained by the following formula:

Equation 7

$$L = \frac{V_{in} - V_{out}}{\Delta I} \cdot T_{on}$$

where, T_{on} is the ON time of the internal switch, given by D · T.

For example, with V_{out} = 3.3 V, V_{in} = 5 V and ΔI_O = 0.45 A, the inductor value is about 2.8 µH. The peak current thought the inductor is given by:

Equation 8

$$I_{PK} = I_O + \frac{\Delta I}{2} \qquad I_{SAT} \geq I_{PK}$$

It can be seen that if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. So, for fixed the peak current, a higher value of the inductor allows a higher value for the output current.

The ST1S10 is designed to have maximum performance with a 3.3 µH inductor value at 900 kHz.

The peak inductor current must be designed in order to not exceed the switching current limit.

2 Thermal considerations

The dissipated power of the device is related to three different sources:

- Switch losses due to the non-negligible $R_{DS(on)}$. These are equal to:

Equation 9

$$P_{ON\_P} = R_{DS(on)\_P} \cdot I^2_{out} \cdot D$$

Equation 10

$$P_{ON\_N} = R_{DS(on)\_N} \cdot I^2_{out} \cdot (1 - D)$$

where, D is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between V_{out} and V_{in}, but in practical terms is quite higher than this value to compensate the losses of the overall application. Due to this reason, the switch losses related to the $R_{DS(on)}$ increase compared to the ideal case.

- Switch losses due to its turn-on and off. These are given by the following relationship:

Equation 11

where T_{on} and T_{off} are the overlap times of the voltage across the power switch and the current flowing into it during the turn-on and turn-off phases. T_{SW} is the equivalent switching time (typ. 30 ns).

- Quiescent current losses

Equation 12

$$P_Q = V_{in} \cdot I_Q$$

where I_Q is the quiescent current.

The junction temperature of device is:

Equation 13

$$T_J = T_A + Rth_{J-A} \cdot P_{TOT}$$

where T_A is the ambient temperature and Rth_{J-A} is the thermal resistance junction-to-ambient.

3 Short-circuit protection

In short condition, the ST1S10 has two short protection functions to avoid a damaged device.

- Overcurrent protection (OCP). The ST1S10 DC-DC converter is provided with a switch overcurrent protection. If the switch current limit is reached, in order to protect the application and the internal power switches and bonding wires, the device is immediately shut down and kept in this condition for a T_{off} period time (T_{off} = 135 µs typ) and turns on again for a T_{on} period (T_{on} = 22 µs typ with typical application conditions). This operation is repeated cycle by cycle. Normal operation is resumed when no overcurrent is detected.
- Overvoltage protection (OVP). In order to protect the whole application and reduce the total power dissipation during an overload or an output short-circuit condition, the device is provided with a dynamic short-circuit protection which works by internally monitoring the V_{FB} (feedback voltage). In case of overload or output short-circuit, if the V_{OUT} voltage is reduced causing the feedback voltage (V_{FB}) to drop below 0.3 V typ, the device goes in shutdown for T_{off} time (T_{off} = 288 µs typ) and turns on again for a T_{on} period (T_{on} = 130 µs typ). This operation is repeated cycle by cycle. Normal operation is resumed when no overload is detected (V_{FB} > 0.3 V typ) for a full T_{on} period. This dynamic operation can greatly reduce the power dissipation in overload condition, still ensuring excellent power-on startup, in most conditions.

4 Board usage recommendation

The board shown in *Figure 2* is provided with a Kelvin connection which means that for each pin two lines are available, one used to supply or sink current and the other one used to perform the needed measurement.

The ST1S10 inhibit pin should be connected to GND or V_{in}, by a jumper, in order to turn off or on the device.

If the SYNC pin is not used, it is better to connect to GND to avoid input noise to the device.

Figure 2. ST1S10 demonstration board typical diagram

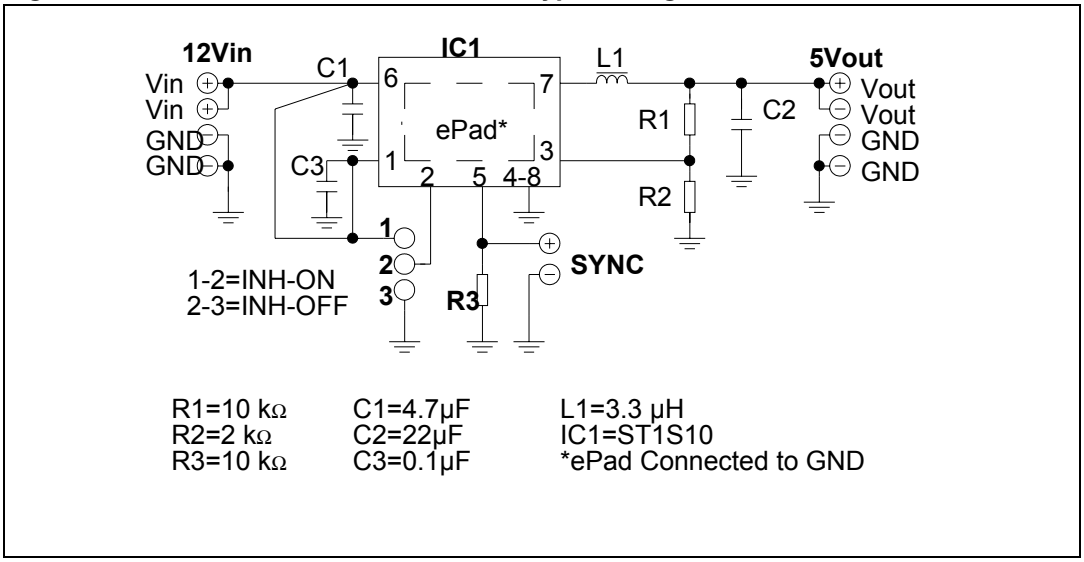


Figure 3. Demonstration board layout ST1S10 MLP package - top side

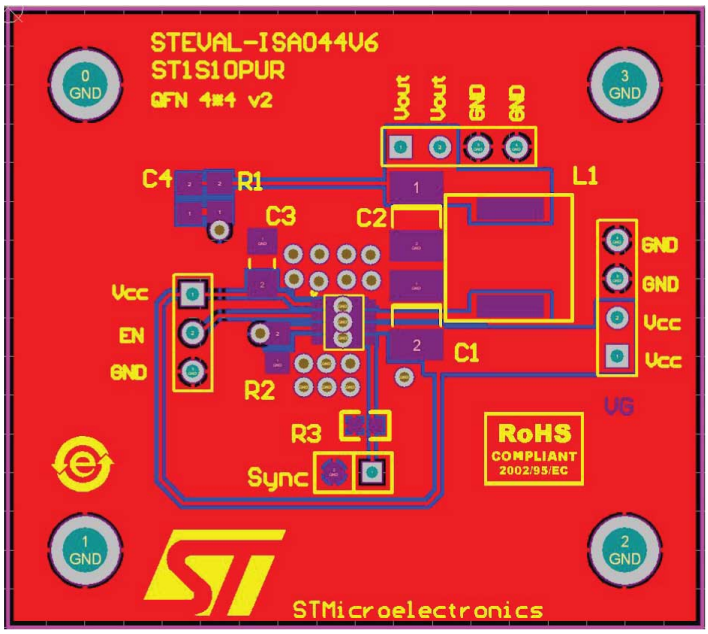


Figure 4. Demonstration board layout ST1S10 MLP package - bottom side

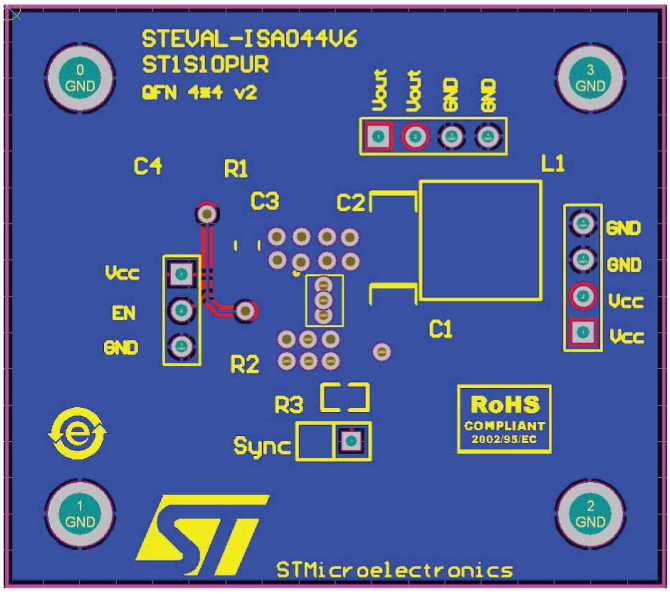


Figure 5. Demonstration board layout ST1S10 SO-8 ePad - top side

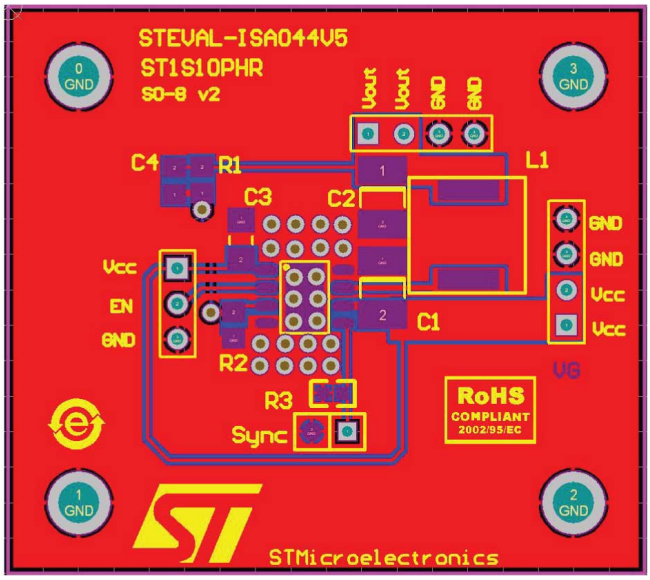


Figure 6. Demonstration board layout ST1S10 SO-8 ePad package - bottom side

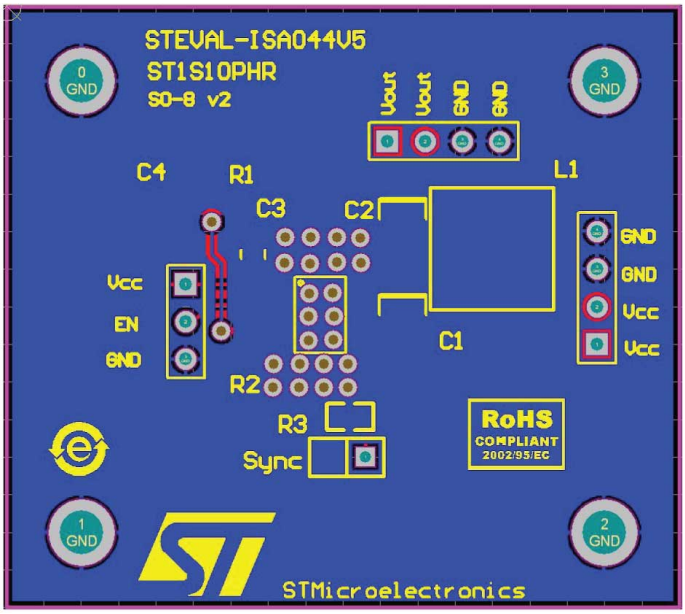


Figure 7. Enable jumper selection

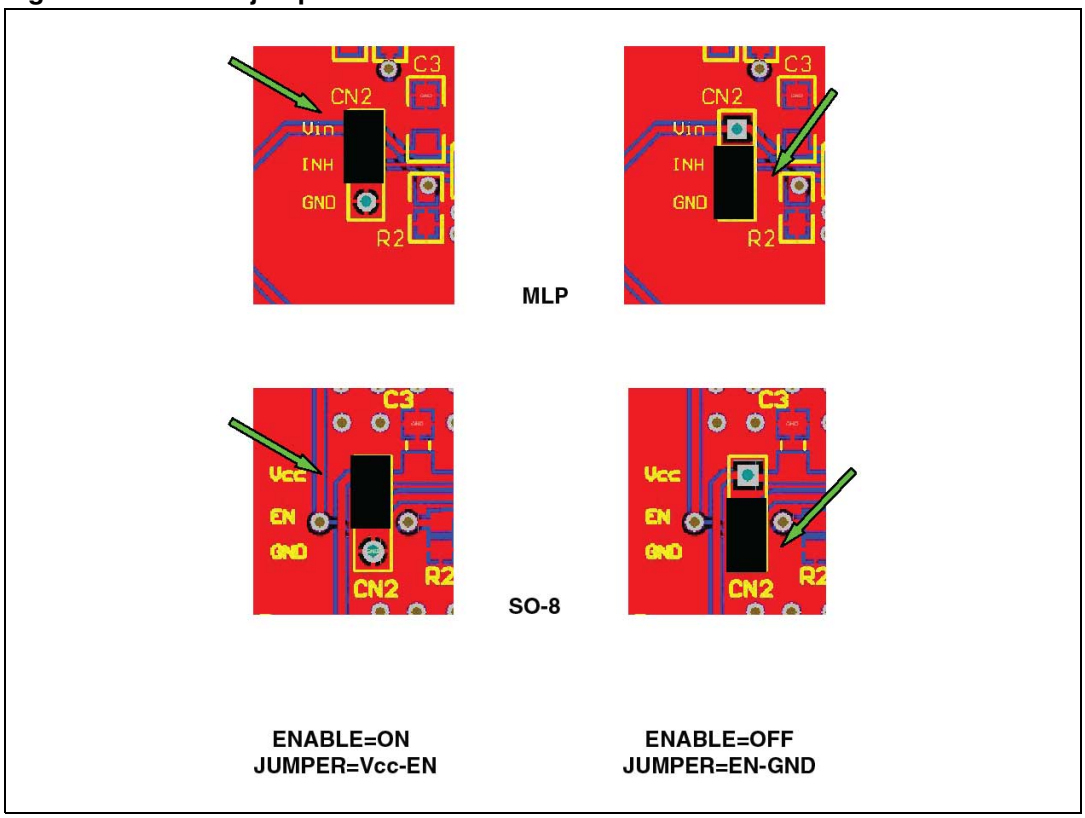
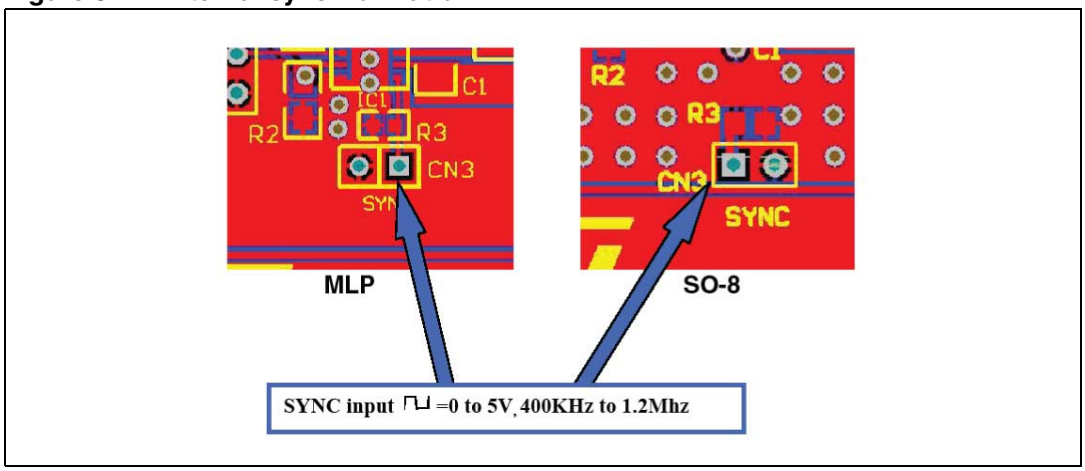


Figure 8. External synchronization



4.1 External component selection for the ST1S10 demonstration board

Figure 2 shows the typical application used to obtain an output voltage of 5 V.

In order to obtain the needed output voltage we must choose the resistor divider according to the following formula:

Equation 14

$$V_{out} = V_{FB} \cdot \left[1 + \frac{R1}{R2}\right]$$

where V_{FB} = 0.8 V and R2 suggested value is ~2 kΩ.

4.2 Inductor selection

Due to the high frequency (900 kHz) it is possible to use a very small inductor value.

We tested our device with an inductor value of 3.3 µH with very good efficiency performances.

As the device is able to provide an operative output current of 3 A, we strongly recommend using inductors able to manage at least 4.4 A.

4.3 Capacitors selection

It is possible to use any X5R or X7R ceramic capacitor

- C1 = 4.7 µF (ceramic) or higher
- C2 = 22 µF (ceramic) or higher, ESR=10 ~ 100 mΩ range
- C3 = 0.1 µF (ceramic) or higher

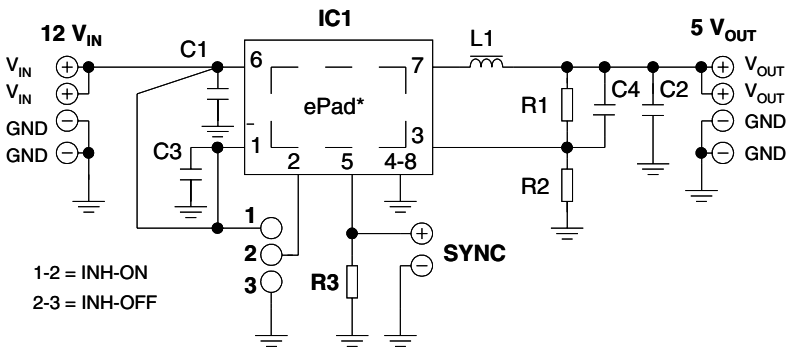
It is possible to put several capacitors in parallel in order to reduce the equivalent series resistor and improve the ripple present in the output voltage.

4.4 Heavy capacitive load condition

Thanks to the OCP and OVP circuit, the ST1S10 is strongly protected against short-circuit and overload damages. However, a highly capacitive load on the output may cause a difficult startup. This can be solved by using the modified application circuit shown in *Figure 9* in which a minimum of 10 µF for C1 and a 4.7 µF ceramic capacitor for C3 are used. Moreover, for C_{LOAD} >100 µF, it is needed to add the C4 capacitor in parallel to the upper voltage divider resistor (R1) as shown in *Figure 9*. The suggested value for C4 is 4.7 nF ~ 47 nF.

Note that the C4 may impact the control loop response and should be added only when a capacitive load higher than 100 µF is present at all times. If the high capacitive load is variable or not present at any time, in addition to C4 it is advisable to increase the output ceramic capacitor C2 from 22 µF to 47 µF (or use 2 x 22 µF capacitors in parallel). Also in this case it is advisable to further increase the input capacitors with a minimum of 10 µF for C1 and a 4.7 µF ceramic capacitor for C3 as shown in *Figure 10*.

Figure 9. ST1S10 application schematic for heavy capacitive load



R1 = 100 kΩ
R2 = 20 kΩ
R3 = 10 kΩ

C1 = 4.7 µF
C2 = 22 µF
C3 = 0.1~4.7 µF
C4 = 4.7 nF

L1 = 3.3 µH
IC1 = ST1S10
*ePad Connected to GND

4.5 Low output voltage (V_{out} < 2.5 V) and 2.5 V < V_{in} < 8 V

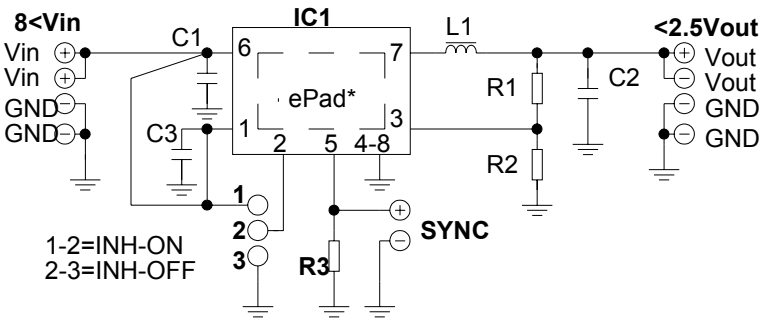
For applications with lower output voltage levels (V_{out} < 2.5 V) the output capacitance and the inductor values should be selected in a way that improves the DC-DC control loop behavior.

In this output condition two cases must be considered: V_{in} > 8 V and V_{in} < 8 V.

For V_{in} < 8 V the use of 2 x 22 µF capacitors in parallel to the output is recommended, as shown in *Figure 10*.

For V_{in} > 8 V, a 100 µF electrolytic capacitor with ESR < 0.1 should be added in parallel to the 2 x 22 µF output capacitors as shown in *Figure 11*.

Figure 10. ST1S10 application schematic for low output voltage (V_{out} < 2.5 V) and 2.5 V < V_{in} < 8 V

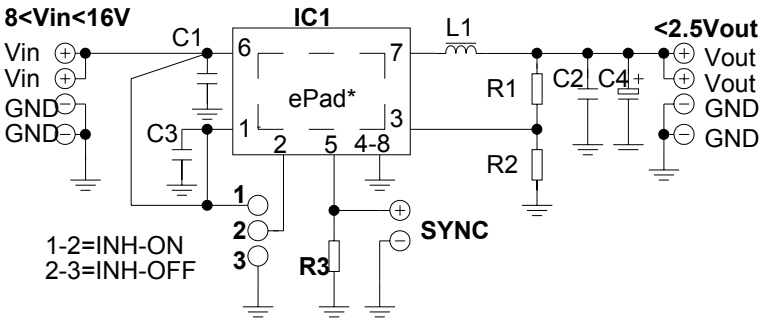


R1=*
R2=2 kΩ
R3=10 kΩ

C1=2*4.7 µF or 10 µF
C2=2*22 µF
C3=0.47~1 µF

L1=2.2 µH to 1 µH
IC1=ST1S10
*ePad Connected to GND

Figure 11. ST1S10 application schematic for low output voltage (V_{out} < 2.5 V) and 8 V < V_{in} < 16 V



R1=*
R2=2 kΩ
R3=10 kΩ

C1=2*4.7 µF or 10 µF
C2=2*22 µF
C3=4.7 µF
C4=100 µF el E.S.R.<0.1 Ω

L1=2.2 µH to 1 µH
IC1=ST1S10
*ePad Connected to GND

C4 suggested component:

Panasonic aluminium electrolytic capacitor FM series, part number - EEUFM1H101

100 µF 50 V impedance = 0.061 Ω at 100 kHz 20 °C

Table 1. Bill of material with most commonly used components

Name	Value	Material	Brand	P/N
C1	4.7 µF	Ceramic	TDK	C3216X7R1475K
			muRata	GRM21BR71A255KA12L
C2	22 µF		TDK	C3225X7R1C226M
			muRata	GRM32ER61C226KE20L
C3	0.1 µF		TDK	C1005X5R1E104K
			muRata	GRM319R71H104KA01
L	1 µH		TDK	RLF7030T-1R0N6R4
	2.2 µH		TDK	RLF7030T-2R2M5R4
	3.3 µH		TDK	RLF7030T-3R3M4R1

4.6 Layout considerations

The layout is an important step in the design for all switching power supplies.

The high-speed operation (900 kHz) of the ST1S10 device demands careful attention to the PCB layout. Care must be taken in the board layout to obtain maximum device performance, otherwise the regulator could show poor line and load regulation, stability issues as well as EMI problems.

It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths.

The input capacitor must be placed as close as possible to the IC pins as well as the inductor and output capacitor. Use a common ground node for power ground and a different one for control ground (AGND) to minimize the effects of ground noise. Connect these ground nodes together underneath the device and make sure that small signal components returning to the AGND pin do not share the high current path of C_{IN} and C_{OUT}.

The feedback voltage sense line (V_{FB}) should be connected right to the output capacitor and routed away from noisy components and traces (e.g., SW line). Its trace should be minimized and shielded by a guard-ring connected to the ground.

Figure 12. PCB layout suggestion

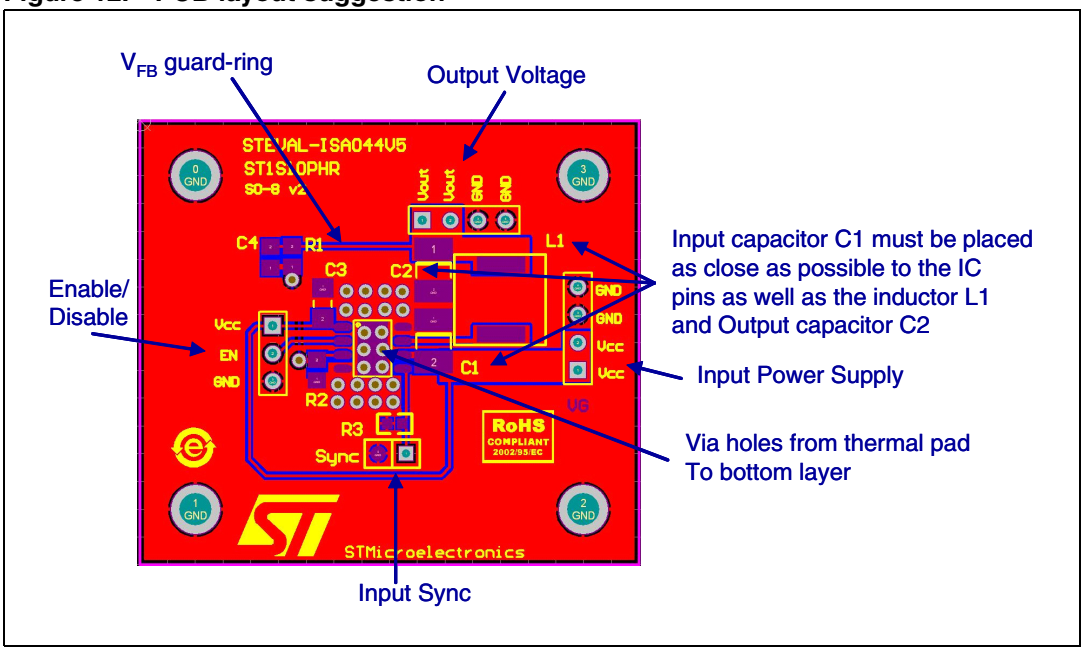


Figure 13. PCB layout Vin_A and Vin_SW detail

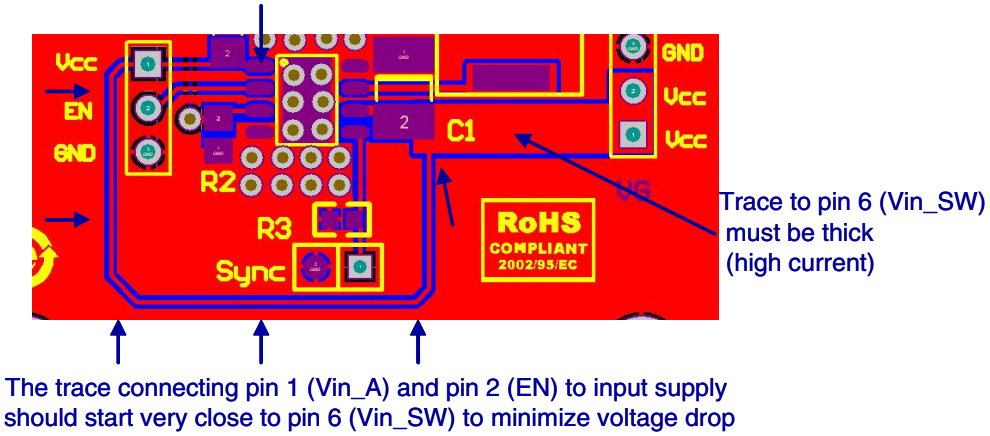
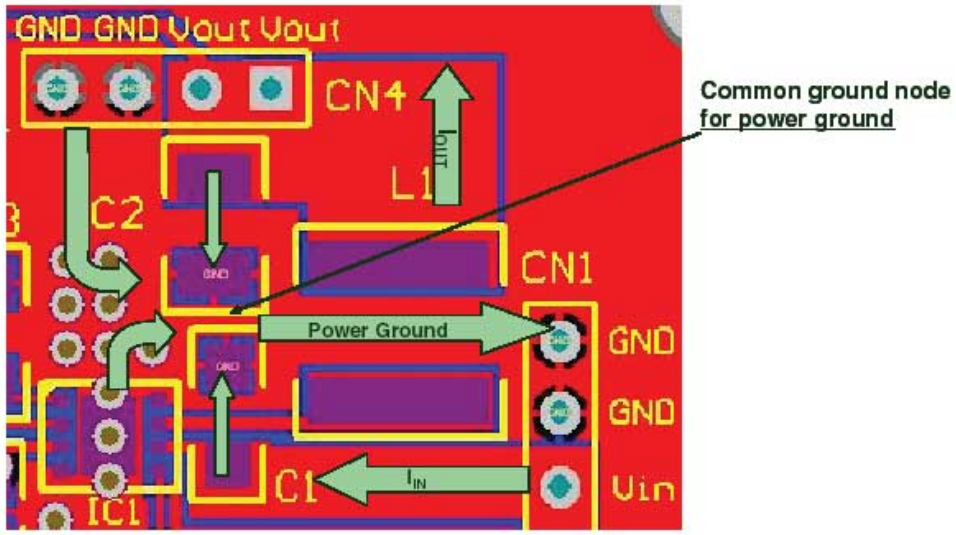


Figure 14. PCB layout details



Equation 15

$$I_{IN} = I_{POWERGROUND} = I_{OUT} + I_{DEVICE} + I_{C1} + I_{C2}$$

5 Layout thermal considerations

The leadframe die pad of the ST1S10 is exposed at the bottom of the package and must be soldered directly to a properly designed thermal pad on the PCB (ground copper area used as a heat sink).

The addition of thermal vias from the thermal pad to an internal or bottom ground plane helps to increase the power dissipation.

6 Revision history

Table 2. Document revision history

Date	Revision	Changes
20-Aug-2008	1	Initial release
04-Nov-2008	2	Title changed on cover page to improve readability
13-May-2010	3	Modified: *Figure 9 on page 14*, *Figure 12* and *Figure 13 on page 17*