

General Description

The EC8320 is a high performance positive voltage regulator designed for use in applications requiring very low input voltage and very low dropout voltage at up to 2 amps. It operates with a V_{IN} as low as 1.6V and VPP voltage 5V with output voltage programmable as low as 0.8V. The EC8320 features ultra low dropout, ideal for applications where V_{OUT} is very close to V_{IN} .

Additionally, the EC8320 has an enable pin to further reduce power dissipation while shutdown. The EC8320 provides excellent regulation over variations in line, load and temperature. The EC8320 provides a power OK signal to indicate if the voltage level of V_O reaches 92% of its rating value.

The EC8320 is available in the power SOP-8(Exposed PAD) package. It is available with 1.2V, 1.5V, 1.8V and 2.5V internally preset outputs that are also adjustable using external resistors.

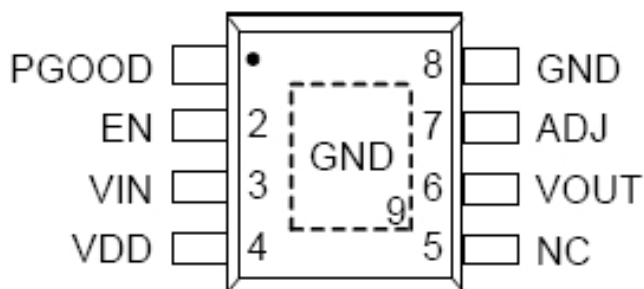
Features

- Adjustable Output Low to 0.8V
- Input Voltage as Low as 1.6V and VPP Voltage 5V
- 240mV Dropout @ 2A
- Over Current and Over Temperature Protection
- Enable Pin
- Low Reverse Leakage (Output to Input)
- Power SOP-8(EP) Packages with Thermal Pad
- $\pm 2\%$ Output Voltage
- V_O Power OK Signal
- 1.2V, 1.5V, 1.8V, 2.5V Options and Adjustable
- Externally Using Resistors
- V_O Pull Low Resistance when Disable

Applications

- Motherboards
- Peripheral Cards
- Network Cards
- Set Top Boxes
- Notebook Computers

Pin Assignments



Pin Description

PIN	NAME	Description
1	PGOOD	Assert high once VO reaches 92% of its rating voltage. Open-drain output.
2	EN	Enable Input. (Active High)
3	VIN	Input voltage. Large bulk capacitance should be placed closely to this pin. A 10µF ceramic capacitor is recommended at this pin.
4	VDD	Input voltage for controlling circuit.
5	NC	Not connected.
6	VOOUT	The power output of the device. A pull low resistance exists when deactivate device by VEN.
7	ADJ	This pin, EC8320A/B when grounded, sets the output voltage by the internal feedback resistors. If external feedback resistors are used, the output voltage will be $VO = 0.8(R1+R2)/R2$ Volts.
8	GND	Reference ground.

Ordering Information

EC8320 X XX XX X

Enable Pin Function & ADJ Pin Function
 A—Enable Pin : Internal Pull High, Active High
 ADJ Pin : grounded output voltage by the internal feedback resistors
 B—Enable Pin : Internal Pull Low, Active High
 ADJ Pin : grounded output voltage by the internal feedback resistors

R : Tape & Reel

Package Type :
 MH : SOP-8
 (Exposed PAD)

Output Voltage :
 12 : 1.2V
 15 : 1.5V
 18 : 1.8V
 25 : 2.5V
 AJ : ADJ

Part Number	Package	Marking	Marking Information
EC8320AXXMHR	SOP-8 (Exposed PAD)	8320A XXLLL YYWWT	1. XX: Output Voltage (Ex- 12:1.2V; AJ:ADJ) 2. LLL: Last three number of Lot No 3. YYWW: Date Code 4. T: Internal Tracking Code
EC8320BXXMHR		8320B XXLLL YYWWT	

Package Types

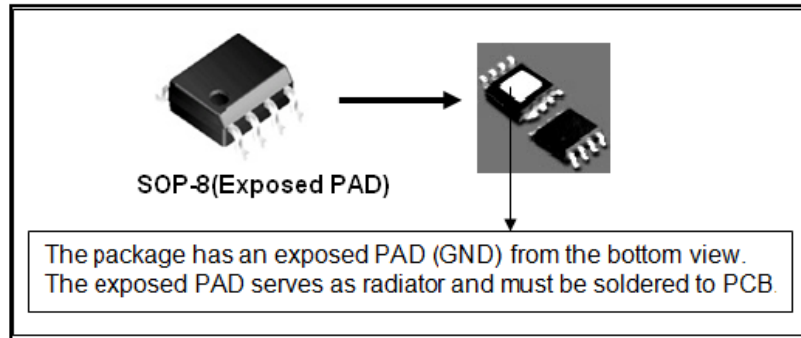


Figure 1. Package Types of EC8320

Function Block Diagram

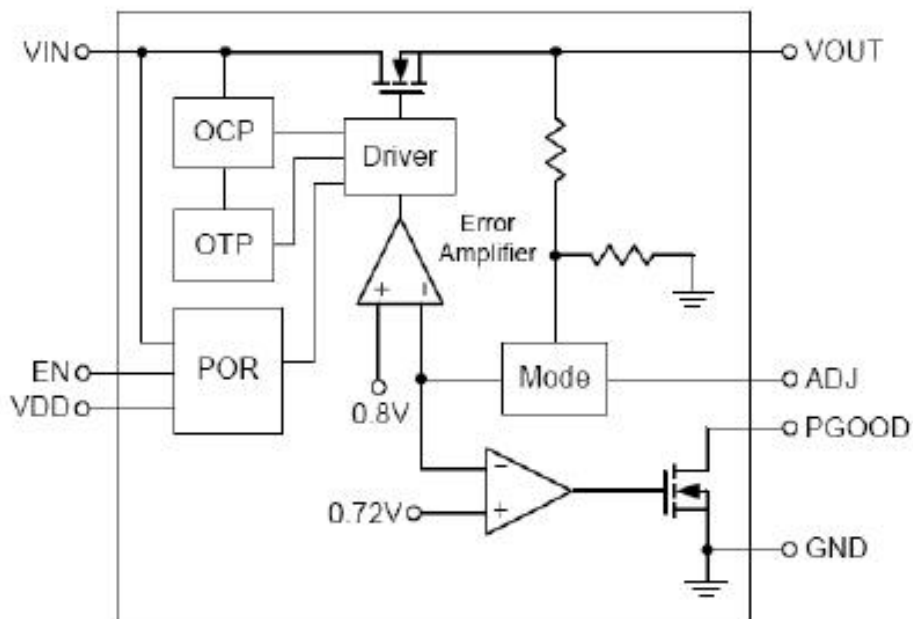


Figure2:Functional Block Diagram of EC8320



Absolute Maximum Ratings

Parameter	Rating	Unit
VCNTL Supply Voltage (VCNTL to GND)	-0.3 ~ 6	V
VIN Supply Voltage (VIN to GND)	-0.3 ~ 6	V
VOUT to GND Voltage	-0.3 ~ VIN+0.3	V
PGOOD to GND Voltage	-0.3 ~ 7	V
EN, ADJ to GND Voltage	-0.3 ~ VCNTL+0.3	V
Power Dissipation	Internally Limited	
Maximum Junction Temperature	150	°C
Storage Temperature Range	-65°C ≤ T _J ≤ +150	°C
Lead Temperature (soldering, 10sec)	260	°C
Thermal Resistance Junction to Ambient	50	°C/W
Thermal Resistance Junction to Case	20	°C/W
Operating Temperature Range	-40 to +125	°C
Storage Temperature	-65 to +150	°C
ESD Rating (Human Body Model)	2000	V

Note1: Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit	
VDD	VCNTL Supply Voltage	3.0 ~ 5.5	V	
VIN	VIN Supply Voltage	1.2 ~ 5.5	V	
VOUT	VOUT Output Voltage (when VCNTL-VOUT>1.7V)	0.8 ~ VIN – VDROPP	V	
IOUT	VOUT Output Current	0~2	A	
R2	ADJ to GND	1K ~ 24K	Ω	
COUT	VOUT Output Capacitance	IOUT = 2A at 25% nominal VOUT	8~770	uF
		IOUT = 1A at 25% nominal VOUT	8~1400	
		IOUT = 0.5A at 25% nominal VOUT	8~1700	
ESRCOUT	ESR of VOUT Output Capacitor	0 ~ 200	mΩ	
TA	Ambient Temperature	-40 ~ 85	°C	
TJ	Junction Temperature	-40 ~ 125	°C	



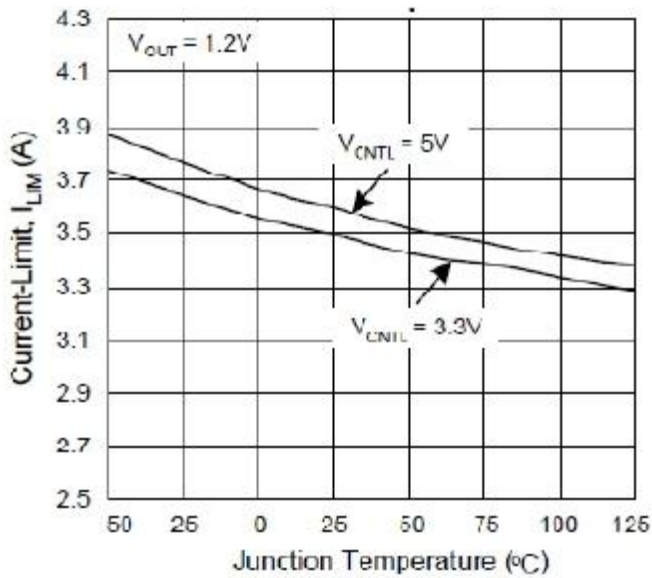
Electrical Characteristics

Note: Refer to the typical application circuits. These specifications apply over $V_{CNTL}=5V$, $V_{IN}=1.8V$, $V_{OUT}=1.2V$, and $T_A = -40 \sim 85^{\circ}C$, unless otherwise specified. Typical values are at $T_J=25^{\circ}C$.

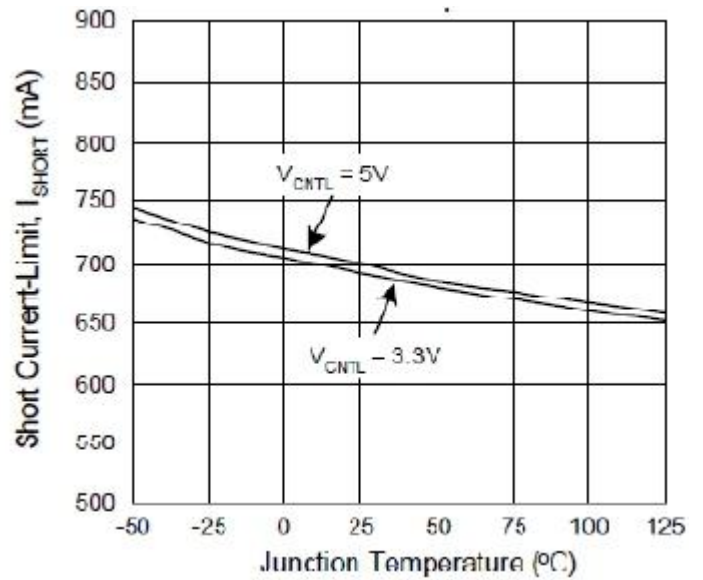
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	POR Threshold		2.4	2.7	3	V
	POR Hysteresis		0.15	0.2		V
V_{TH_ADJ}	Adjustable Pin Threshold	$I_{OUT}=1mA$		0.2	0.4	V
V_{ADJ}	Reference Voltage	$I_{OUT}=1mA$	0.784	0.8	0.816	V
ΔV_{OUT}	Fixed Output Voltage Range		-2	0	+2	%
ΔV_{LINE_IN}	Line Regulation(V_{IN})	$V_{IN}=V_{OUT}+0.5V$ TO 5V $I_{OUT}=1mA$		0.2	0.6	%
ΔV_{LOAD}	Load Regulation	$V_{IN}=V_{OUT}+1V$ $I_{OUT}=1mA$ TO 2A		0.1	1	%
V_{DROP}	Dropout Voltage	$I_{OUT}= 2A$		150	250	mV
I_Q	Quiescent Current	$V_{DD}=5.5V$		0.6	1.2	mA
I_{LIM}	Current Limit		2.8	3.2		A
	Short Circuit Current	$V_{OUT}<0.2V$	0.5	1.8		A
	In-rush Current	$C_{OUT}=10\mu F$, Enable Start-up		0.6		A
	V_{OUT} Pull-Low Resistance	$V_{EN}=0V$		150		Ω
Chip Enable						
I_{EN}	EN Input Bias Current	$V_{EN}=0V$		12		μA
I_{SHDN}	VDD Shutdown Current	EC8320A		10	20	μA
		EC8320B			1	
V_{ENL}	EN Threshold	Logic-Low Voltage	-	-	0.2	V
		Logic-High Voltage	1.2			
Power Good						
	PGOOD Rising Threshold			90	93	%
	PGOOD Hysteresis		3	10	-	%
	PGOOD Sink Capability	$I_{PGOOD}=10mA$		0.2	0.4	V
	PGOOD Delay		0.5	1.5	5	mS
Thermal Protection						
T_{SD}	Thermal Shutdown Temperature		-	160	-	$^{\circ}C$
ΔT_{SD}	Thermal Shutdown Hysteresis		-	30	-	$^{\circ}C$
	Thermal Shutdown Temperature Fold-back	$V_{OUT}<0.4V$	-	110	-	$^{\circ}C$

Typical Operating Characteristics

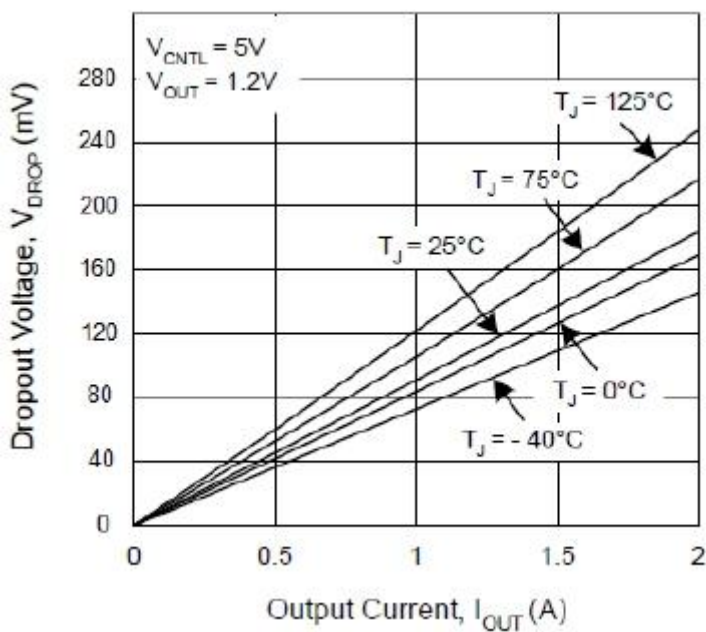
Current-Limit vs. Junction Temperature



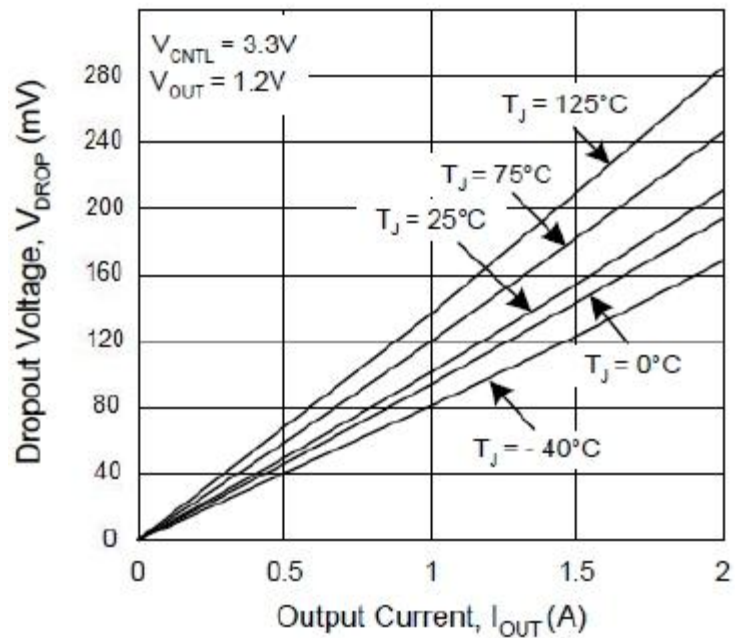
Short Current-Limit vs. Junction Temperature



Dropout Voltage vs. Output Current

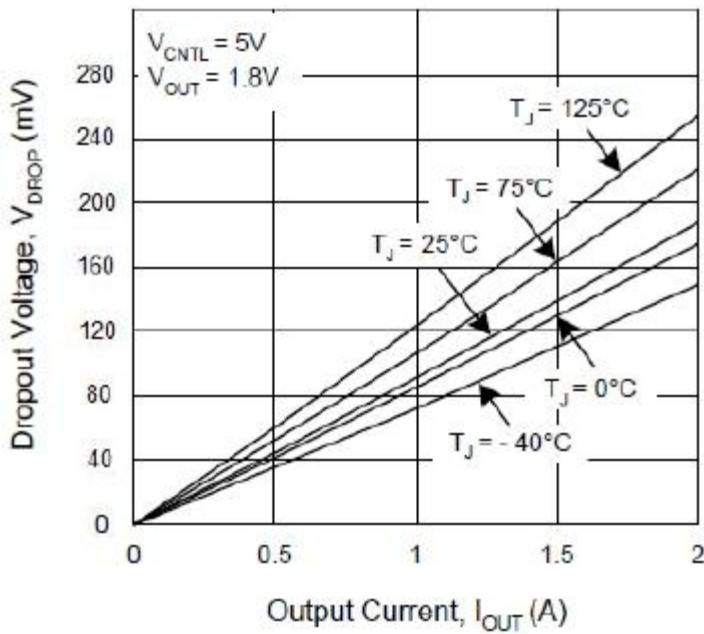


Dropout Voltage vs. Output Current

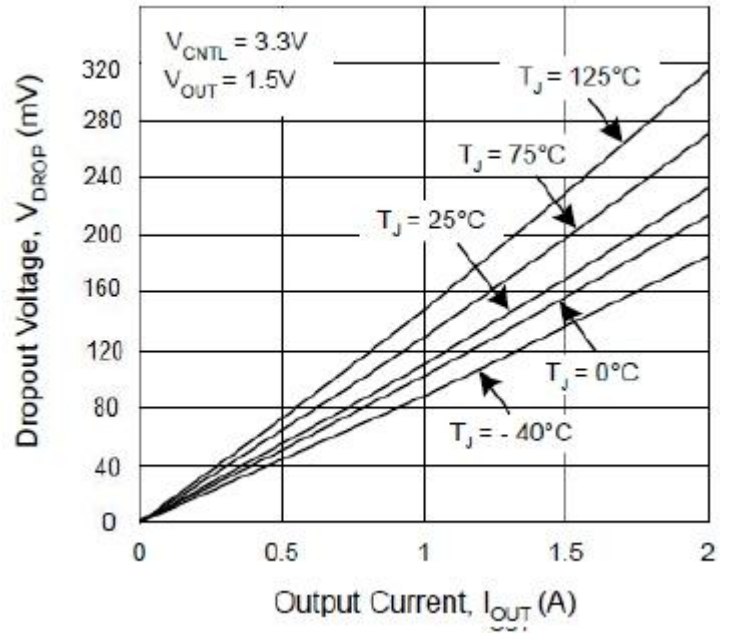


Typical Operating Characteristics(Cont.)

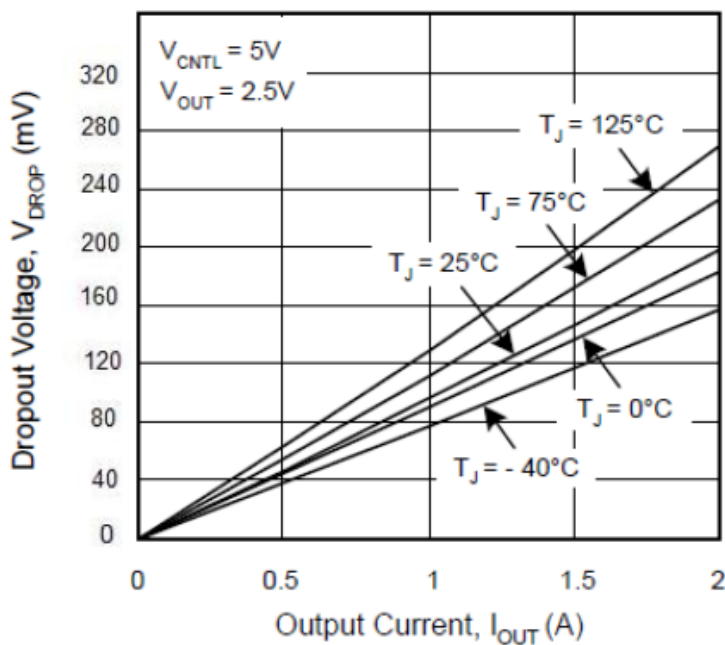
Dropout Voltage vs. Output Current



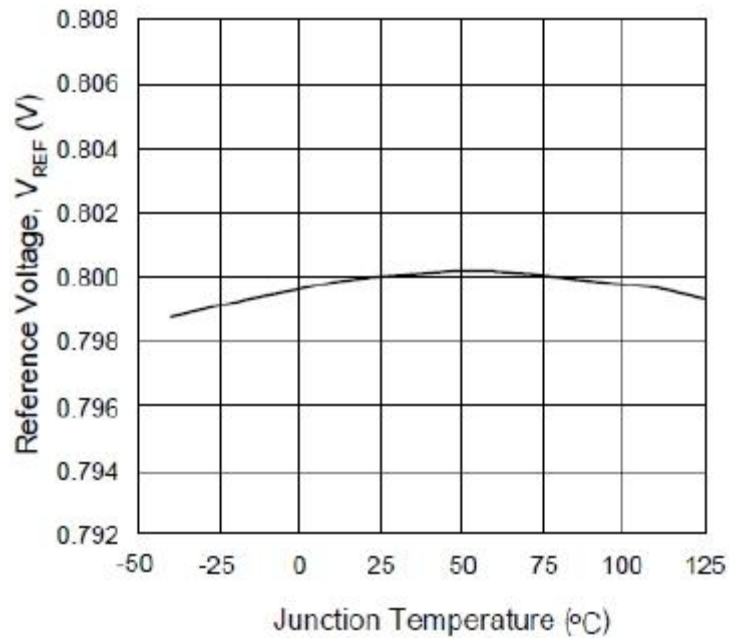
Dropout Voltage vs. Output Current



Dropout Voltage vs. Output Current

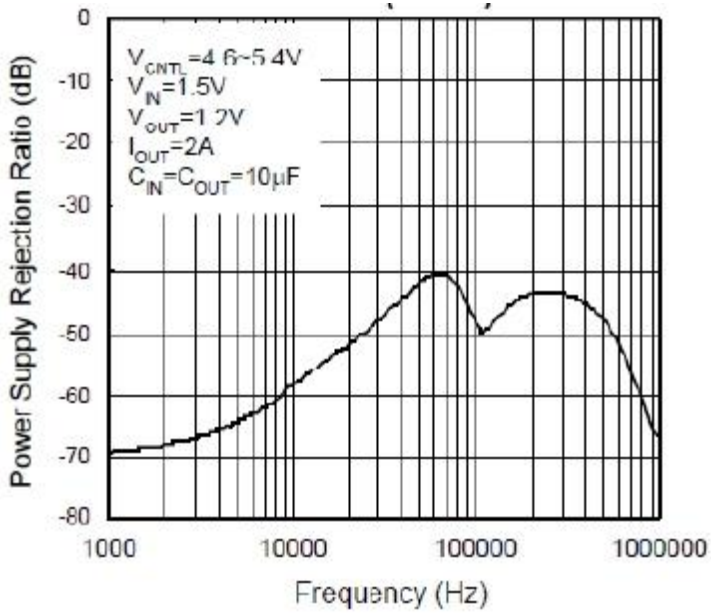


Reference Voltage vs. Junction Temperature

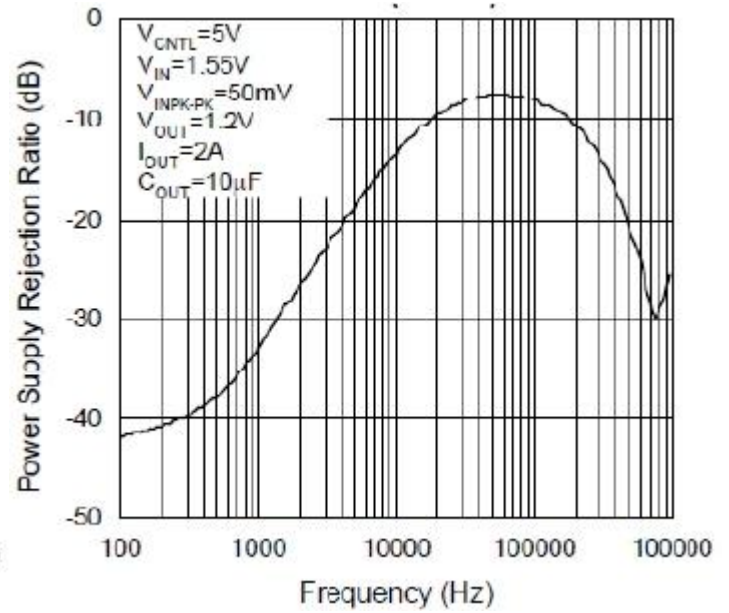


Typical Operating Characteristics(Cont.)

VCNTL Power Supply Rejection Ratio(PSRR)



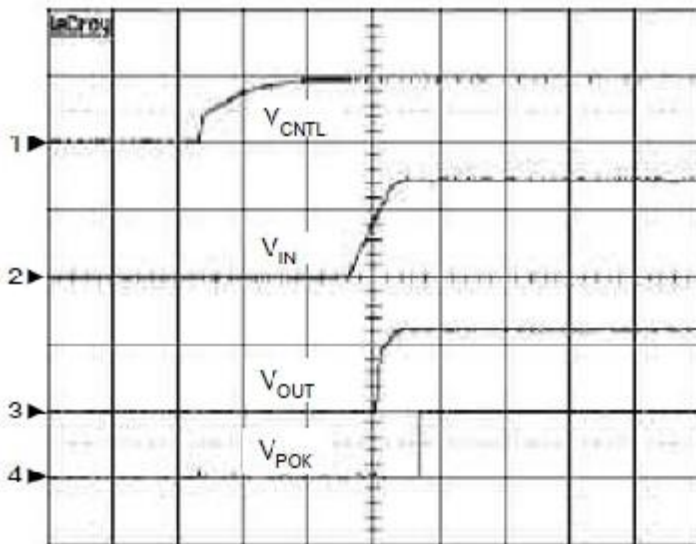
VIN Power Supply Rejection Ratio(PSRR)



Operating Waveforms

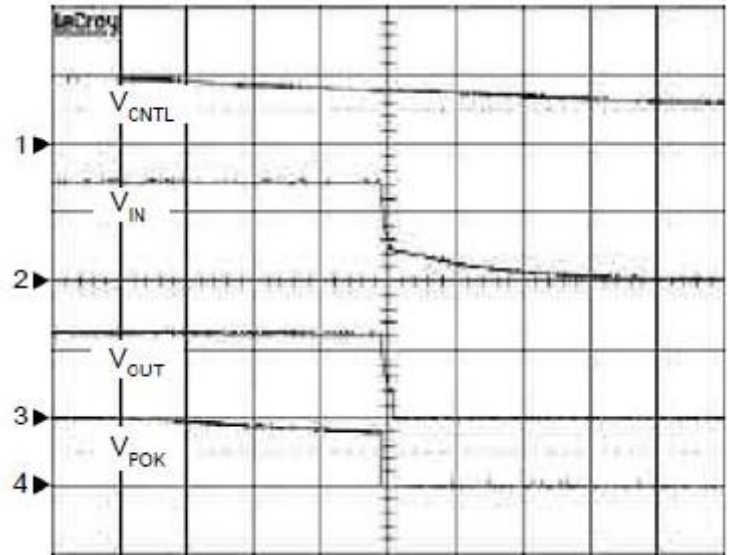
Refer to the typical application circuit. The test condition is $V_{IN}=1.5V$, $V_{CNTL}=5V$, $V_{OUT}=1.2V$, $T_A=25^\circ C$ unless otherwise specified

Power On



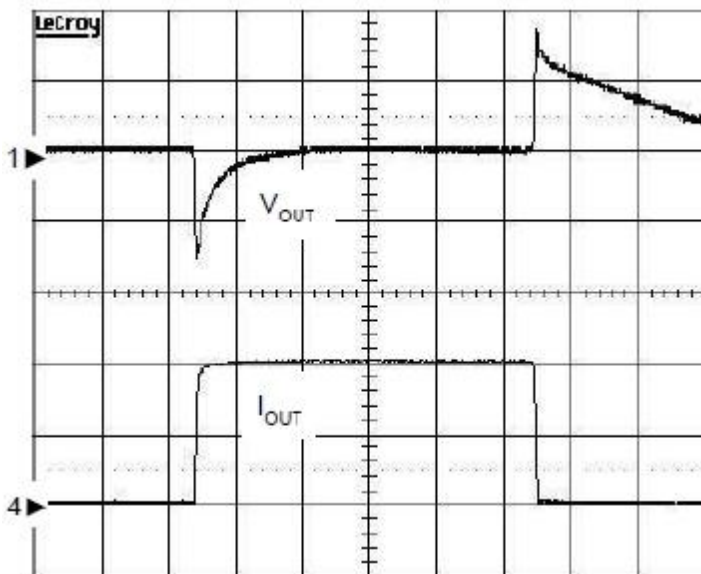
$C_{OUT}=10\mu F$, $C_{IN}=10\mu F$, $R_L=0.6\Omega$ / TIME: 5ms/Div
 CH1: V_{CNTL} , 5V/Div, DC/CH2: V_{IN} , 1V/Div, DC
 CH3: V_{OUT} , 1V/Div, DC/CH4: V_{POK} , 5V/Div, DC

Power Off



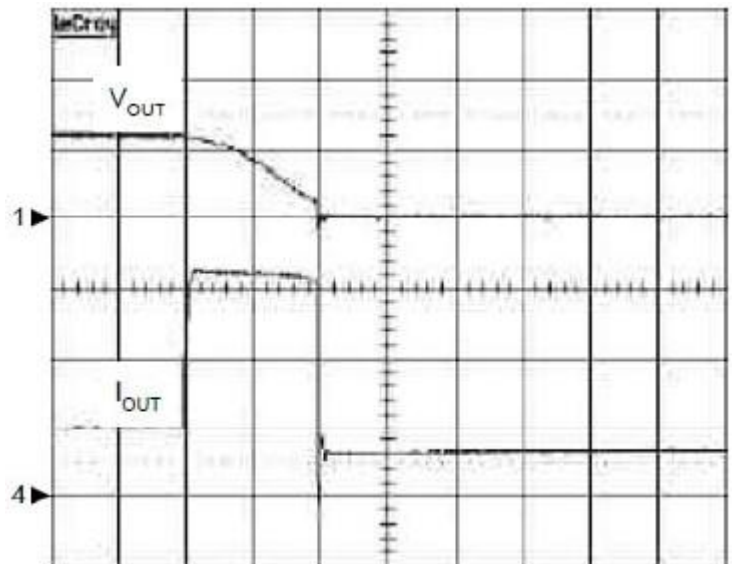
$C_{OUT}=10\mu F$, $C_{IN}=10\mu F$, $R_L=0.6\Omega$ / TIME: 10ms/Div
 CH1: V_{CNTL} , 5V/Div, DC/CH2: V_{IN} , 1V/Div, DC
 CH3: V_{OUT} , 1V/Div, DC/CH4: V_{POK} , 5V/Div, DC

Load Transient Response



$I_{OUT}=10mA$ to $2A$ to $10mA$ (rise / fall time = 1us) $C_{OUT}=10\mu F$, $C_{IN}=10\mu F$
 CH1: V_{OUT} , 50mV/Div, AC/CH4: I_{OUT} , 1A/Div, DC/ TIME: 20us/Div

Over Current Protection

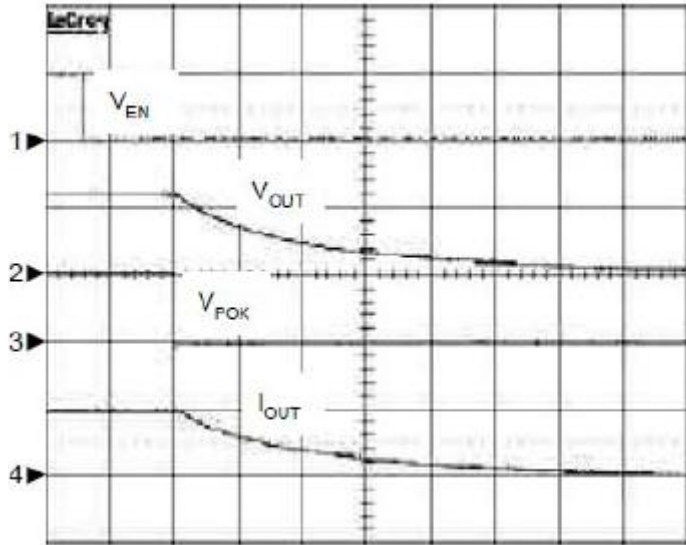


$C_{OUT}=10mF$, $C_{IN}=10mF$, $I_{OUT}=1A$ to $3.4A$
 CH1: V_{OUT} , 1V/Div, DC/ CH4: I_{OUT} , 1A/Div, DC/ TIME: 0.2ms/Div

Operating Waveforms(Cont.)

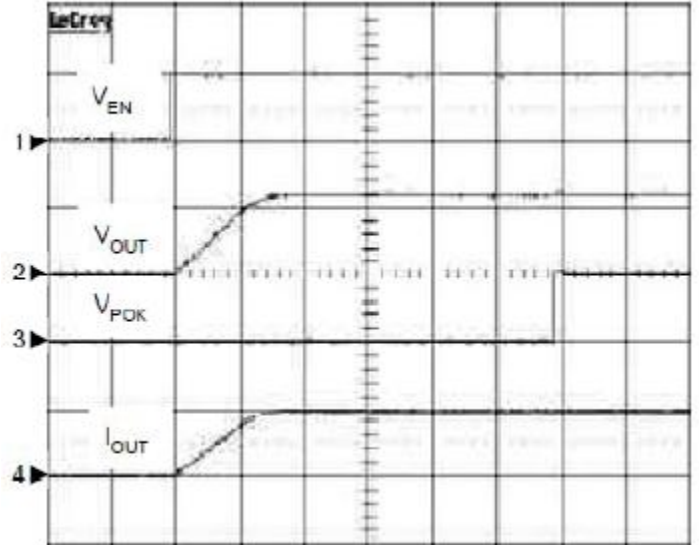
Refer to the typical application circuit. The test condition is $V_{IN}=1.5V$, $V_{CNTL}=5V$, $V_{OUT}=1.2V$, $T_A=25^\circ C$ unless otherwise specified

Shutdown



$C_{OUT}=10mF$, $C_{IN}=10mF$, $R_L=0.6W$ / TIME: 5us/Div
 CH1: V_{EN} , 5V/Div, DC/CH2: V_{OUT} , 1V/Div, DC
 CH3: V_{POK} , 5V/Div, DC/CH4: I_{OUT} , 2A/Div, DC

Enable



$C_{OUT}=10mF$, $C_{IN}=10mF$, $R_L=0.6W$ / TIME: 0.5ms/Div
 CH1: V_{EN} , 5V/Div, DC/CH2: V_{OUT} , 1V/Div, DC
 CH3: V_{POK} , 5V/Div, DC/CH4: I_{OUT} , 2A/Div, DC

Typical Application Circuit

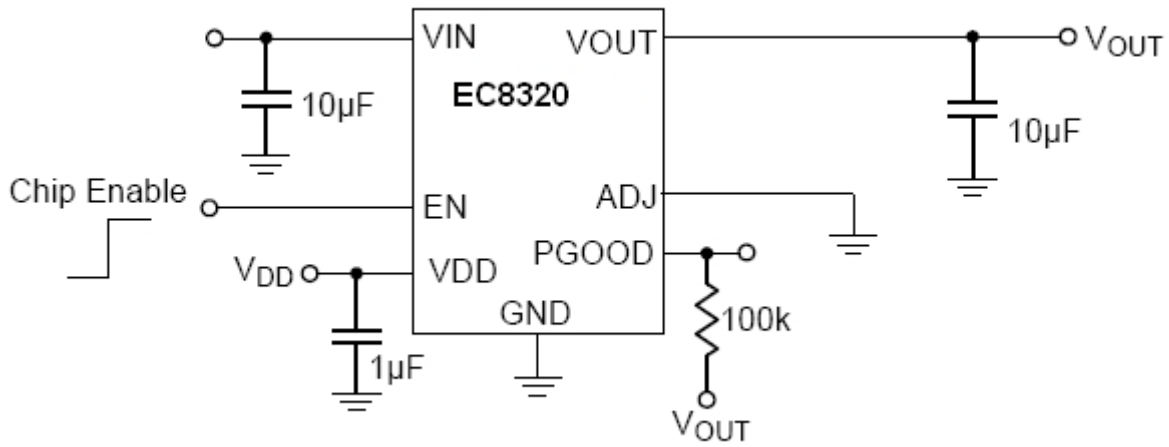


Figure3:Fixed Voltage Regulator Application Circuit of EC8320A/B

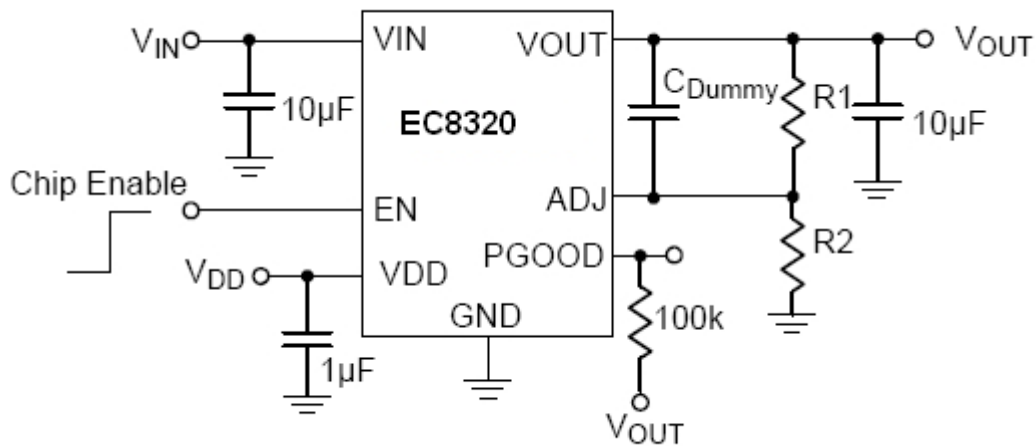


Figure4:Adjustable Voltage Regulator Application Circuit of EC8320A/B

Function Description

Power-On-Reset

A Power-On-Reset (POR) circuit monitors both of supply voltages on VCNTL and VIN pins to prevent wrong logic controls. The POR function initiates a soft-start process after both of the supply voltages exceed their rising POR voltage thresholds during powering on. The POR function also pulls low the POK voltage regardless of the output status when one of the supply voltages falls below its falling POR voltage threshold.

Internal Soft-Start

An internal soft-start function controls rise rate of the Output voltage to limit the current surge during start-up. The typical soft-start interval is about 0.6ms.

Output Voltage Regulation

An error amplifier working with a temperature compensated 0.8V reference and an output NMOS regulates output to the preset voltage. The error amplifier is designed with high bandwidth and DC gain provides very fast transient response and less load regulation. It compares the reference with the feedback voltage and amplifies the difference to drive the output NMOS which provides load current from VIN to VOUT.

Current-Limit Protection

The EC8320 monitors the current flowing through the output NMOS and limits the maximum current to prevent load and EC8320 from damages during current overload conditions.

Short Current-Limit Protection

The short current-limit function reduces the current-limit level down to 0.8A (typical) when the voltage on ADJ pin falls below 0.2V (typical) during current overload or shortcircuit conditions.

The short current-limit function is disabled for successful start-up during soft-start.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of EC8320. When the junction temperature exceeds +170 °C, a thermal sensor turns off the output NMOS, allowing the device to cool down.

The regulator regulates the output again through initiation of a new soft-start process after the junction temperature cools by 50°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown is designed with a 50 °C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending lifetime of the device. For normal operation, the device power dissipation should be externally limited so that junction temperatures will not exceed +125 °C.

Enable Control

The EC8320A/B has a dedicated enable pin (EN). EC8320A: A logic low signal applied to this pin shuts down the output. Following a shutdown, a logic high signal re-enables the output through initiation of a new soft-start cycle. When left open, this pin is pulled up by an internal current source (5uA typical) to enable normal operation. It's not necessary to use an external transistor to Save Cost.

Function Description(Cont.)

EC8320B: A logic low signal applied to this pin shuts down the output. Following a shutdown, a logic high signal re-enables the output through initiation of a new soft-start cycle. When left open, this pin is pulled up by an internal current source (5uA typical) to turn off operation.

Power-OK and Delay

The EC8320 indicates the status of the output voltage by monitoring the feedback voltage (V_{ADJ}) on ADJ pin. As the V_{ADJ} rises and reaches the rising Power-OK voltage threshold (V_{THPOK}), an internal delay function starts to work. At the end of the delay time, the IC turns off the internal NMOS of the POK to indicate the output is ok. As the V_{ADJ} falls and reaches the falling Power-OK voltage threshold, the IC turns on the NMOS of the POK (after a debounce time of 10ms typical).

Application Information

Power Sequencing

The power sequencing of VIN and VCNTL is not necessary to be concerned. However, do not apply a voltage to VOUT for a long time when the main voltage applied at VIN is not present. The reason is the internal parasitic diode from VOUT to VIN conducts and dissipates power without protections due to the forward-voltage.

Output Capacitor

The EC8320 requires a proper output capacitor to maintain stability and improve transient response. The output capacitor selection is dependent upon ESR (equivalent series resistance) and capacitance of the output capacitor over the operating temperature.

Ultra-low-ESR capacitors (such as ceramic chip capacitors) and low-ESR bulk capacitors (such as solid tantalum, POSCap, and Aluminum electrolytic capacitors) can all be used as output capacitors.

During load transients, the output capacitors which is depending on the stepping amplitude and slew rate of load current, are used to reduce the slew rate of the current seen by the EC8320 and help the device to minimize the variations of output voltage for good transient response. For the applications with large stepping load current, the low-ESR bulk capacitors are normally recommended.

Decoupling ceramic capacitors must be placed at the load and ground pins as close as possible and the impedance of the layout must be minimized.

Input Capacitor

The EC8320 requires proper input capacitors to supply current surge during stepping load transients to prevent the input voltage rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the surge currents, more parasitic inductance needs more input capacitance.

Ultra-low-ESR capacitors (such as ceramic chip capacitors) and low-ESR bulk capacitors (such as solid tantalum, POSCap, and Aluminum electrolytic capacitors) can all be used as an input capacitor of VIN.

For most applications, the recommended input capacitance of VIN is 10uF at least. However, if the drop of the input voltage is not cared, the input capacitance can be less than 10uF. More capacitance reduces the variations of the supply voltage on VIN pin.

Setting The Output Voltage

The output voltage is programmed by the resistor divider connected to ADJ pin. The preset output voltage is calculated by the following equation :

$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2} \right)$$

where R1 is the resistor connected from VOUT to ADJ with Kelvin sensing connection and R2 is the resistor connected from ADJ to GND. A bypass capacitor(C1) may be connected with R1 in parallel to improve load transient response and stability.

Layout Consideration(See Figure A)

1. Please solder the Exposed Pad on the system ground pad on the top-layer of PCBs. The ground pad must have wide size to conduct heat into the ambient air through the system ground plane and PCB as a heat sink.
2. Please place the input capacitors for VIN and VCNTL pins near the pins as close as possible for decoupling high-frequency ripples.
3. Ceramic decoupling capacitors for load must be placed near the load as close as possible for decoupling high-frequency ripples.
4. To place EC8320 and output capacitors near the load reduces parasitic resistance and inductance for excellent load transient response.
5. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
6. Large current paths, shown by bold lines on the figure A, must have wide tracks.
7. Place the R1, R2, and C1 (option) near the EC8320 as close as to avoid noise coupling.
8. Connect the ground of the R2 to the GND pin by using a dedicated track.
9. Connect the one pin of the R1 to the load for Kelvin sensing.
10. Connect one pin of the C1 (option) to the VOUT pin

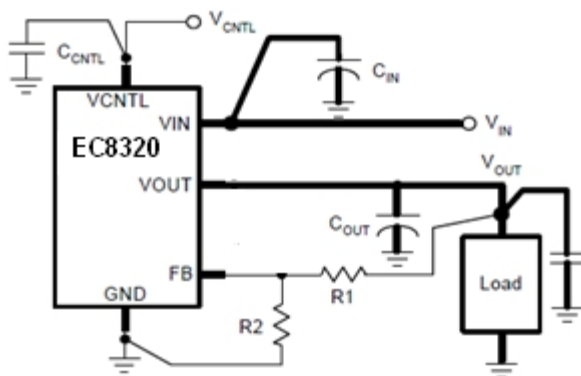


Figure A.

Thermal Consideration

Refer to the figure B, the SOP-8(EP) is a cost-effective package featuring a small size like a standard SOP-8 and a bottom exposed pad to minimize the thermal resistance of the package, being applicable to high current applications. The exposed pad must be soldered to the top-layer ground plane. It is recommended to connect the top-layer ground pad to the internal ground plan by using vias. The copper of the ground plane on the top-layer conducts heat into the PCB and ambient air. Please enlarge the area of the top-layer pad and the ground plane to reduce the case-to-ambient resistance (θ_{CA}).

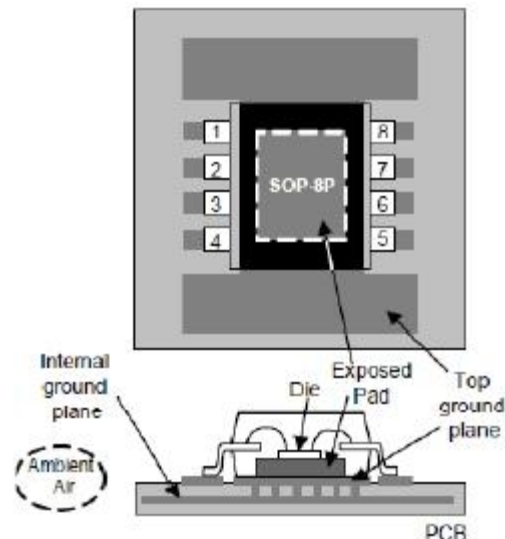
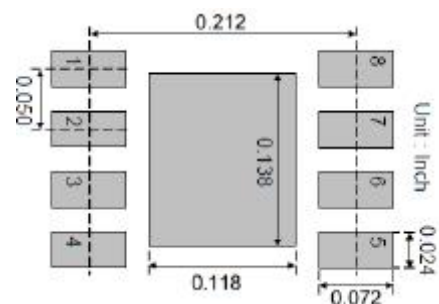
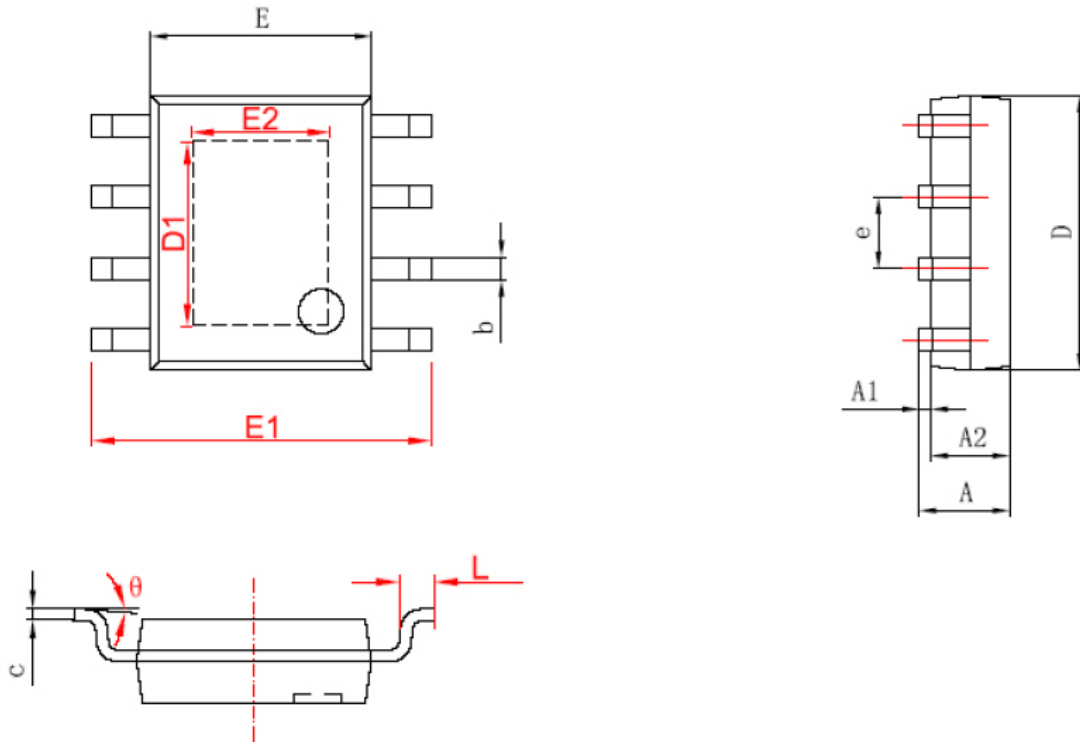


Figure B.



Package Information

SOP-8(Exposed PAD) Package Outline Dimensions



	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
theta	0°		8°	