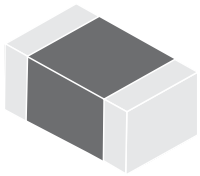
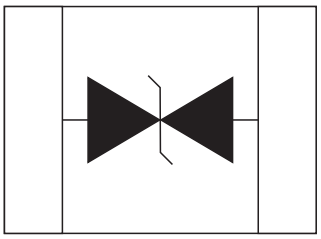
Electro-Static Discharge for Aotomobile
ALSD05BT
Low Capacitance ESD Protection

0402



Pin Configuration



Features

- ESD Protection:Level 4
- Working voltage : 5V
- Low clamping voltage
- 100 Watts peak pulse power per line(tp=8/20μs)
- Ultra low capacitance
- Protection one line I/O port
- AEC-Q101

IEC Compatibility

- EN61000 -4
- IEC61000-4-2(ESD):Level 4,Contact:±30kv,Air:±30kv
- IEC61000-4-4(EFT):40A -5/50ns
- IEC61000-4-5(Surge):4A -8/20μs

Applications

- Lan equipment
- Video
- DVI
- High Speed Data Line
- Ethernet
- USB 2.0 Power and Data line Protection

Mechanical Characteristics

- JEDEC 0402 Package
- Molding Compound Flammability Rating : UL 94V-O
- Quantity Per Reel : 10,000pcs
- Reel Size : 7 inch
- Lead Finish : Lead Free

Maximum Ratings(T_A=25℃ unless otherwise specified)

Parameter	Symbol	Value	Units
Peak Pulse Power(tp=8/20μs)	P_{PP}	100	Watts
Operating Temperature Range	T_J	-55~150	℃
Storage Temperature Range	T_{STG}	-55~150	℃

Electrical Characteristics(T_A=25℃ unless otherwise specified)

ALSD05BT(Marking:None)

Parameter	Symbol	Conditions	Min.	Max.	Units
Reverse Stand-off Voltage	V_{RWM}	Pin2 to 1 / Pin1 to 2		5	V
Reverse Breakdown Voltage	V_{BR}	Iz=1mA,Pin2 to 1 / Pin1 to 2	5.6	9.4	V
Reverse Leakage Current	I_R	@V_{RWM}		90	μA
Forward Voltage	V_F	I_F=15mA		1.15	V
Clamping Voltage	V_C	I_{PP}=1A,tp=8/20μs		12	V
Peak Pulse Current	I_{PP}	tp=8/20μs		4	A
Junction Capacitance	$C_{I/O}$	0Vdc,f=1MHz Between I/O Pins and GND		6	pF

Ratings and Characteristic Curves

Fig.1 Power Derating Curve

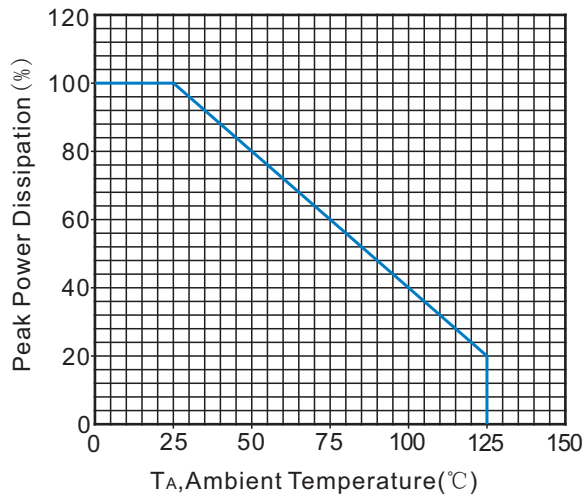
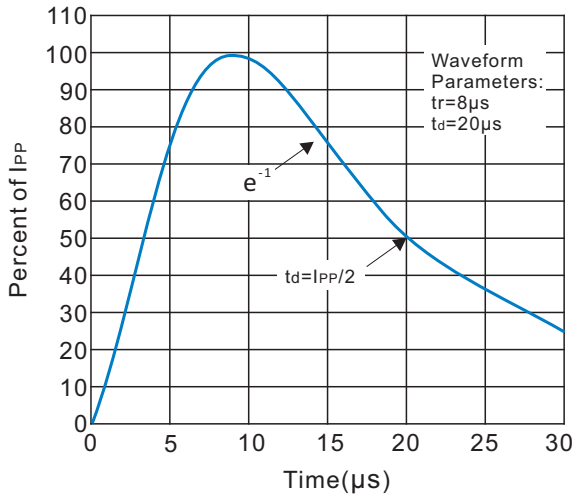
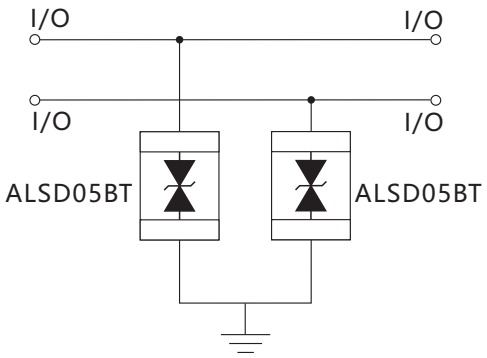


Fig.2 Pulse Waveform



Application Information

I/O Protection

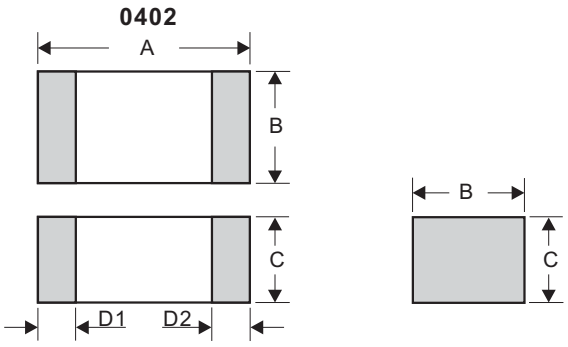


PCB Layout Recommendations

The location and circuit board layout is critical to maximize the effectiveness of the I/O protection circuit. The following guidelines are recommended:

- Locate the protection devices as close as possible to the I/O connector. This allows the protection devices to absorb the energy of the transient voltage before it can be coupled into the adjacent traces on the PCB.
- Minimize the loop area for the high.speed data lines, power and ground lines to reduce the radiated emissions.
- Avoid running protection conductors in parallel with unprotected conductors
- Use ground planes wherever possible to reduce the parasitic capacitance and inductance of the PCB that degrades the effectiveness of a filter device.
- Using shared transient return paths to a common ground point.

Dimensions(0402)



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	0.90	1.10	0.035	0.043
B	0.50	0.70	0.020	0.027
C		0.60		0.023
D1/D2	0.10	0.40	0.004	0.016

Recommended Mounting Pad Layout