

**SYNCHRONOUS MOSFET CONTROLLER IN SO-8**
**Description**

The ZXGD3109N8 is intended to drive a MOSFET configured as an ideal diode replacement. The device is comprised of a high-voltage detector stage and gate driver. The detector monitors the voltage between the drain and the source of the MOSFET, and if this voltage is less than the turn-on threshold voltage of the controller, a positive voltage is applied to the MOSFET's Gate Pin. As the load current decays to zero, and the voltage between the drain and source of the MOSFET increases beyond the turn-off threshold value, the MOSFET is rapidly turned off.

Intelligent features of this IC are the Minimum Off-Time ( $T_{OFF}$ ) and Minimum On-Time ( $T_{ON}$ ). These features blanket the noise generated during the turn-on and turn-off instances of the power FET. Also Light Load Detection (LLD) for improved efficiency at light and no load, where synchronous rectification is no more beneficial. Other features include, Undervoltage Lockout (UVLO) and low turn-off threshold voltage for improved efficiency.

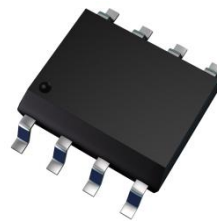
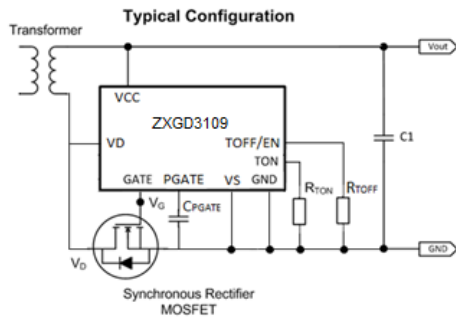
**Applications**

Flyback Converters in:

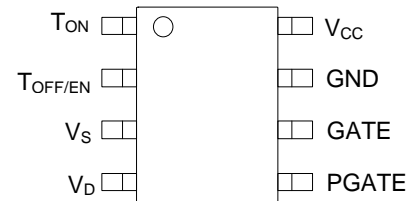
- Power Adaptors
- Auxiliary Power Supplies
- PoE Power Devices

Resonant Converters in:

- High Power Adaptors
- 85+/90+ Compliant ATX and Server Power Supplies



SO-8  
Top view



Top View  
Pin-Out

**Features**

- Frequency of Operation Up to 500kHz
- Suitable for Discontinuous Conduction Mode (DCM) and Critical Conduction Mode (CrCM)
- Minimum On-Time and Off-Time to Reduce Turn-On/Off Oscillations
- Intelligent Light Load Detection and Sleep Mode
- Turn-Off Propagation Delay Time of 30ns Typically
- Drain Voltage Rating of 200V
- Recommended Operating Voltage from 4.5V up to 12V
- Source and Sink Current of 2A and 4A Respectively
- Low Component Count
- **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony free. "Green" Device (Note 3)**

**Mechanical Data**

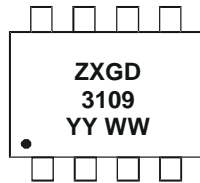
- Case: SO-8
- Case Material: Molded Plastic. "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (E3)
- Weight: 0.074 grams (Approximate)

**Ordering Information** (Note 4)

| Product      | Marking  | Reel Size (inches) | Tape Width (mm) | Quantity per Reel |
|--------------|----------|--------------------|-----------------|-------------------|
| ZXGD3109N8TC | ZXGD3109 | 13                 | 12              | 2,500             |

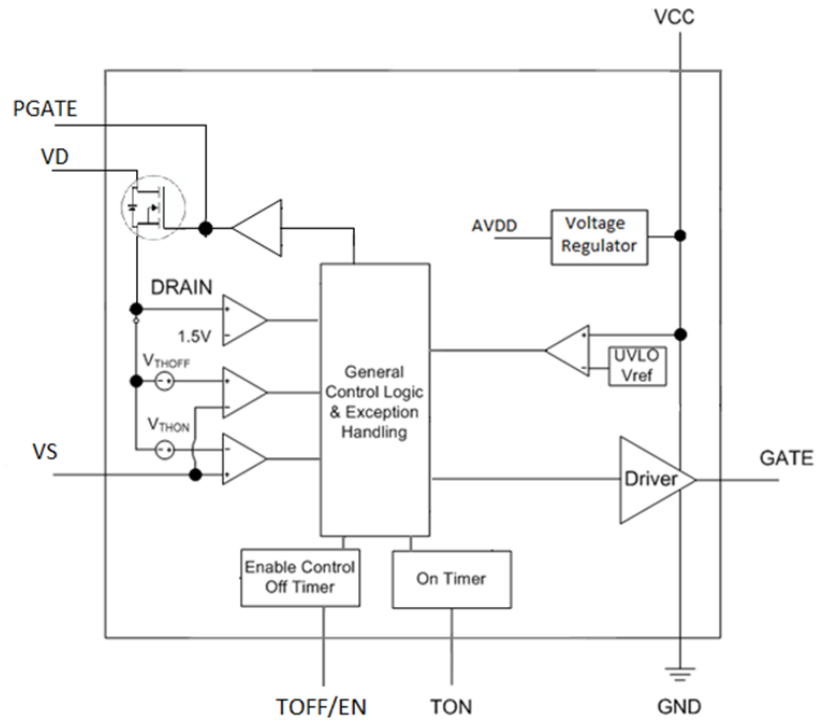
- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

**Marking Information**



ZXGD = Product Type Marking Code, Line 1  
 3109 = Product Type Marking Code, Line 2  
 YY = Year (ex: 15 = 2015)  
 WW = Week (01 - 53)

**Functional Block Diagram**



## Pin Descriptions

| Pin Number | Pin Name     | Function  |
|------------|--------------|---|
| 1          | $T_{ON}$     | <b>Minimum On-Time</b><br>Minimum on-time setting pin. Connect this pin to Ground via $R_{TON}$ resistor.   |
| 2          | $T_{OFF/EN}$ | <b>Minimum Off-Time/Enable Pin</b><br>This pin combines the functions of setting the programmable minimum off-time as well as acting as the Enable Pin. The device enters Undervoltage Lockout (UVLO) mode when $V_{CC}$ falls below the UVLO threshold. At this point, the $T_{OFF/EN}$ Pin is internally shorted to Ground through a resistor. The internal current source (used for setting $T_{OFF}$ ) is powered down. Once the UVLO threshold is exceeded, the internal resistor is removed and the current source is activated. If the voltage applied to the $T_{OFF/EN}$ Pin exceeds the $V_{EN-ON}$ threshold then the device is in Active Mode. If the voltage drops below the $V_{EN-OFF}$ threshold then the device is in Sleep Mode.  |
| 3          | $V_S$        | <b>Source Voltage</b><br>Connect this pin to the source of the synchronous MOSFET   |
| 4          | $V_D$        | <b>Drain Voltage</b><br>The pin needs to be connected as closely as possible to the transformer used in the application to minimize the effects of parasitic inductance on the performance of the device. The device requires that $V_D$ has a voltage greater than 1.5V, and that the $T_{OFF}$ timer has expired before the MOSFET is able to be activated. Once these conditions are met, and the voltage sensed on the $V_D$ Pin is 150mV lower than the $V_S$ Pin, the Gate output to the synchronous MOSFET will go high and the $T_{ON}$ (minimum on-time) period is started. The MOSFET will remain on for at least the length of the minimum on-time. After the $T_{ON}$ period, the MOSFET will remain on until the $V_D$ to $V_S$ voltage has reached the $V_{THOFF}$ threshold, at which point the Gate output will go low. If the $V_{THOFF}$ threshold is reached before the $T_{ON}$ period has expired, the device will enter the Light Load Mode. Under this mode, the MOSFET will not be turned on the next switching cycle. The device will come out of light load once the on-time of the synchronous MOSFET exceeds the set minimum on-time. |
| 5          | PGATE        | <b>Protection MOSFET Gate</b><br>A 100nF capacitor should be connected between this pin and GND.  |
| 6          | GATE         | <b>Gate</b><br>Connect GATE to the gate of the synchronous MOSFET through a small-series resistor using short PC board tracks to achieve optimal switching performance. The Gate output can source >2A peak source current while turning on the sync MOSFET, and can sink >4A peak current while turning on the sync MOSFET.  |
| 7          | GND          | <b>Ground</b><br>This is the reference potential for all internal comparators and thresholds. A 10 $\mu$ F decoupling capacitor is required to be placed as close as possible between $V_{CC}$ and GND Pins.  |
| 8          | $V_{CC}$     | <b>Power Supply Pin</b><br>$V_{CC}$ supplies all the internal circuitry of the device. A DC supply is required to be connected to this pin. A 10 $\mu$ F or larger capacitor must be connected between this pin and GND Pin as close as possible. The device will not function until the $V_{CC}$ has risen above the UVLO threshold. The device can safely be turned off by bringing $V_{CC}$ below the UVLO threshold (minus the UVLO threshold hysteresis). If $V_{CC}$ drops below the UVLO threshold (minus UVLO threshold hysteresis), the MOSFET is turned off and the $T_{OFF/EN}$ Pin is internally connected to GND.  |

**Absolute Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

| Characteristic                                  | Symbol              | Value      | Unit |
|---|---------------------|------------|------|
| Supply Voltage, Relative to GND                 | V <sub>CC</sub>     | -0.3 to 15 | V    |
| Drain Pin Voltage                               | V <sub>D</sub>      | -1 to +200 | V    |
| Gate Output Voltage                             | V <sub>G</sub>      | 12         | V    |
| Minimum On-Time (T <sub>OFF</sub> ) Pin Voltage | V <sub>TOFF</sub>   | -0.3 to 6  | V    |
| Minimum Off-Time (T <sub>ON</sub> ) Pin Voltage | V <sub>TON</sub>    | -0.3 to 6  | V    |
| Gate Driver Peak Source Current                 | I <sub>SOURCE</sub> | 5          | A    |
| Gate Driver Peak Sink Current                   | I <sub>SINK</sub>   | 5          | A    |
| Input Voltage Range V <sub>S</sub>              | V <sub>S</sub>      | -1 to 1    | V    |

**Thermal Characteristics**

| Characteristic                              | Symbol           | Value       | Unit        |
|---|------------------|-------------|-------------|
| Power Dissipation<br>Linear Derating Factor | P <sub>D</sub>   | 490         | mW<br>mW/°C |
|   |                  | 3.92        |             |
|   |                  | 655         |             |
|   |                  | 5.24        |             |
|   |                  | 720         |             |
| Thermal Resistance, Junction to Ambient     | R <sub>θJA</sub> | 5.76        | °C/W        |
|   |                  | 785         |             |
|   |                  | 6.28        |             |
|   |                  | 255         |             |
| Thermal Resistance, Junction to Lead        | R <sub>θJL</sub> | 191         | °C/W        |
|   |                  | 173         |             |
|   |                  | 159         |             |
| Thermal Resistance, Junction to Case        | R <sub>θJC</sub> | 55          | °C/W        |
| Maximum Junction Temperature                | T <sub>J</sub>   | +150        | °C          |
| Storage Temperature Range                   | T <sub>STG</sub> | -65 to +150 |             |

**ESD Ratings** (Note 11)

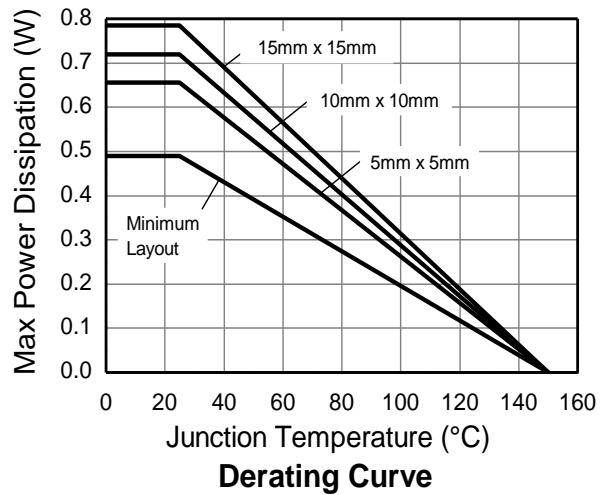
| Characteristic                             | Symbol  | Value | Unit | JEDEC Class |
|--|---------|-------|------|-------------|
| Electrostatic Discharge - Human Body Model | ESD HBM | 2,000 | V    | 1C          |
| Electrostatic Discharge - Machine Model    | ESD MM  | 500   | V    | C           |

- Notes:
- For a device surface mounted on minimum recommended pad layout FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
  - Same as Note (5), except Pin 8 (V<sub>CC</sub>) and Pin 7 (GND) are both connected to separate 5mm x 5mm 1oz copper heatsinks.
  - Same as Note (6), except both heatsinks are 10mm x 10mm.
  - Same as Note (6), except both heatsinks are 15mm x 15mm.
  - Thermal resistance from junction to solder-point at the end of each lead on Pin 8 (V<sub>CC</sub>) and Pin 7 (GND).
  - Thermal resistance from junction to top of the case.
  - Refer to JEDEC specification JESD22-A114 and JESD22-A115.

**Recommended Operating Conditions**

| Symbol            | Parameter                            | Min  | Max  | Unit |
|-------------------|--------------------------------------|------|------|------|
| V <sub>CC</sub>   | Supply Voltage Range                 | 4.5  | 12   | V    |
| V <sub>DS</sub>   | Voltage Cross Drain and Source       | -1   | 200  |      |
| F <sub>SW</sub>   | Switching Frequency                  | 20   | 600  | kHz  |
| T <sub>J</sub>    | Operating Junction Temperature Range | -40  | +125 | °C   |
| R <sub>TOFF</sub> | T <sub>OFF</sub> Resistor Value      | 85   | 200  | kΩ   |
| R <sub>TON</sub>  | T <sub>ON</sub> Resistor Value       | 8.25 | 100  | kΩ   |
| C <sub>VCC</sub>  | V <sub>CC</sub> Bypass Capacitor     | 10   | —    | μF   |

**Thermal Derating Curve**



**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

| Symbol                             | Parameter   | Conditions   | Min   | Typ  | Max  | Unit |
|------------------------------------|---|--|-------|------|------|------|
| ICC <sub>START</sub>               | Supply Current (Undervoltage)                             | V <sub>CC</sub> = 2.6V   | —     | 160  | 220  | μA   |
| ICC <sub>STANDBY</sub>             | Supply Current (Disabled)                                 | V <sub>CC</sub> = 5.5V, R <sub>EN/OFF</sub> = 0Ω   | —     | 380  | 500  |      |
|                                    |   | V <sub>CC</sub> = 12V, R <sub>EN/OFF</sub> = 0Ω  | —     | 450  | 600  |      |
| ICC <sub>CON</sub>                 | Supply Current (Enabled)                                  | V <sub>CC</sub> = 5.5V, F <sub>SW</sub> = 100KHz<br>C <sub>GATE</sub> = 0pF              | —     | 1.5  | 1.8  | mA   |
|                                    |   | V <sub>CC</sub> = 12V, F <sub>SW</sub> = 100KHz<br>C <sub>GATE</sub> = 0pF               | —     | 1.8  | 2.3  |      |
|                                    |   | V <sub>CC</sub> = 5.5V, F <sub>SW</sub> = 100KHz<br>C <sub>GATE</sub> = 3,300pF          | —     | 3.2  | 4    |      |
|                                    |   | V <sub>CC</sub> = 12V, F <sub>SW</sub> = 100KHz<br>C <sub>GATE</sub> = 3,300pF           | —     | 5    | 7    |      |
| V <sub>EN-ON</sub>                 | T <sub>OFF/EN</sub> Turn-on Threshold, Rising             | T <sub>OFF/EN</sub> Driven, V <sub>TON</sub> > 0.6V                                      | 1.31  | 1.4  | 1.49 | V    |
| V <sub>EN-OFF</sub>                | T <sub>OFF/EN</sub> Turn-off Threshold, Falling           | T <sub>OFF/EN</sub> Driven,<br>V <sub>TON</sub> > 0.2V                                   | 0.55  | 0.6  | 0.65 |      |
| I <sub>EN-START</sub>              | T <sub>OFF/EN</sub> Input Current (Disabled)              | R <sub>TOFF</sub> = 50kΩ   | -23   | -20  | -17  | μA   |
| I <sub>EN-ON</sub>                 | T <sub>OFF/EN</sub> Input Current (Enabled)               | R <sub>TOFF</sub> = 100kΩ  | -11.5 | -10  | -8.5 |      |
| <b>Undervoltage Lockout (UVLO)</b> |   |  |       |      |      |      |
| UVLO <sub>TH</sub>                 | V <sub>CC</sub> Undervoltage Lockout Threshold Rising     | —  | 2.8   | 3.0  | 3.20 | V    |
| UVLO <sub>HYS</sub>                | V <sub>CC</sub> Undervoltage Lockout Threshold Hysteresis | —  | —     | 200  | —    | mV   |
| <b>MOSFET Voltage Sensing</b>      |   |  |       |      |      |      |
| V <sub>THARM</sub>                 | Gate Re-Arming Threshold                                  | V <sub>D</sub> to GND, Rising  | -1.3  | 1.5  | -1.7 | V    |
| V <sub>THON</sub>                  | Gate Turn-On Threshold                                    | (V <sub>D</sub> -V <sub>S</sub> ) Falling, V <sub>S</sub> = 0V                           | -220  | -150 | -80  | mV   |
| V <sub>THOFFLV</sub>               | Gate Turn-Off Threshold                                   | (V <sub>D</sub> -V <sub>S</sub> ) Rising, V <sub>S</sub> = 0V,<br>V <sub>CC</sub> < 4.3V | -30   | -20  | -10  | mV   |
| V <sub>THOFFHV</sub>               | Gate Turn-Off Threshold                                   | (V <sub>D</sub> -V <sub>S</sub> ) Rising, V <sub>S</sub> = 0V,<br>V <sub>CC</sub> > 4.3V | -10   | -4   | -1   | mV   |
| T <sub>D(ON)</sub>                 | Gate Turn-On Propagation Delay                            | From V <sub>THON</sub> to Gate > 1V  | —     | 30   | 52   | ns   |
| T <sub>D(OFF)</sub>                | Gate Turn-Off Propagation Delay                           | From V <sub>THOFF</sub> to Gate < 4V   | —     | 30   | 62   | ns   |
| <b>Minimum On-Time</b>             |   |  |       |      |      |      |
| T <sub>ON-LR</sub>                 | Minimum On-Time Low Resistance                            | R <sub>TON</sub> = 8.25kΩ  | 0.26  | 0.34 | 0.42 | μs   |
| T <sub>ON-HR</sub>                 | Minimum On-Time High Resistance                           | R <sub>TON</sub> = 100kΩ   | 2.2   | 3    | 3.8  | μs   |

**Electrical Characteristics** (Continued) (@T<sub>A</sub> = +25°C, unless otherwise specified.)

| <b>Minimum Off-Time</b>   |   |   |     |      |     |    |
|---------------------------|---|---|-----|------|-----|----|
| T <sub>OFF-LR</sub>       | Minimum Off-Time Low Resistance                       | R <sub>TOFF</sub> = 100kΩ                                     | 1.2 | 3    | 5   | μs |
| T <sub>OFF-HR</sub>       | Minimum Off-Time High Resistance                      | R <sub>TOFF</sub> = 200kΩ                                     | 15  | 21   | 25  | μs |
| T <sub>OFF-LV</sub>       | Minimum Off-Time Low Voltage                          | V <sub>EN/TOFF</sub> = 1V                                     | —   | 3    | —   | μs |
| T <sub>OFF-HV</sub>       | Minimum Off-Time High Voltage                         | V <sub>EN/TOFF</sub> = 2V                                     | —   | 21   | —   | μs |
| T <sub>OFF-OV</sub>       | Minimum Off-Time Over Voltage                         | 2V < V <sub>EN/TOFF</sub> < V <sub>AVDD</sub>                 | —   | 21   | —   | μs |
| <b>Gate Driver</b>        |   |   |     |      |     |    |
| R <sub>GUP</sub>          | Gate Pull-Up Resistance Enabled                       | I <sub>GATE</sub> = -100mA                                    | —   | 2.3  | —   | Ω  |
| R <sub>GDN</sub>          | Gate Pull-Down Resistance Enabled                     | I <sub>GATE</sub> = 100mA                                     | —   | 1.1  | —   |    |
| I <sub>SOURCE</sub>       | Peak Gate Source Current                              | C <sub>GATE</sub> = 22nF                                      | —   | 3    | —   | A  |
| I <sub>SINK</sub>         | Peak Gate Sink Current                                | C <sub>GATE</sub> = 22nF                                      | —   | 4    | —   |    |
| V <sub>OHG</sub>          | Gate Output High Voltage                              | V <sub>CC</sub> = 5V  | 4.7 | —    | —   | V  |
|                           |   | V <sub>CC</sub> = 12V   | 9   | —    | —   |    |
| V <sub>OLG</sub>          | Gate Output Low Voltage                               | V <sub>CC</sub> = 5V  | —   | —    | 0.3 |    |
| T <sub>FGATE</sub>        | Gate Fall Time  | 4V to 1V, C <sub>GATE</sub> = 3,300pF, V <sub>CC</sub> = 5V   | —   | 14   | 42  | ns |
|                           |   | 9V to 1V, C <sub>GATE</sub> = 3,300pF, V <sub>CC</sub> = 12V  | —   | 20   | 42  |    |
| T <sub>RGATE</sub>        | Gate Rise Time  | 1V to 4V, C <sub>GATE</sub> = 3,300pF, V <sub>CC</sub> = 5V   | —   | 16   | 42  |    |
|                           |   | 1V to 10V, C <sub>GATE</sub> = 3,300pF, V <sub>CC</sub> = 12V | —   | 20   | 42  |    |
| T <sub>DIS</sub>          | Disable Delay (Note 8)                                | EN Falling to Gate Falling                                    | —   | 160  | —   |    |
| <b>Exception Handling</b> |   |   |     |      |     |    |
| T <sub>OVER</sub>         | Overtemperature                                       | —   | —   | +150 | —   | °C |
| T <sub>RECOVER</sub>      | Temperature to Recover from Overtemperature Exception | —   | —   | +125 | —   | °C |





**Typical Performance Characteristics**

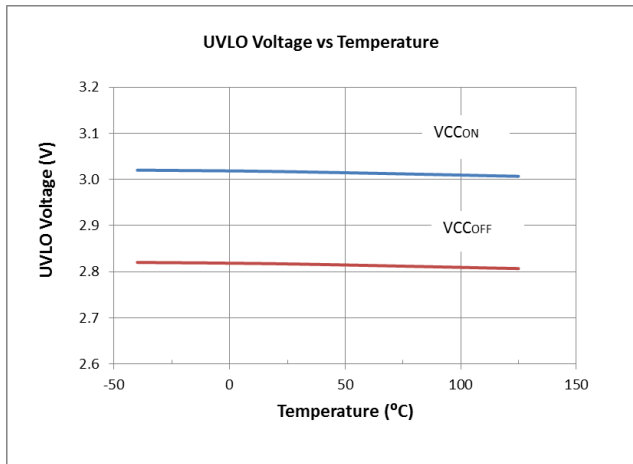


Figure 1

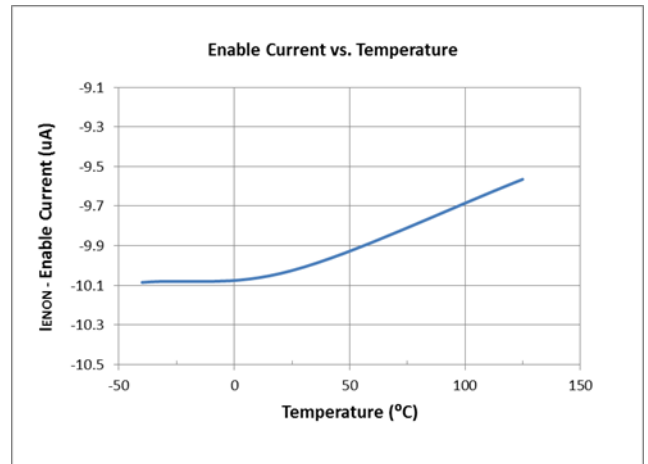


Figure 2

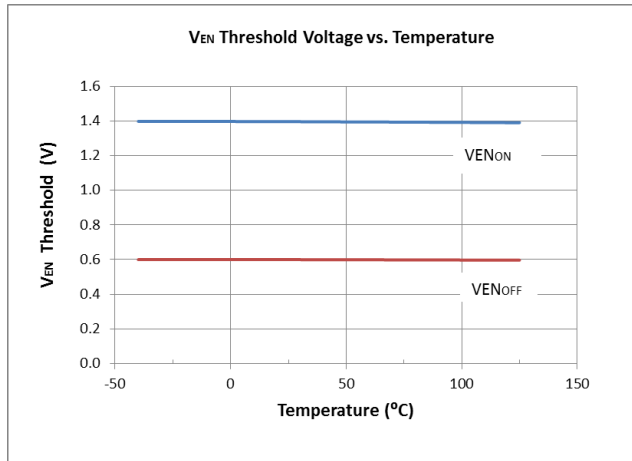


Figure 3

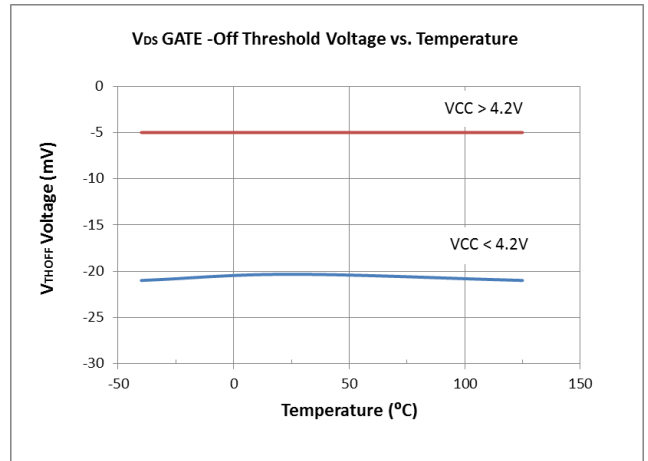


Figure 4

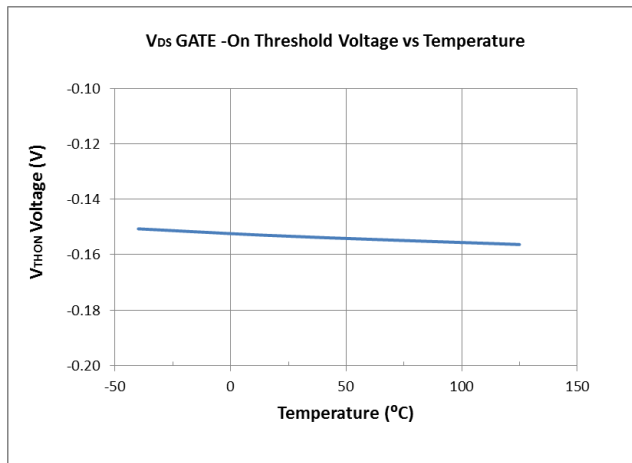


Figure 5

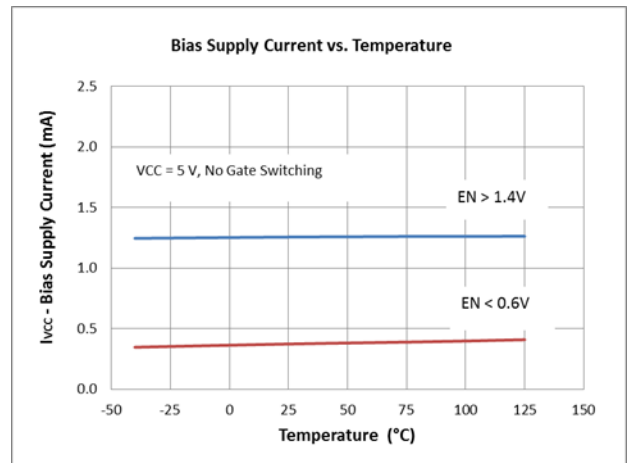
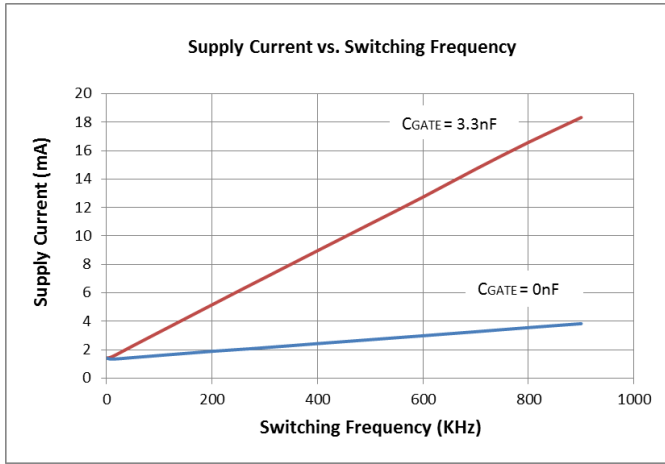
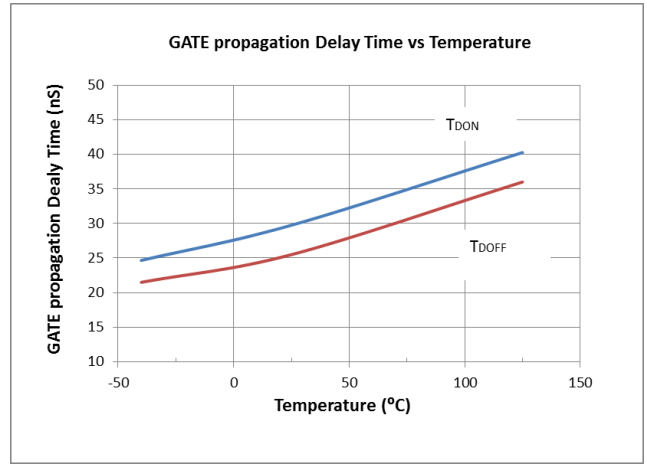


Figure 6

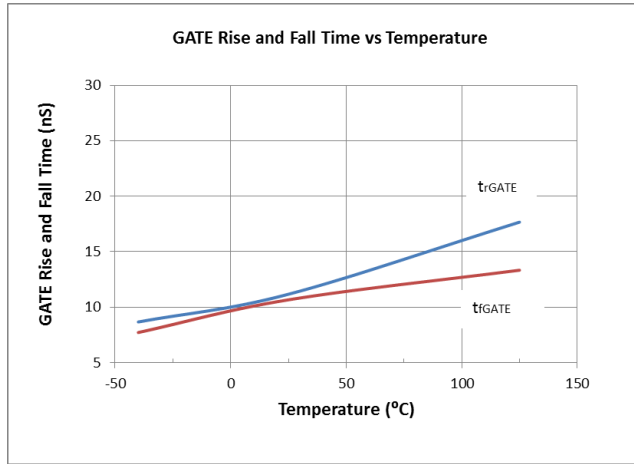
**Typical Performance Characteristics** (Continued)



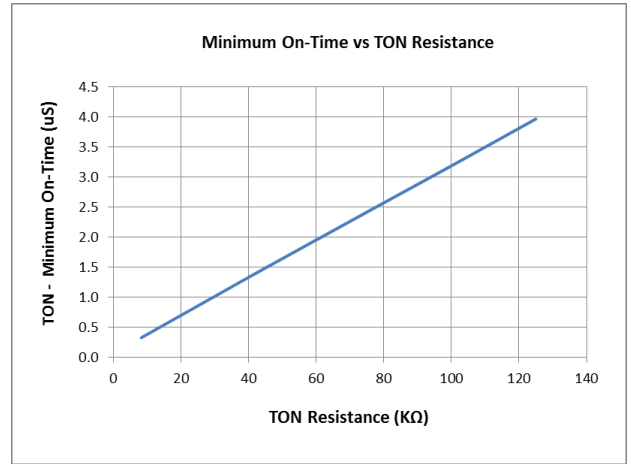
**Figure 7**



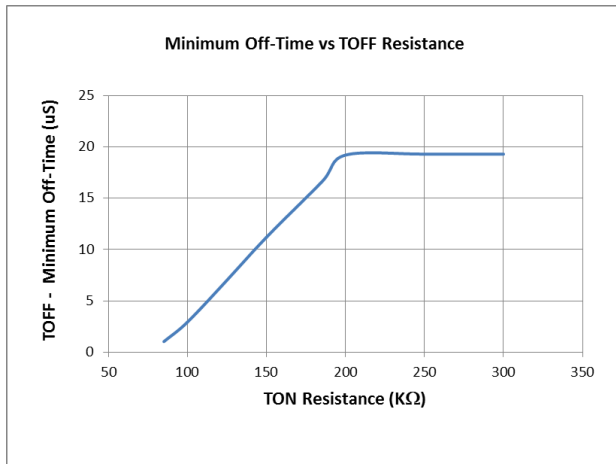
**Figure 8**



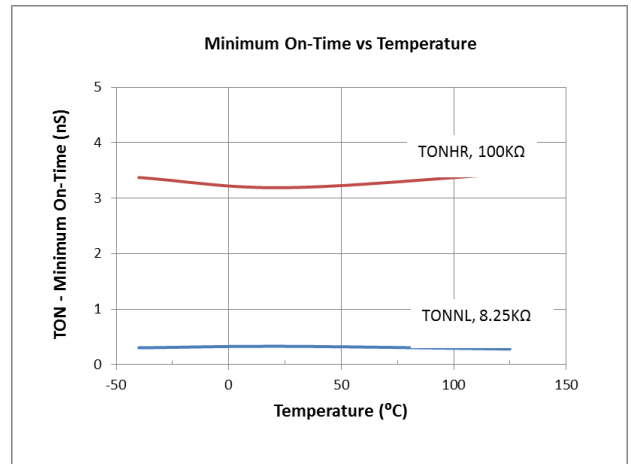
**Figure 9**



**Figure 10**

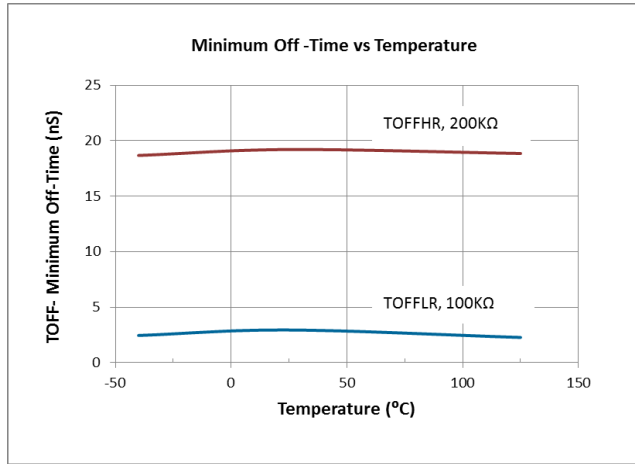


**Figure 11**

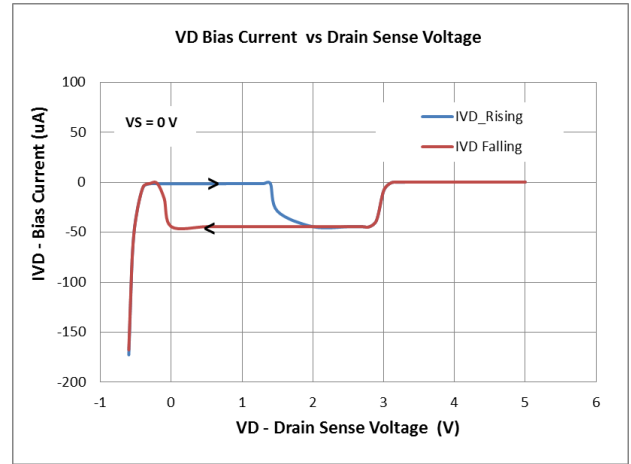


**Figure 12**

**Typical Performance Characteristics (Cont.)**



**Figure 13**

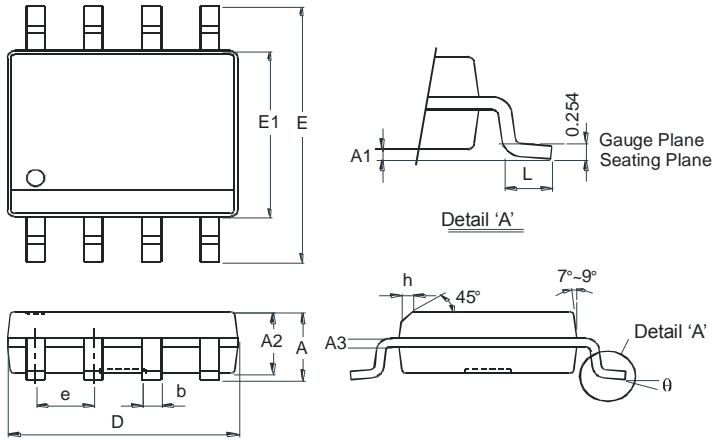


**Figure 14**

**Package Outline Dimensions**

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.

**SO-8**

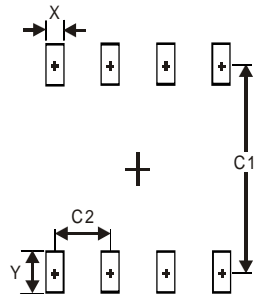


| SO-8                        |          |      |
|-----------------------------|----------|------|
| Dim                         | Min      | Max  |
| A                           | -        | 1.75 |
| A1                          | 0.10     | 0.20 |
| A2                          | 1.30     | 1.50 |
| A3                          | 0.15     | 0.25 |
| b                           | 0.3      | 0.5  |
| D                           | 4.85     | 4.95 |
| E                           | 5.90     | 6.10 |
| E1                          | 3.85     | 3.95 |
| e                           | 1.27 Typ |      |
| h                           | -        | 0.35 |
| L                           | 0.62     | 0.82 |
| θ                           | 0°       | 8°   |
| <b>All Dimensions in mm</b> |          |      |

**Suggested Pad Layout**

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

**SO-8**



| Dimensions | Value (in mm) |
|------------|---------------|
| X          | 0.60          |
| Y          | 1.55          |
| C1         | 5.4           |
| C2         | 1.27          |

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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