QPB7464

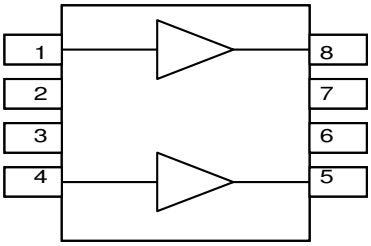
CATV 75 Ω pHEMT Dual RF Amplifier

Product Overview

The QPB7464 is a 75Ω, fully integrated, dual-die differential RF Amplifier covering medium power applications in the CATV band. It is fabricated using 6 inch GaAs pHEMT technology to optimize performance and cost.

SOIC-8 Package

Functional Block Diagram



Top View

Key Features

- 50 – 2600 MHz Bandwidth
- 75Ω Impedance
- pHEMT Device Technology
- Meets DOCSIS 3.1 Output Requirements
- +5 V Supply Voltage
- 240 mA Current Consumption
- SOIC-8 package
- +37 dBm OIP3
- 12 dB Gain

Applications

- Replacement for +5 V SOIC-8 Amplifiers
- Edge QAM Output Stage
- MDU Output
- Satellite Frequency Distribution
- V-ONU Receiver Output Stage

Ordering Information

Part No.	Description
QPB7464SQ	Sample bag with 25 pieces
QPB7464SR	7” Reel with 100 pieces
QPB7464TR13	13” Reel with 2500 pieces
QPB7464PCK401	Amplifier Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_{DD})	+10 V
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +100 °C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (V_{DD})		+5.0		V
I_{DD} (Total EVB Current)		+240		mA
Tj for>10^6 hours MTTF			+150	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

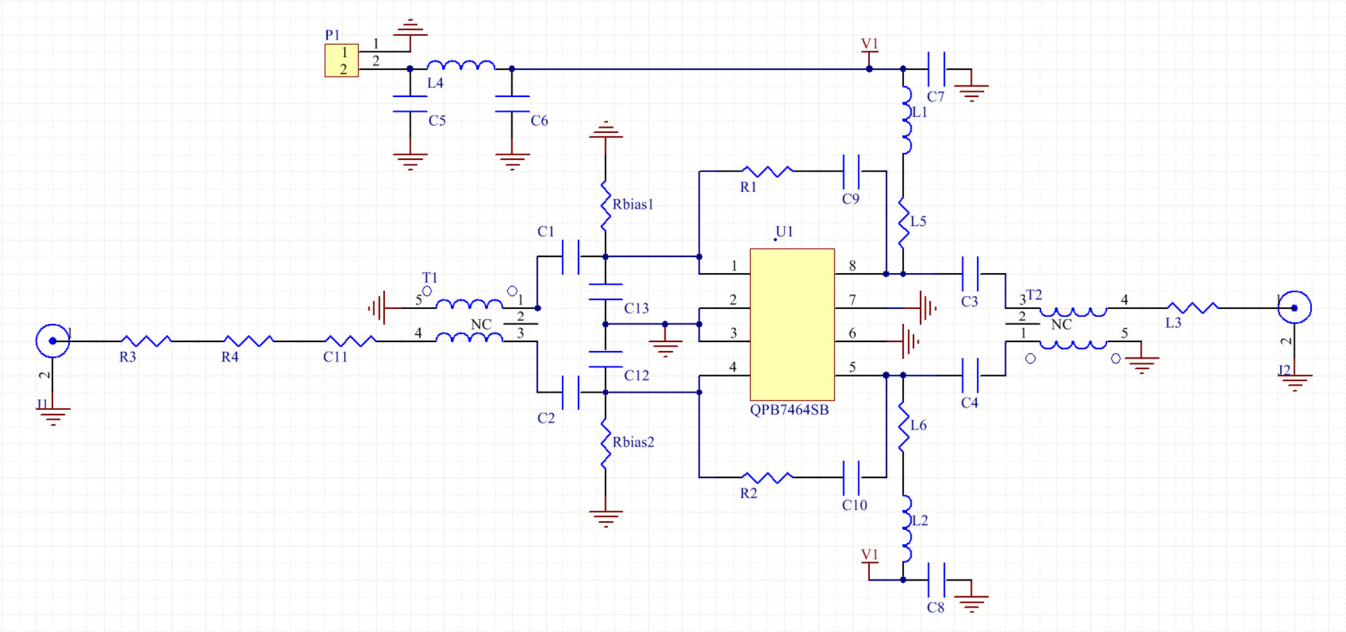
Electrical Specifications

Parameter	Conditions (1)	Min	Typ	Max	Unit
Operational Frequency Range		50		2600	MHz
Gain			11.5		dB
Gain Flatness			±0.75		dB
Noise Figure			4.5		dB
Input Return Loss			8		dB
Output Return Loss			8		dB
OIP3			37		dBm
V_{DD}			5		V
I_{DD}			240		mA
Thermal Resistance (θ_{jc})	Junction to Case		14		°C / W

Notes:

1. Test conditions unless otherwise noted: Temp. = +25 °C, V_{DD} = 5 V, 75 Ω system

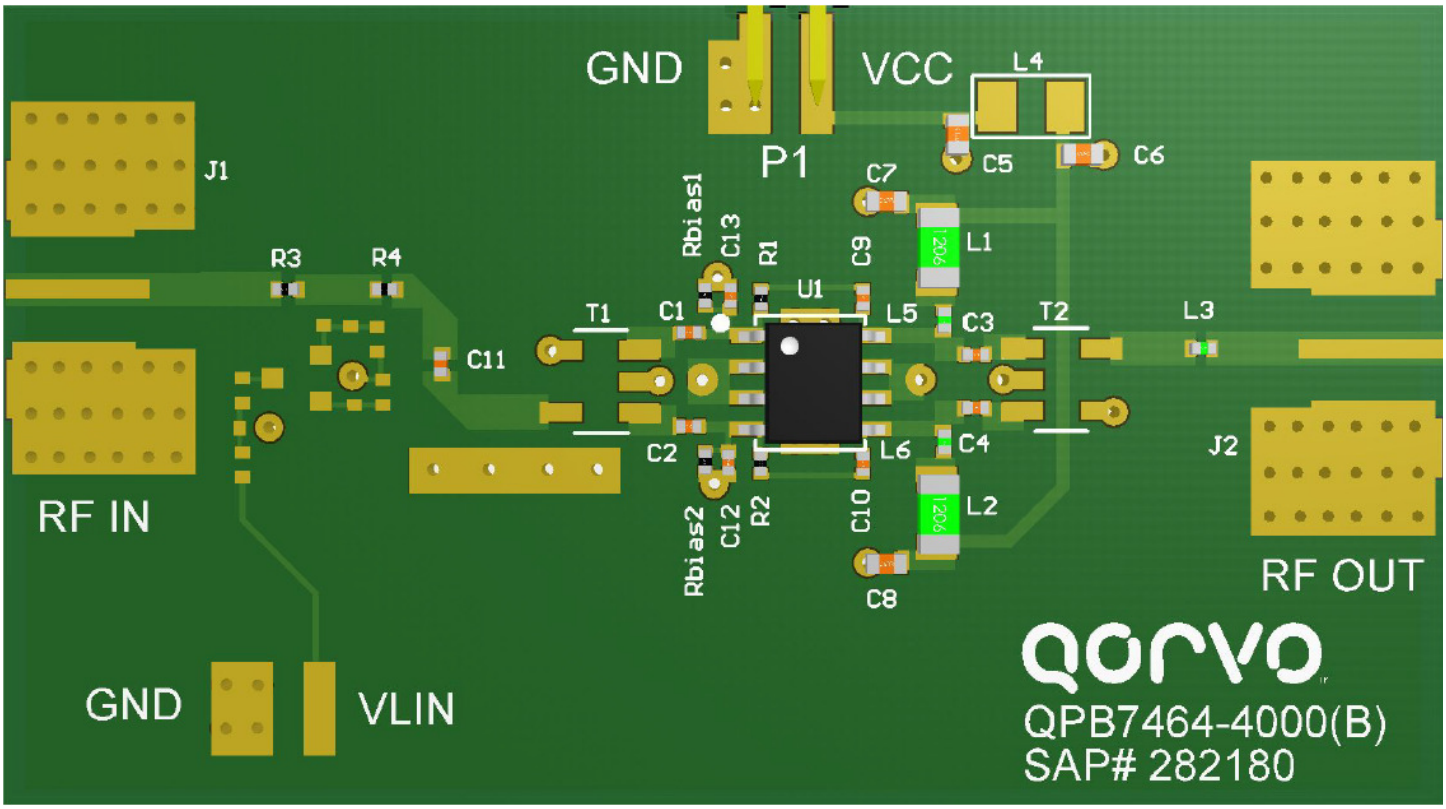
Typical Application Schematic



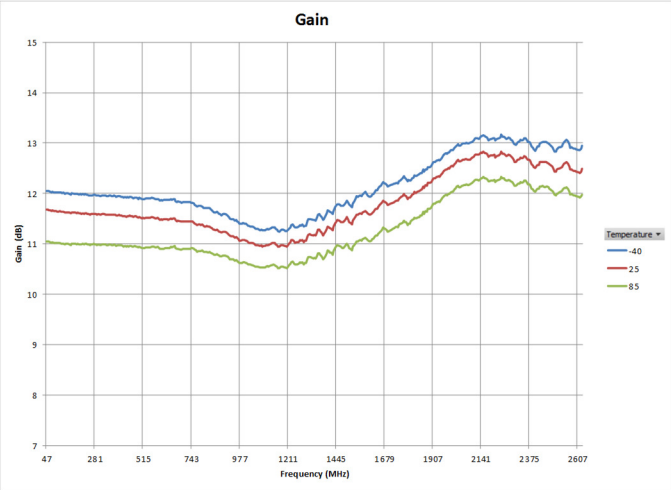
Evaluation Board Bill of Materials (BOM)

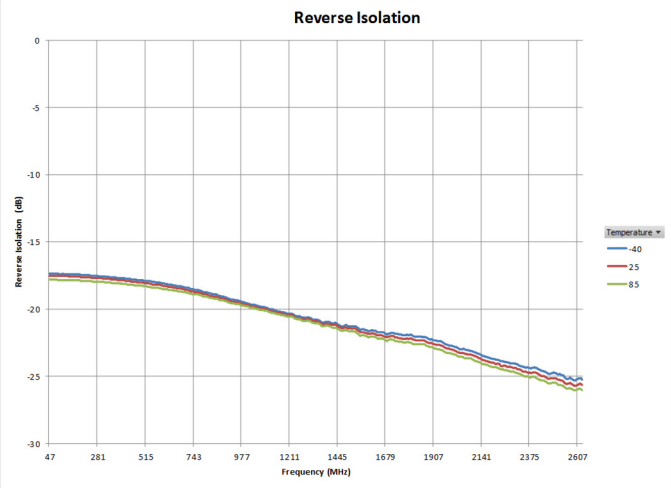
Description	Designator	Manufacturer	Part Number
QPB7464 50-2600MHz GP CATV Gain Block	U1	Qorvo, Inc.	QPB7464SB
PCB		Viasystems Technologies Corp LLC	
CAP, 1000 pF, 10%, 50 V, 0402	C3, C4	Murata Electronics-Singapore	GRM155R71H102KA01D
CAP, 0.01uF, 10%, 16 V, X7R, 0402	C1, C2, C5, C6, C7, C8, C9, C10	Panasonic	ECJ-0EB1C103K
CAP, 0.7 pF, +/-0.1pF, 50 V, C0G, 0402	C12, C13	Murata Electronics-Singapore	GJM1555C1HR70BB01D
IND, 880 nH, +/-5%, 1 MHz, 1206	L1, L2, L4	Murata	LQH31HNR88J03
RES, 330 Ω, 1%, 1/16W, 0402	R1, R2	Vishay	CRCW0402330RFKRD
RES, 0 Ω, 5%, 1/10W, 0402	C11, L3, L5, L6, R3, R4	Kamaya, Inc.	RMC1/16SJPTH
Balun, 1:1, 75 Ω	T1, T2	Mini-Circuits	TC1-1-13M-17+
HEADER PIN, 2 POS 0.1"RA, SMT	P1	Molex	022-28-8021
Connector 75 Ω, Edge Launch F	J1, J2	Lighthorse Technologies	LTI-FSF55NT-P
Not Populated Item	RBIAS1, RBIAS2		

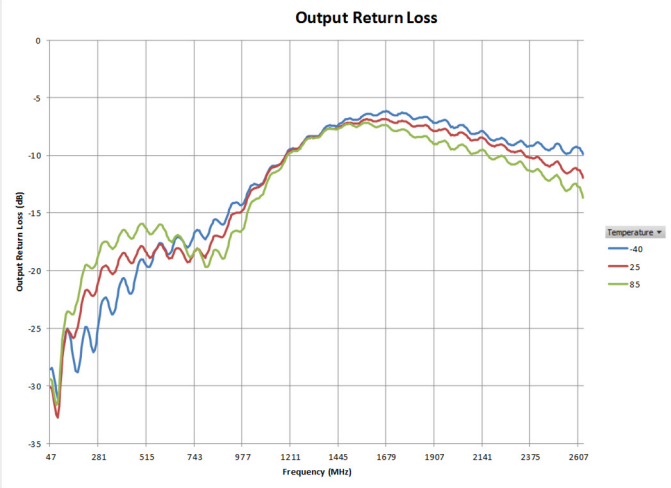
Evaluation Board Assembly Drawing

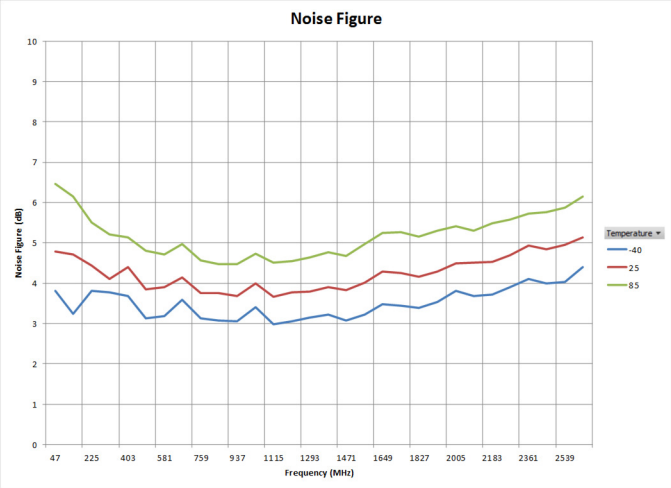


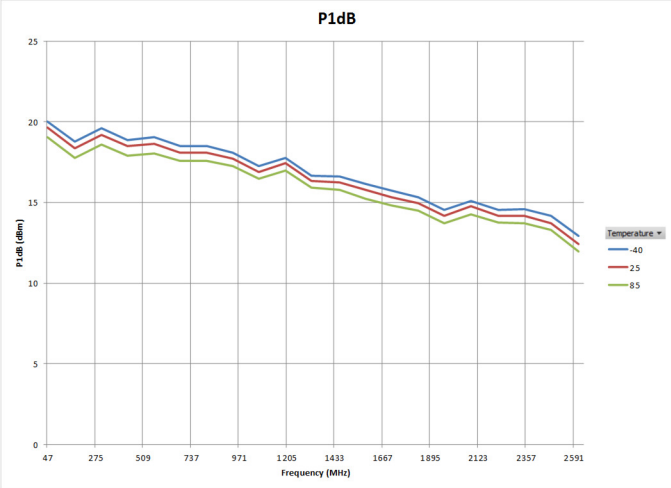
Performance Plots



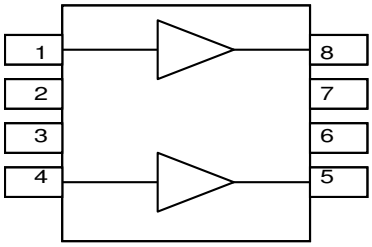






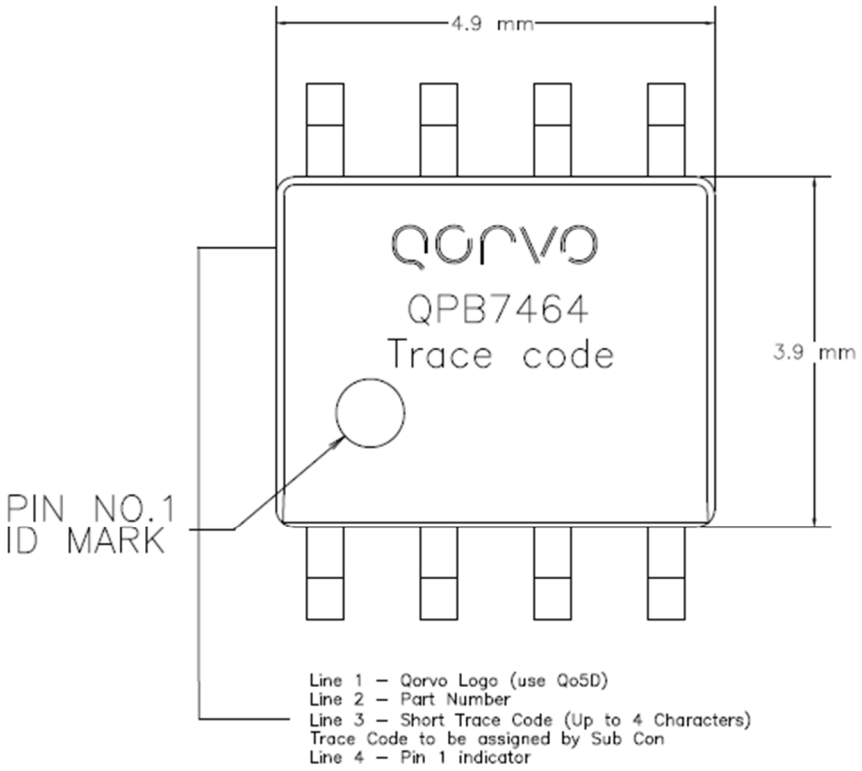


Pin Configuration and Description

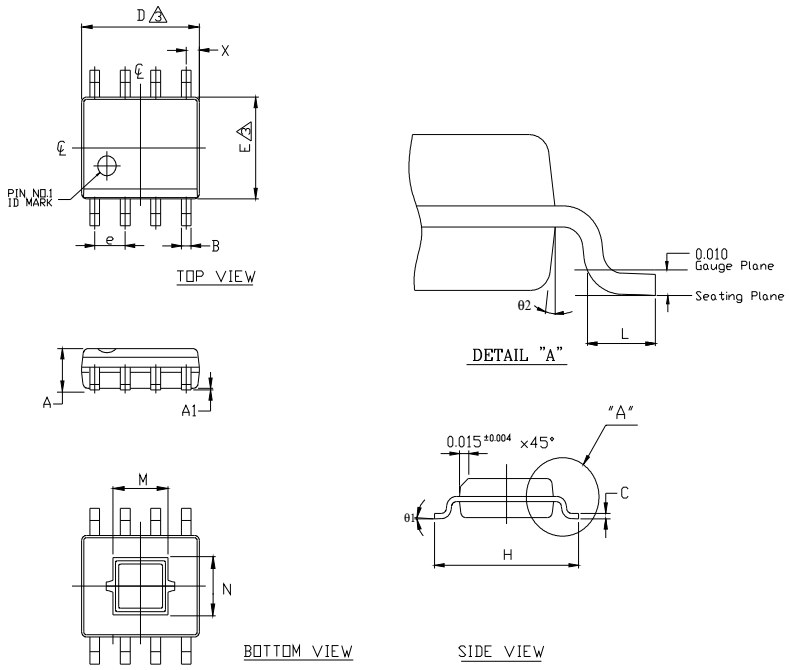


Pin Number	Label	Description
1	$RF_{IN}A$	RF Input A. DC blocking capacitor required.
2	NC	Not Connected
3	NC	Not Connected
4	$RF_{IN}B$	RF Input B. DC blocking capacitor required.
5	$RF_{OUT}B$ / V_{DD}	RF Output B. DC blocking capacitor required.
6	NC	Not Connected
7	NC	Not Connected
8	$RF_{OUT}A$ / V_{DD}	RF Output A. DC blocking capacitor required.
Backside Pad	RF/DC GND	Ground Slug

Package Marking



Package Dimensions

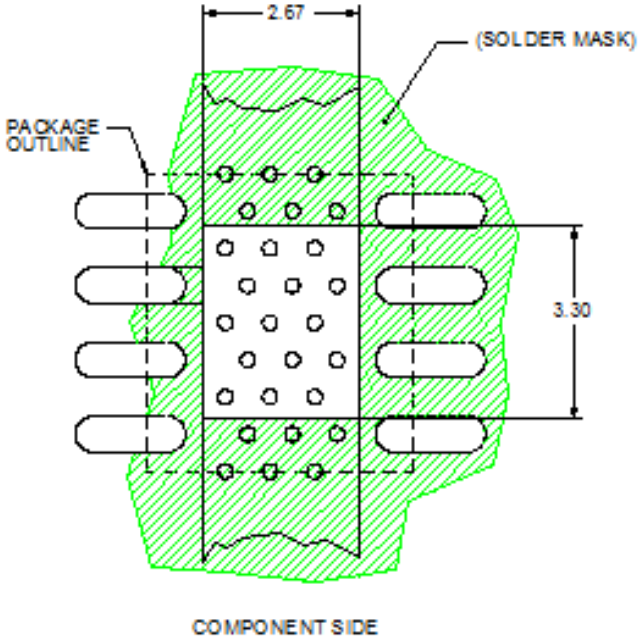


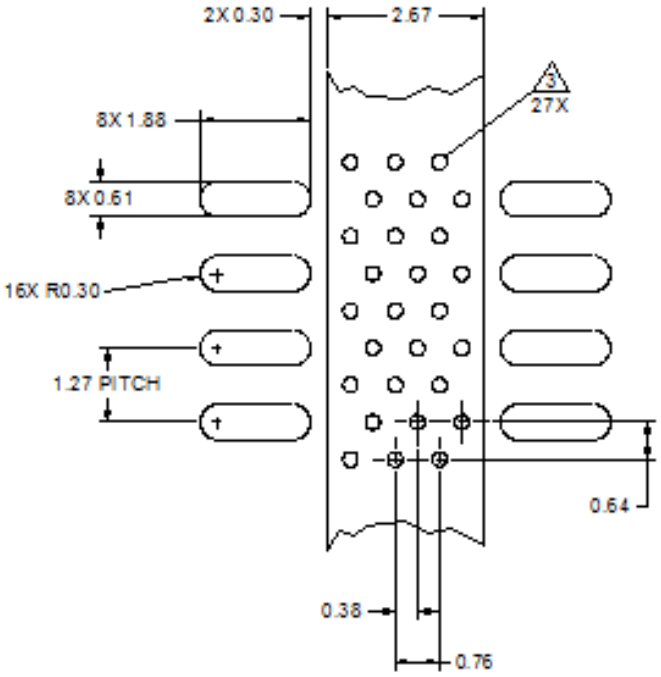
SYMBOL	8 SOIC	
	MIN	MAX
A	0.054	0.068
A1	0.001	0.004
B	0.014	0.019
D	0.189	0.197
E	0.150	0.157
H	0.228	0.244
M	0.072	0.097
N	0.067	0.092
e	0.050 BSC	
C	0.0070	0.0010
L	0.016	0.050
X	0.0215 REF	
θ1	0°	8°
θ2	7° BSC	

NOTE :
1. All dimension are in inch
2. Top package surface to be NiPdAu plating
3. Bottom package surface to be NiPdAu plating
4. Dimension are exclusive of mold flash and gate burr
5. Foot length measurement is based on the gauge plane method

Pin

PCB Mounting Pattern





Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.010").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA / JEDEC JS-001-2014
ESD – Charged Device Model (CDM)	Class C1	JEDEC JS-002-2014
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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