64M-BIT Low Voltage, Serial MASK ROM with 50MHz SPI Bus Interface

GENERAL DESCRIPTION

The N55S064 is a 64Mbit (8M Bytes) Serial Mask ROM accessed by a high speed Serial peripheral interface.

KEY FEATURES

- Operating voltage ranges from 3.0V to 3.6V
- Serial Peripheral Interface compatible-mode 0 and 3
- High performance: "fast read" mode at 50MHz and "normal read" at 20MHz
- Low power consumption: 8mA for fast read mode or 4mA for normal read mode
- Low standby current: 15uA

PIN DESCRIPTION

SYMBOL	DESCRIPTION
SCLK	Serial Clock
SI	Serial Data Input
SO	Serial Data Output
CSB	Chip Select
HOLDB	Hold to pause the device without deselecting the device
VCC	Power Supply
VSS	Ground

ORDER INFORMATION

Part No.	Speed	Grade
N55S064	20ns	Commercial

PHYSICAL SPECIFICATIONS

Chip Size: 4326.0 x 4860.0 (um)
Pad Size: 76 x 76 (um)
Die Thickness: 725 ±15 (um)

FIGURE 1. DIE PAD LOCATIONS

NOTE:

1. The IC substrate should be connected to VSS in PCB layout.

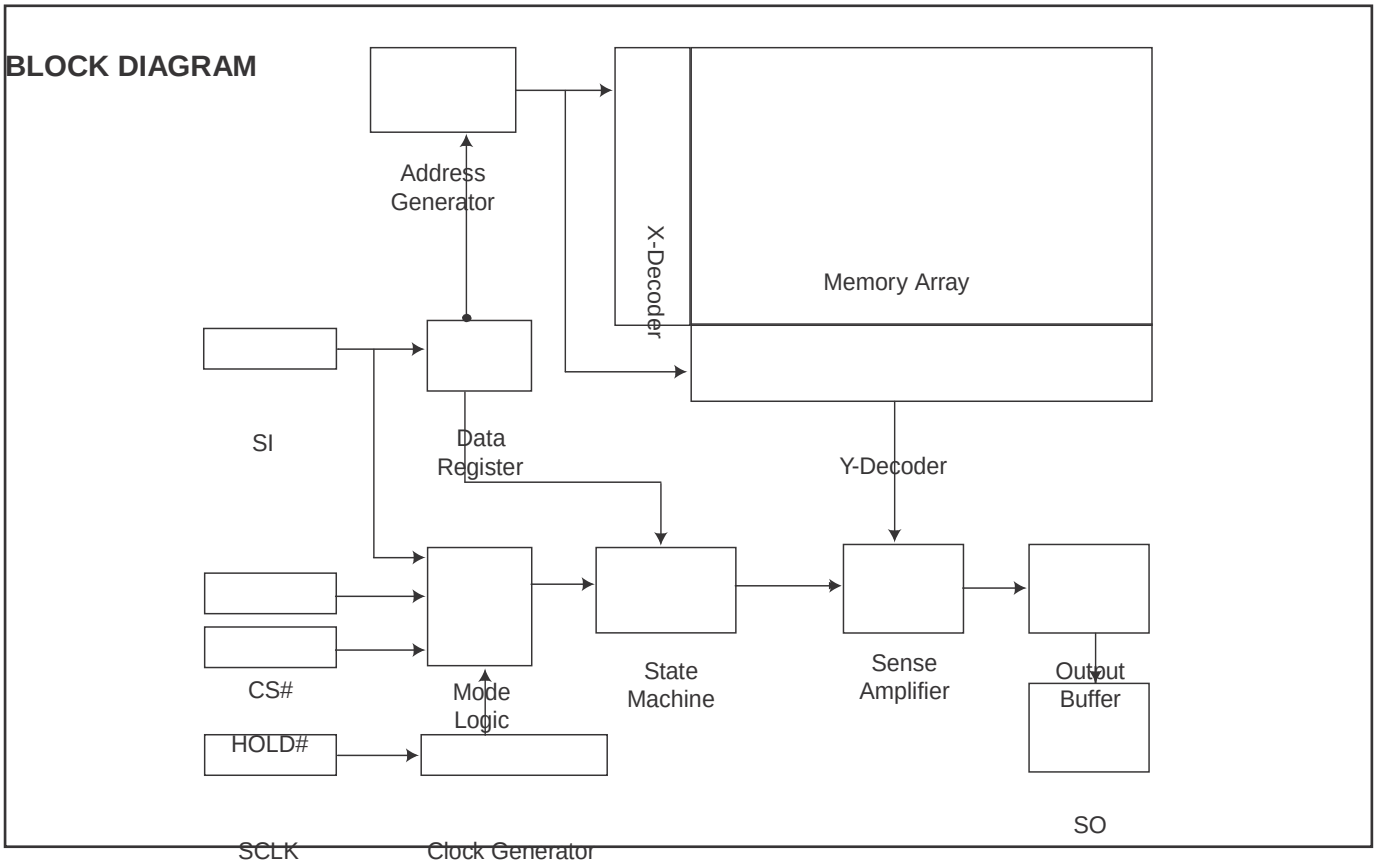
TABLE 1. PAD DESCRIPTION

ORDER	PAD-NAME	X-COORD	Y-COORD
1	HOLDB	-1920.09	-2258.71
2	VCC1	-1618.14	-2262.37
3	VCC2	-1395.43	-2262.37
4	CSB	412.80	-2258.71
5	SO	848.97	-2265.23
6	NC	1880.89	2259.56
7	VSS1	1641.88	2272.15
8	VSS2	1408.61	2272.15
9	SI	-1613.52	2259.56
10	SCLK	-1848.82	2259.56

MEMORY ORGANIZATION

The memory is organized as:
- 8M bytes

BLOCK DIAGRAM



DEVICE OPERATION

Stand-by Mode

When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps in standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z.

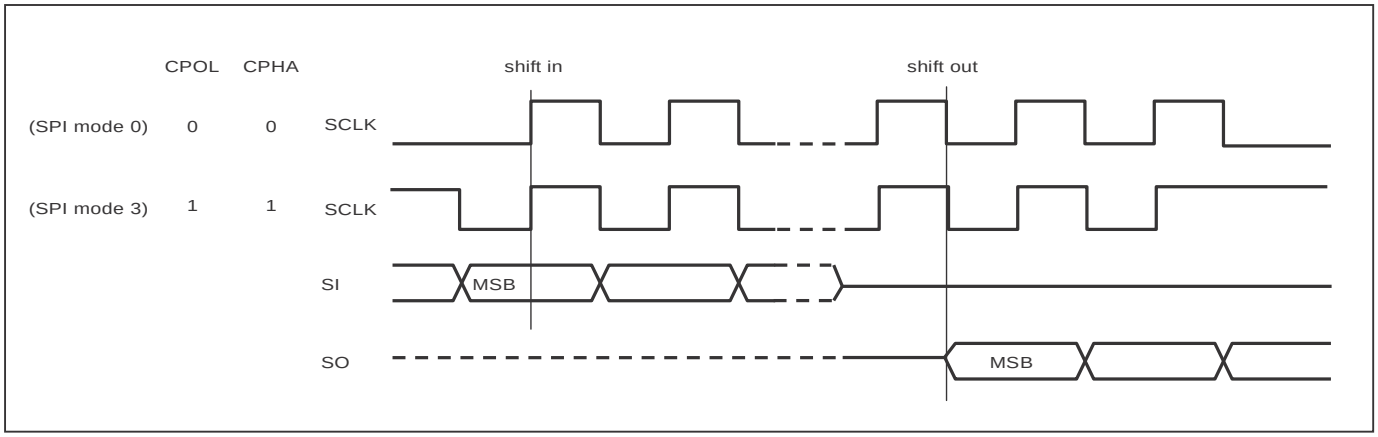
Active Mode

When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

SPI Feature

Input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of SPI mode 0 and mode 3 is shown as Figure 1.

Figure 1. SPI Modes Supported



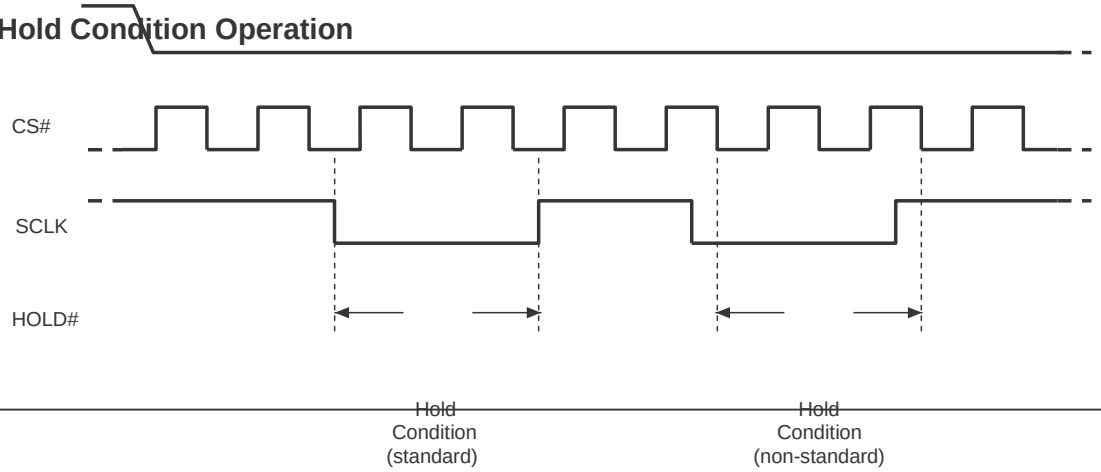
Note:
CPOL indicates clock polarity of SPI master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which SPI mode is supported.

HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device.

The operation of HOLD requires Chip Select(CS#) to stay low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal keeps to be low (if Serial Clock signal does not keep to be low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal keeps to be low(if Serial Clock signal does not keep to be low, HOLD operation will not end until Serial Clock being low), Please refer to Figure 2.

Figure 2. Hold Condition Operation



The Serial Data Output (SO) is a high impedance, that both Serial Data Input (SI) and Serial Clock (SCLK) are "don't care" during the HOLD operation. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start the communication with chip, the HOLD# must be kept as high and CS# must be kept as low.

Table 1. COMMAND DEFINITION

Command Set	1st byte Code	2nd byte	3rd byte	4th byte	5th byte	6th byte
RDID(read ID)	9Fh	Manufacturer ID	Memory type	Memory density ID		
READ (read data)	03h	AD1 (A23-A16)	AD2 (A15-A8)	AD3 (A7-A0)	Data out (D7-D0)	Note 1
Fast Read	0Bh	AD1 (A23-A16)	AD2 (A15-A8)	AD3 (A7-A0)	Dummy cycle	Data out (D7-D0)

Notes:
1. n bytes are read out until CS# goes high.
2. It is not recommended to adopt any code not in the above command definition table.

COMMAND DESCRIPTION

(1) Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and is followed by Device ID of 2-byte. The nuvoTon Manufacturer ID is C2h, the memory type ID is 05h as the first-byte device ID, and the individual device ID of second-byte ID is:15h.

The sequence of issuing RDID instruction is: CS# goes low-> sending RDID instruction code -> 24-bits ID data is sent out on SO -> to end RDID operation which can use CS# to be high at any time during data out. (see Figure 3) When CS# goes high, the device is at standby stage.

Table of ID Definitions:

RDID	manufacturer ID	memory type	memory density
9Fh	C2h	05h	17h

(2) Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low-> sending READ instruction code-> 3-byte address is sent on SI -> data out on SO-> to end READ operation which can use CS# to be high at any time during data out. (see Figure 4)

(3) Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low-> send FAST_READ instruction code-> 3-byte address is sent on SI-> 1-dummy byte address is sent on SI->data out on SO-> to end FAST_READ operation which can use CS# to be high at any time during data out. (see Figure 5)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 3. Read Identification (RDID) Sequence (Command 9F)

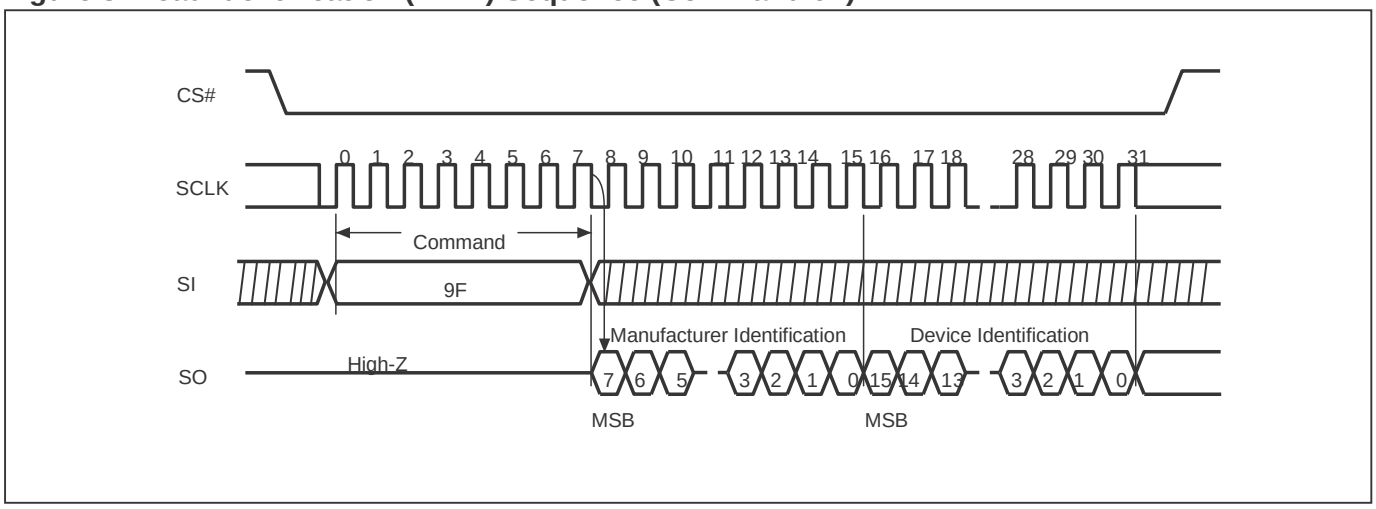


Figure 4. Read Data Bytes (READ) Sequence (Command 03)

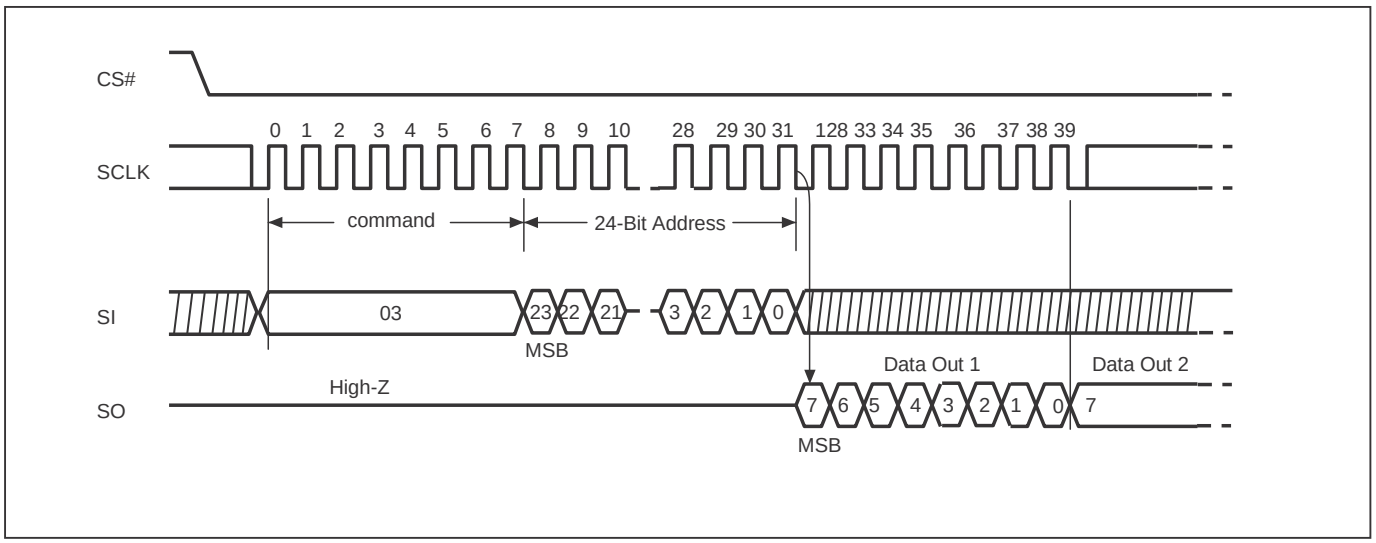
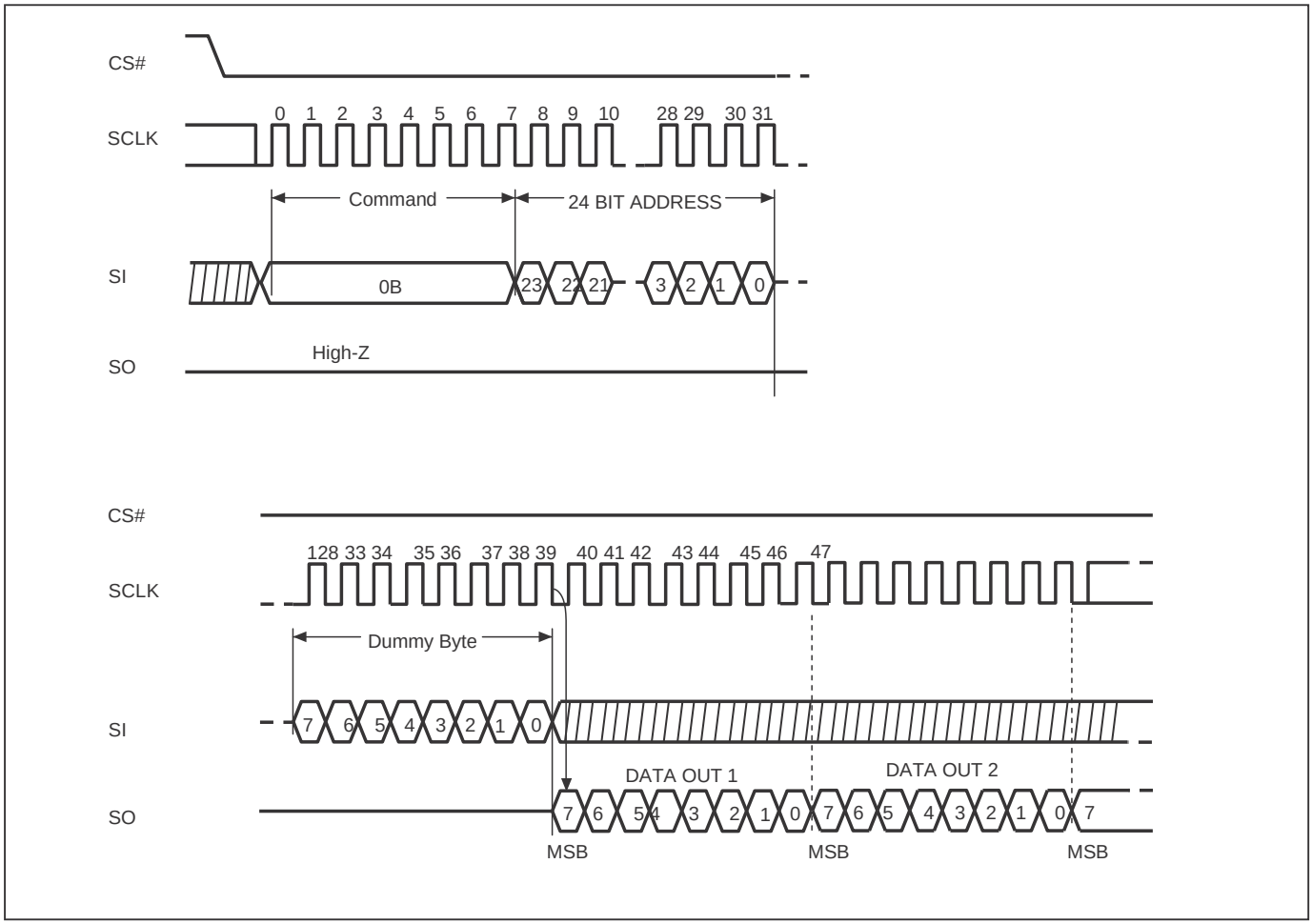


Figure 5. Read at Higher Speed (FAST_READ) Sequence (Command 0B)



ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING		VALUE
Ambient Operating Temperature	Commercial grade	0°C to 70°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.6V to 4.0V
Applied Output Voltage		-0.6V to 4.0V
VCC to Ground Potential		-0.6V to 4.0V

NOTICE:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage of the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions in long period of time may affect reliability.
2. Specifications contained within the following Table 2 and 3 are subjects to change.
3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, see Figure 6,7.

Figure 6.Maximum Negative Overshoot Waveform

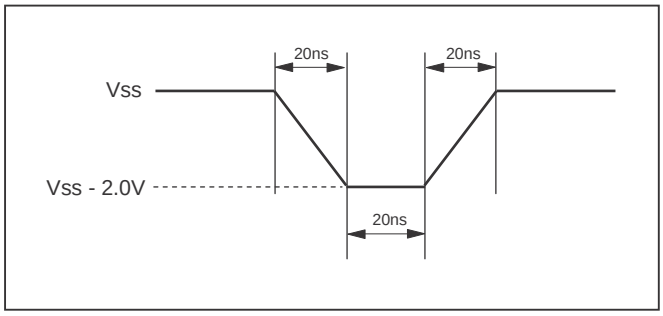
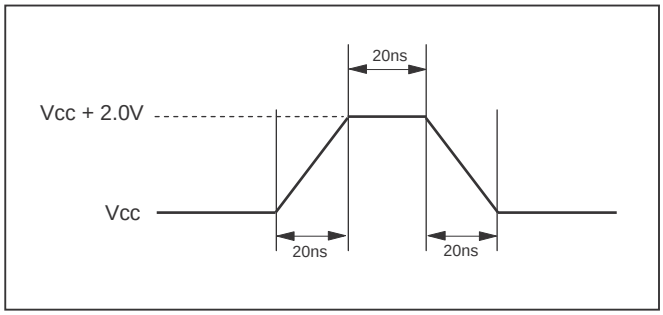


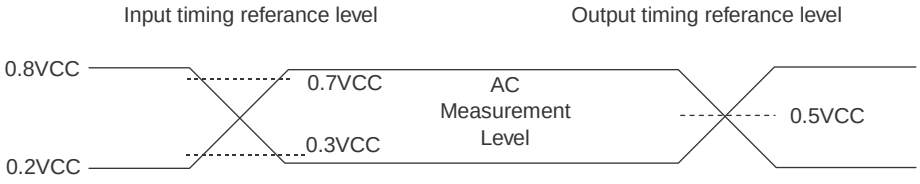
Figure 7. Maximum Positive Overshoot Waveform



CAPACITANCE TA = 25°C, f = 20 MHz

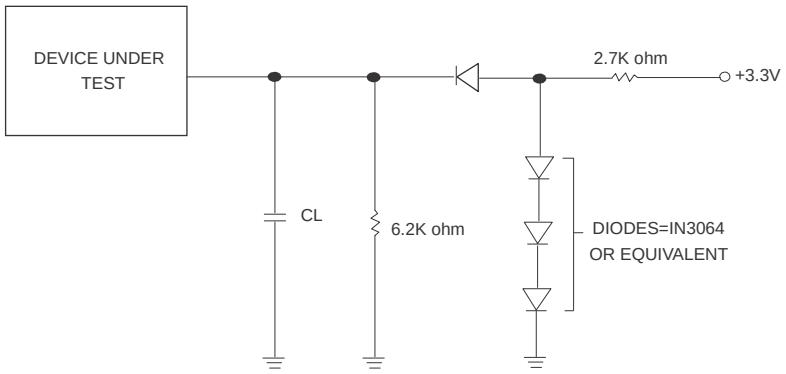
SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 8. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



Note: The rise and fall time of input pulse < 5ns

Figure 9. OUTPUT LOADING



The condition "CL=30pF" includes jig capacitance

Table 2. DC CHARACTERISTICS (Temperature = 0°C to 70°C, VCC = 3.0V ~ 3.6V)

SYMBOL	PARAMETER	NOTES	MIN.	TYP	MAX.	UNITS	TEST CONDITIONS
ISB1	VCC Standby	1			15	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1			8	mA	f=50MHz , SCLK=0.1VCC/0.9VCC, SO=Open
					4	mA	f=20MHz , SCLK=0.1VCC/0.9VCC, SO=Open
ILI	Input Load	1			± 2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage	1			± 2	uA	VCC = VCC Max, VIN = VCC or GND
VIL	Input Low Voltage		-0.5		0.3VCC	V	
VOL	Output Low Voltage				0.4	V	IOL = 1.6mA
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Table 3. AC CHARACTERISTICS (Temperature = 0°C to 70°C, VCC = 3.0V ~ 3.6V)

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for FAST_READ, RDID Commands	D.C.		50 (Condition:30pF)	MHz
fRSCLK	fR	Clock Frequency for READ Commands	D.C.		20	MHz
tCH(1)	tCLH	Clock High Time	9			ns
tCL(1)	tCLL	Clock Low Time	9			ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)	5			ns
tDVCH	tDSU	Data In Setup Time	2			ns
tCHDX	tDH	Data In Hold Time	5			ns
tCHSH		CS# Active Hold Time (relative to SCLK)	5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)	5			ns
tSHSL	tCSH	CS# Deselect Time	100			ns
tSHQZ(2)	tDIS	Output Disable Time			8	ns
tCLQV	tV	Clock Low to Output Valid			8	ns
tCLQX	tHO	Output Hold Time	0			ns
tCLCH(2)		Clock Rise Time (3) (peak to peak)	0.1			V/ns
tCHCL(2)		Clock Fall Time (3) (peak to peak)	0.1			V/ns
tHHQX(2)	tLZ	HOLD to Output Low-Z			8	ns
tHLQZ(2)	tHZ	HOLD# to Output High-Z			8	ns
tHLCH		HOLD# Setup Time (relative to SCLK)	5			ns
tCHHH		HOLD# Hold Time (relative to SCLK)	5			ns
tHHCH		HOLD Setup Time (relative to SCLK)	5			ns
tCHHL		HOLD Hold Time (relative to SCLK)	5			ns

Notes:
(1). tCH + tCL must be greater than or equal to 1/ fC.
(2). The values in the table are guaranteed by characterization, not 100% tested in production.
(3). Indicated as a slew rate.

Figure 10. Input Timing

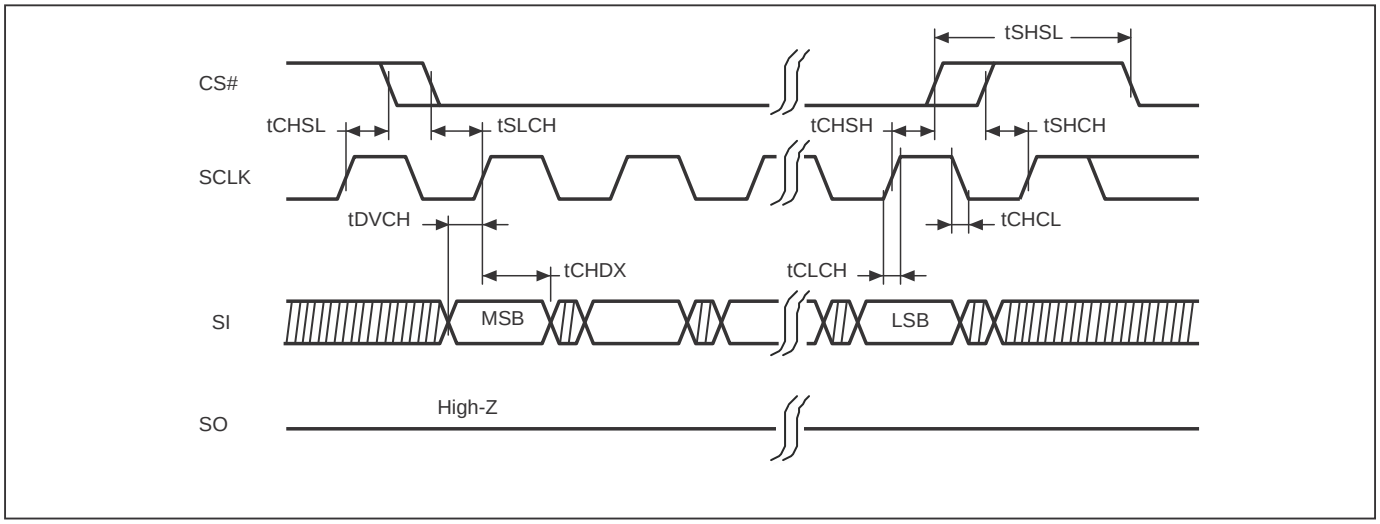


Figure 11. Output Timing

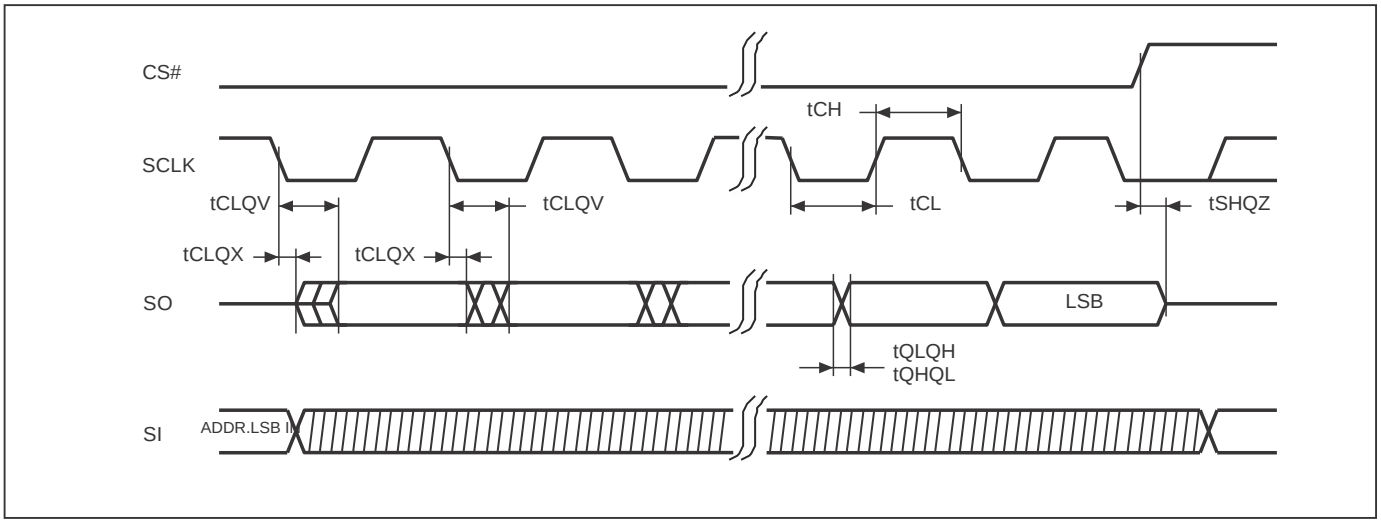
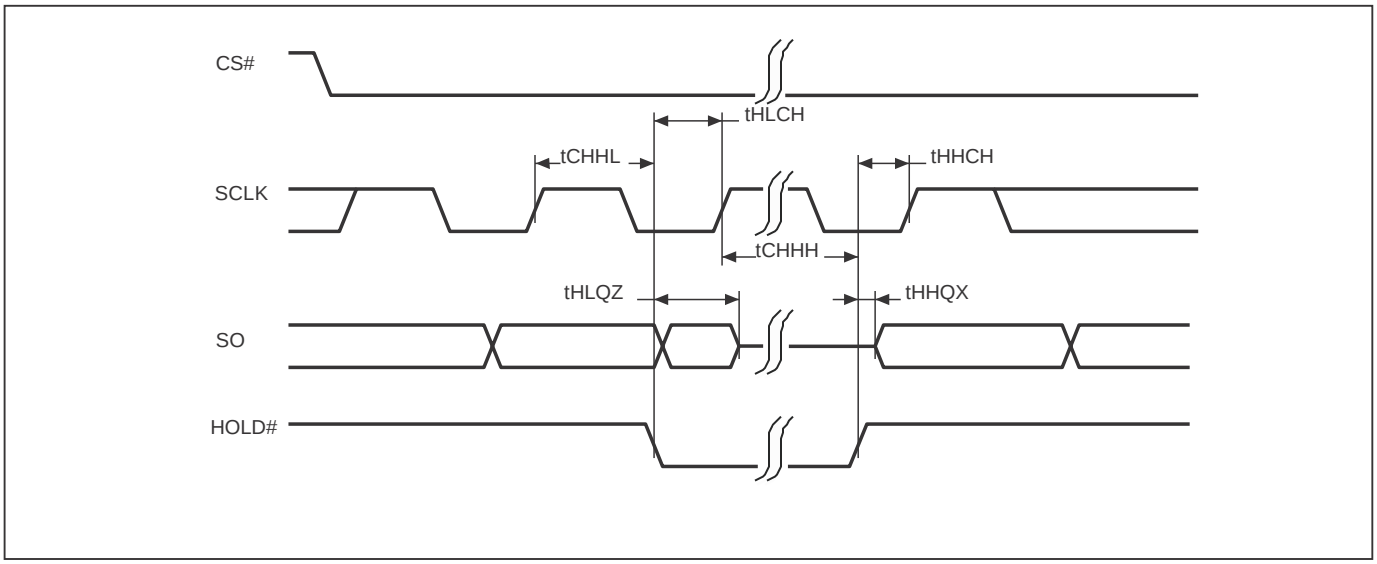


Figure 12. Hold Timing



* SI is "don't care" during HOLD operation.

Revision History

Version	Date	Substantial Changes	Page
A1.0	Jul. 2009	Initial Release	All
A1.1	Mar. 2010		

Important Notice

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