

## Description

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

## Features and Benefits:

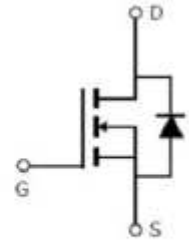
- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature



DPAK



Marking and pin Assignment



Schematic diagram

## Main Product Characteristics

$V_{DSS}$	60V
$R_{DS(on)}$	12mΩ (typ.)
$I_D$	60A

## Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D$ @ TC = 25°C	Continuous Drain Current, $V_{GS}$ @ 10V <sup>①</sup>	60	A
$I_D$ @ TC = 100°C	Continuous Drain Current, $V_{GS}$ @ 10V <sup>①</sup>	42	
$I_{DM}$	Pulsed Drain Current <sup>②</sup>	240	
$P_D$ @ TC = 25°C	Power Dissipation <sup>③</sup>	115	W
	Linear Derating Factor	0.74	W/°C
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-to-Source Voltage	± 20	V
EAS	Single Pulse Avalanche Energy @ L=0.3mH	235	mJ
IAS	Avalanche Current @ L=0.3mH	39	A
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C


## Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
R $\theta$ JC	Junction-to-case <sup>③</sup>	—	1.31	°C/W
R $\theta$ JA	Junction-to-ambient <sup>④</sup>	—	62	°C/W

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

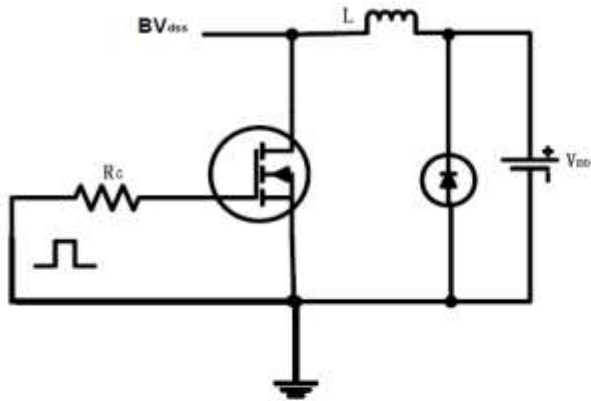
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V(BR)DSS	Drain-to-Source breakdown voltage	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250 $\mu$ A
RDS(on)	Static Drain-to-Source on-resistance	—	12	14	m $\Omega$	V <sub>GS</sub> =10V, I <sub>D</sub> = 30A
VGS(th)	Gate threshold voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 $\mu$ A T <sub>J</sub> = 125°C
		—	2.0	—		
IDSS	Drain-to-Source leakage current	—	—	2	$\mu$ A	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V T <sub>J</sub> = 150°C
		—	—	10		
IGSS	Gate-to-Source forward leakage	—	—	100	nA	V <sub>GS</sub> = 20V
		—	—	-100		V <sub>GS</sub> = -20V
Qg	Total gate charge	—	45	—	nC	I <sub>D</sub> = 30A, V <sub>DS</sub> =30V, V <sub>GS</sub> = 10V
Qgs	Gate-to-Source charge	—	4	—		
Qgd	Gate-to-Drain("Miller") charge	—	15	—		
td(on)	Turn-on delay time	—	14.6	—	ns	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, R <sub>L</sub> =15 $\Omega$ , R <sub>GEN</sub> =2.5 $\Omega$
tr	Rise time	—	14.2	—		
td(off)	Turn-Off delay time	—	40	—		
tf	Fall time	—	7.3	—		
Ciss	Input capacitance	—	1480	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1MHz
Coss	Output capacitance	—	190	—		
Crss	Reverse transfer capacitance	—	135	—		

## Source-Drain Ratings and Characteristics

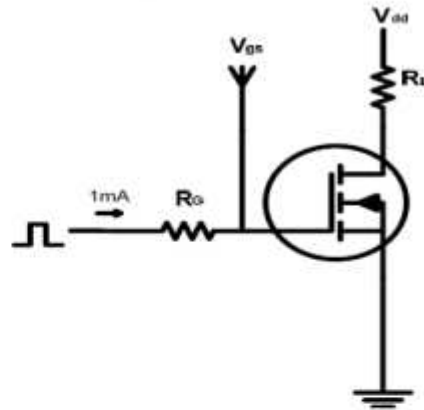
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	60	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode)	—	—	240	A	
VSD	Diode Forward Voltage	—	—	1.3	V	I <sub>S</sub> =30A, V <sub>GS</sub> =0V
trr	Reverse Recovery Time	—	33	—	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 15A,
Qrr	Reverse Recovery Charge	—	61	—	nC	di/dt = 100A/ $\mu$ s

Test circuits and Waveforms

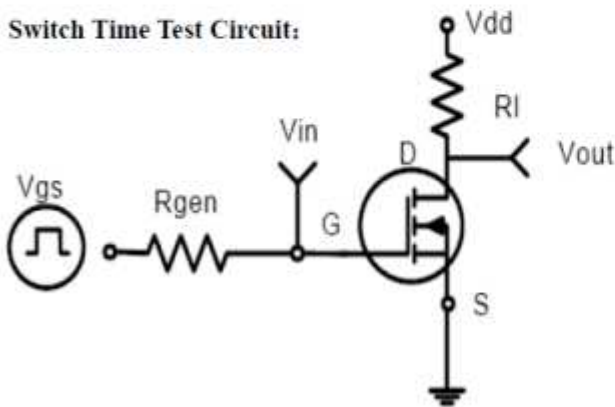
EAS test circuits:



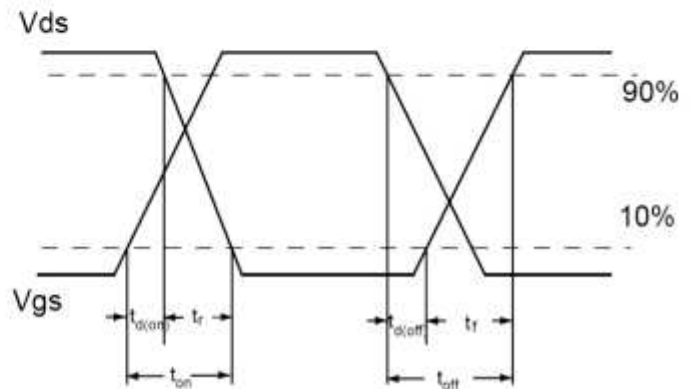
Gate charge test circuit:



Switch Time Test Circuit:



Switch Waveforms:



Notes:

- ① The maximum current rating is limited by bond-wires.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of  $R_{\theta JA}$  is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^{\circ}C$
- ⑤ These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)} = 175^{\circ}C$ .
- ⑥ The maximum current rating is limited by bond-wires.

Typical electrical and thermal characteristics

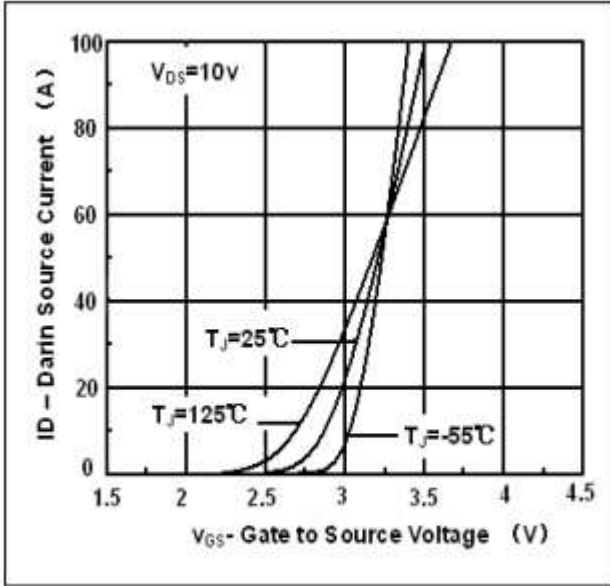


Figure 1, Transfer Characteristic

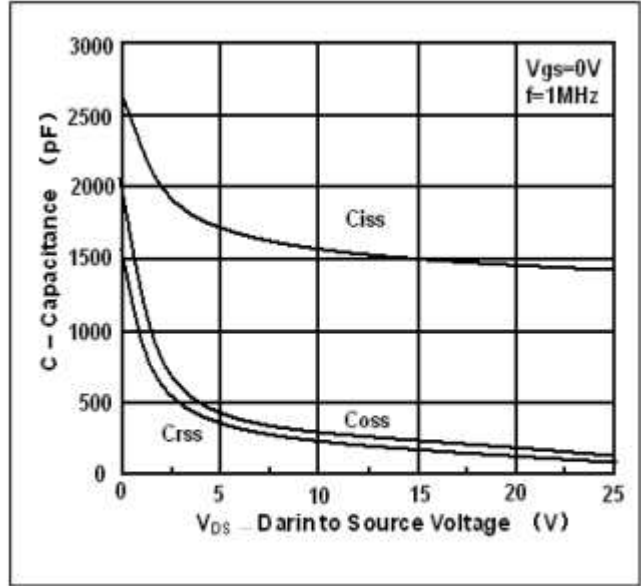


Figure 2, Capacitance

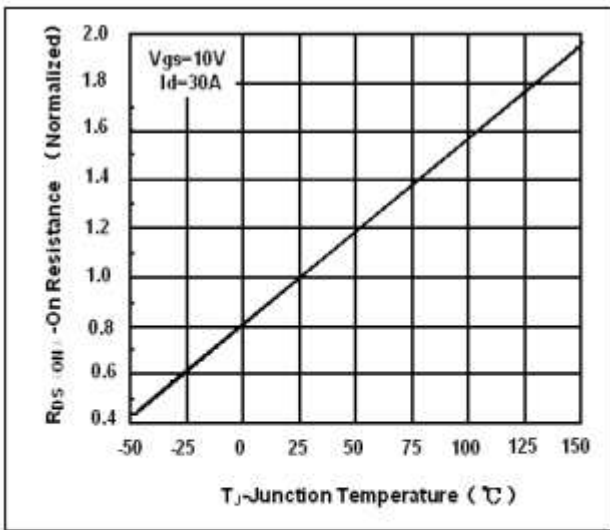


Figure 3, On Resistance vs. Junction Temperature

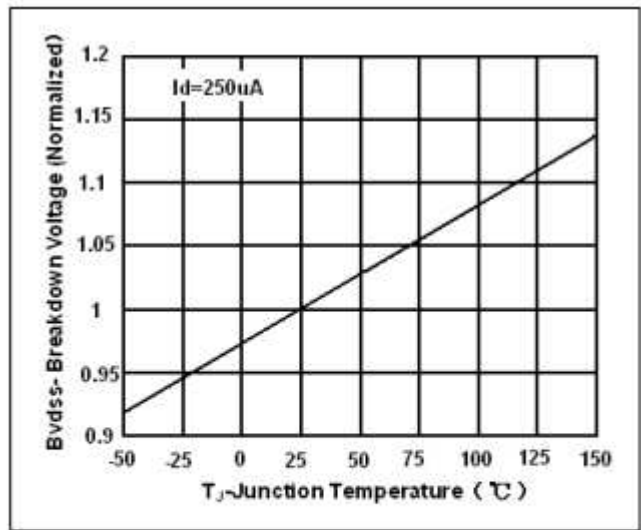


Figure 4, Breakdown Voltage vs. Junction Temperature

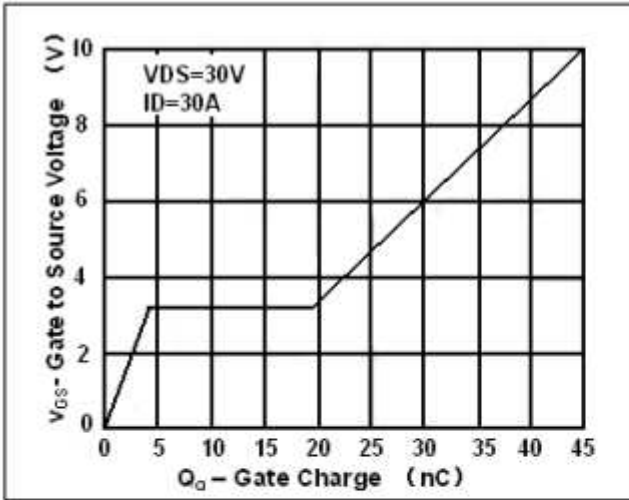


Figure 5, Gate Charge

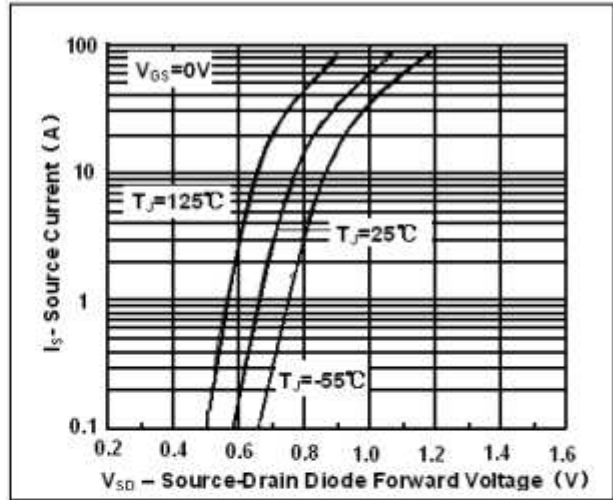


Figure 6, Source-Drain Diode Forward Voltage

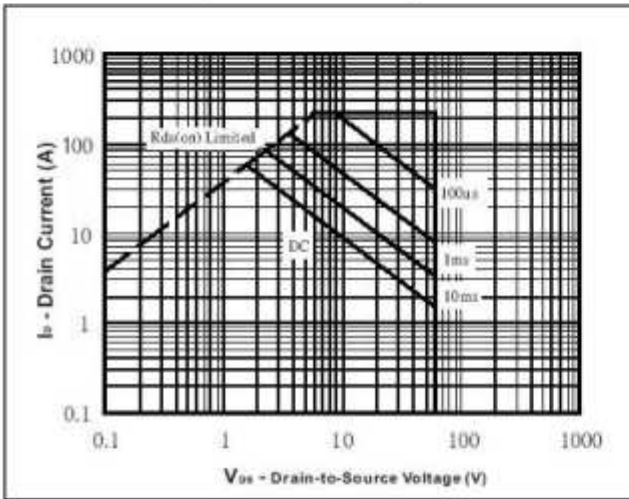


Figure 7. Safe Operation Area

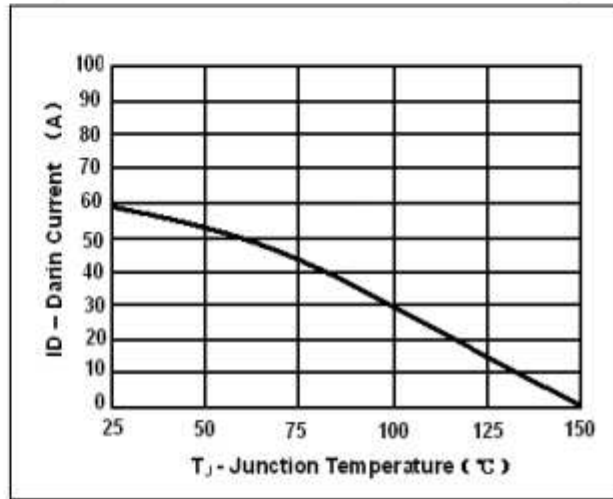


Figure 8. Max Drain Current vs. Junction Temperature

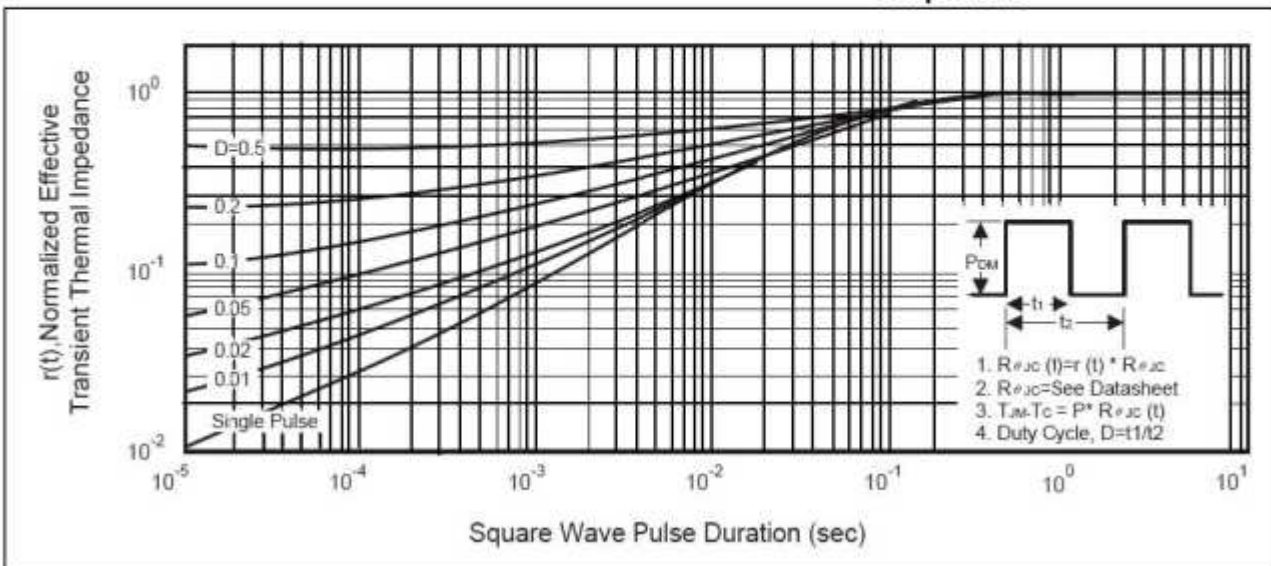
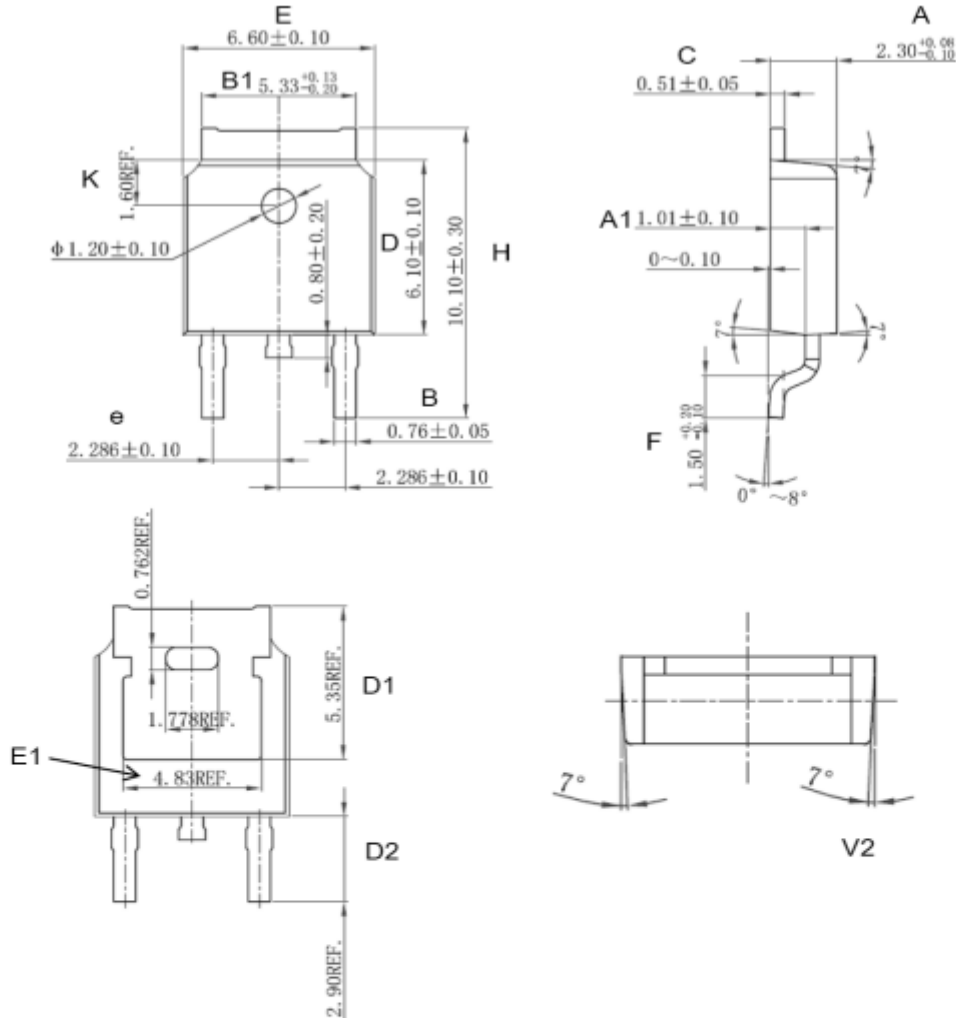


Figure 9. Transient Thermal Impedance Curve



Package Outline Dimension

DPAK PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.200	2.300	2.380	0.087	0.091	0.094
A1	0.910	1.010	1.110	0.036	0.040	0.044
B	0.710	0.760	0.810	0.028	0.030	0.032
B1	5.130	5.330	5.460	0.202	0.210	0.215
C	0.460	0.510	0.560	0.018	0.020	0.022
D	6.000	6.100	6.200	0.236	0.240	0.244
D1	5.350 (REF)			0.211 (REF)		
D2	2.900 (REF)			0.114 (REF)		
E	6.500	6.600	6.700	0.256	0.260	0.264
E1	4.83 (REF)			0.190 (REF)		
e	2.186	2.286	2.386	0.086	0.090	0.094
H	9.800	10.100	10.400	0.386	0.398	0.409
F	1.400	1.500	1.700	0.055	0.059	0.067
K	1.600 (REF)			0.063 (REF)		
V2	8° (REF)			8° (REF)		