8 KEYS TOUCH PAD DETECTOR IC

GENERAL DESCRIPTION

The TTP229-FSD TonTouch™ IC is capacitive sensing design specifically for touch pad controls. The device built in regulator for touch sensor. Stable sensing method can cover diversity conditions. Human interfaces control panel links through non-conductive dielectric material. The main application is focused at replacing of the mechanical switch or button. The ASSP can independently handle the 8 touch pads.

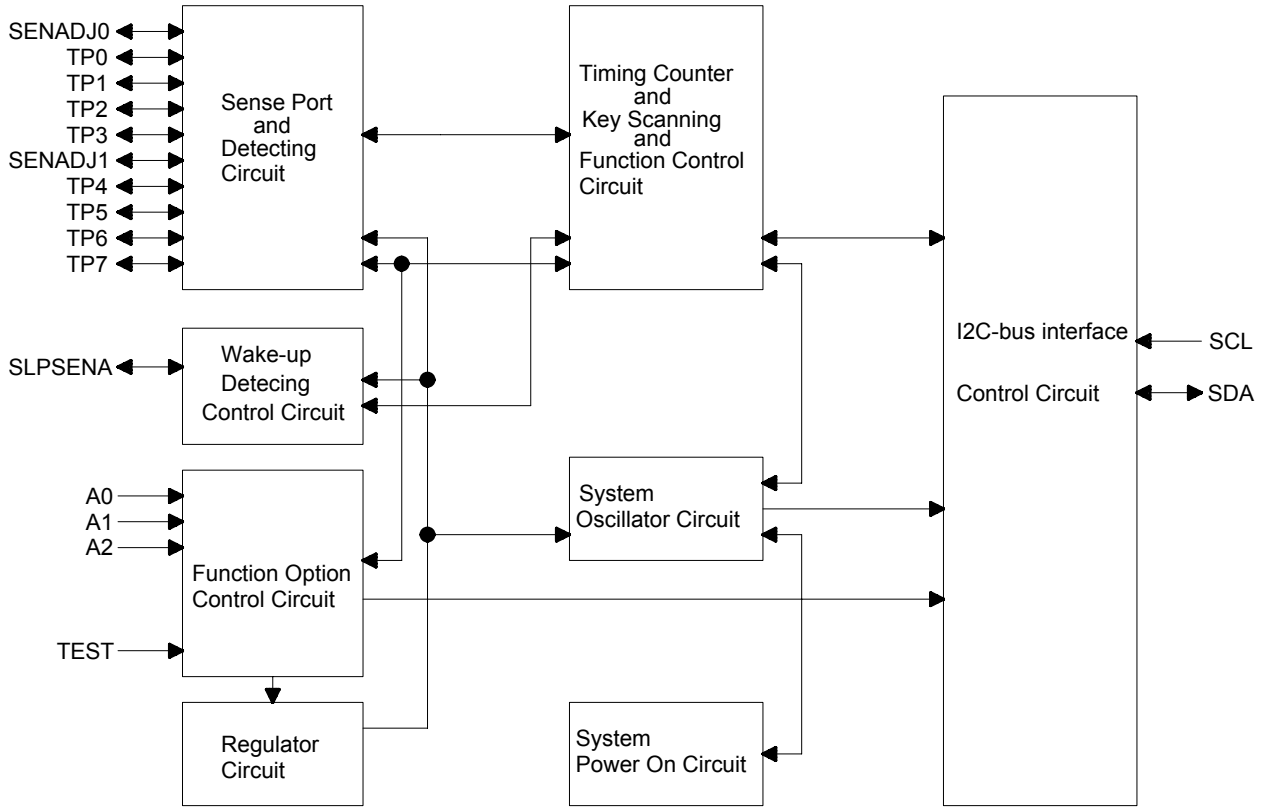
FEATURES

- Operating voltage：2.4V~5.5V
- Built-in regulator
- Stand-by current
  At 3V, and sleep mode slow sampling rate 8Hz：=> Typical 2.0uA
- Provides I^2C-bus slave interface
- Offer multi-key or single-key feature by option
- Provides two kinds of sampling rate that slow sampling rate 8Hz
  and fast sampling rate 64Hz at sleep mode
- Have the maximum key-on time about 80sec by pin option
- Sensitivity can adjust by the capacitance(1~50pF) outside
- After power-on have about 0.5sec stable-time,
  During the time do not touch the key pad, and all functions are disabled
- Auto calibration for environment changing
  And the re-calibration period is about 4.0sec, when all keys are not activated for fixed time

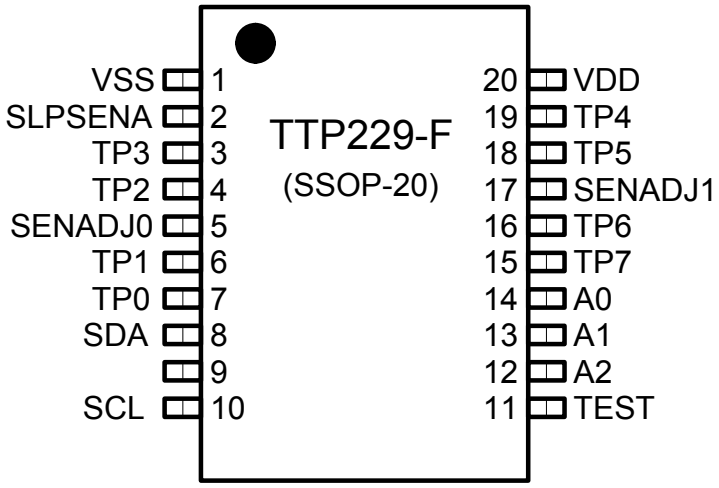
APPLICATION

- Wide consumer products
- Button key replacement

BLOCK DIAGRAM



PACKAGE CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	Share Pin	I/O Type	Pin Description
1	VSS		P	Negative power supply, ground
2	SLPSENA		I/O	Sleep mode sensitivity adjustment pin for group-A(TP0~7)
3	TP3	SKMS1	I/O	Touch pad input pin(KEY-3) Key action function option-1(Single-key/Multi-key) Default is all single-key
4	TP2		I/O	Touch pad input pin(KEY-2)
5	SENADJ0		I/O	Touch pad TP0~3 sensitivity adjust common pin
6	TP1		I/O	Touch pad input pin(KEY-1)
7	TP0		I/O	Touch pad input pin(KEY-0)
8	SDA		I/OD	Data pin for the I^2C-bus serial data interface
9	NC			
10	SCL		I	Serial clock input pin for the I^2C-bus serial interface
11	TEST		I-PL	Only for test
12	A2		I-PH	A2~0 are input pins for the I^2C-bus device address selection
13	A1		I-PH	A2~0 are input pins for the I^2C-bus device address selection
14	A0		I-PH	A2~0 are input pins for the I^2C-bus device address selection
15	TP7	SKSRT	I/O	Touch pad input pin(KEY-7) Maximum key-on time function option(Infinite/80sec) Default is infinite
16	TP6	SLWPTM	I/O	Touch pad input pin(KEY-6) Sleep mode sampling length function option(4.0/2.0mS) Default is 4.0ms
17	SENADJ1		I/O	Touch pad TP4~7 sensitivity adjust common pin
18	TP5	WPSCT	I/O	Touch pad input pin(KEY-5) Sampling rate at sleep mode function option(8Hz/64Hz) Default is 8Hz
19	TP4	SKMS0	I/O	Touch pad input pin(KEY-4) Key action function option-0(Single-key/Multi-key) Default is all single-key
20	VDD		P	Positive power supply

Note：Pin Type

I ＝＞CMOS input only
I-PH ＝＞CMOS input and pull-high resister
I-PL ＝＞CMOS input and pull-low resister
O ＝＞CMOS push-pull output
I/O ＝＞CMOS I/O
P ＝＞Power / Ground
OD ＝＞CMOS open drain output

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit
Operating Temperature	T_{OP}	—	-40 ~ +85	℃
Storage Temperature	T_{STG}	—	-50 ~ +125	℃
Power Supply Voltage	VDD	Ta=25°C	VSS-0.3 ~ VSS+6.0	V
Input Voltage	V_{IN}	Ta=25°C	VSS-0.3 to VDD+0.3	V
Human Body Mode	ESD	—	6	KV
Note：VSS symbolizes for system ground				

• DC/AC Characteristics：(Test condition at room temperature=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD		2.4	-	5.5	V
Internal Regulator Output	VREG		2.2	2.3	2.4	V
Operating Current (no load)	I_{OP}	VDD=3.0V		20		uA
Stand-by Current (VDD=3.0V) (Sampling length 4.0mS)	I_{SD}	Sampling rate 8Hz		2.0		uA
		Sampling rate 64Hz		5.5		
Input Ports	V_{IL}	Input Low Voltage	0	-	0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8	-	1.0	VDD
Output Port Sink Current	I_{OL}	VDD=3V, V_{OL}=0.6V	-	8	-	mA
Output Port Source Current	I_{OH}	VDD=3V, V_{OH}=2.4V	-	-4	-	mA
Wake-up Response Time (at sleep mode)	T_{WU}	VDD=3V, Sampling rate 8Hz		125		mS
		VDD=3V, Sampling rate 64Hz		15.6		mS
Output Response Time (at operation)	T_R	VDD=3V		16		mS
Maximum Key-on Time	T_{MOT}		50	80	110	Sec
Input Pin Pull-high Resistor (A0~A2)	R_{PH}	VDD=3V,		30K		ohm
Input Pin Pull-low Resistor (TEST)	R_{PL}	VDD=3V		30K		ohm

FUNCTION DESCRIPTION

1. Sensitivity adjustment

The total loading of electrode size and capacitance of connecting line on PCB can affect the sensitivity. So the sensitivity adjustment must according to the practical application on PCB. The TTP229-FSD offers some methods for adjusting the sensitivity outside.

1-1 by the electrode size

Under other conditions are fixed. Using a larger electrode size can increase sensitivity. Otherwise it can decrease sensitivity. But the electrode size must use in the effective scope.

1-2 by the panel thickness

Under other conditions are fixed. Using a thinner panel can increase sensitivity. Otherwise it can decrease sensitivity. But the panel thickness must be below the maximum value.

1-3 by the value of external capacitor (please see the down Figure 1-3-1)

Under other conditions are fixed. When adding the values of CJ0~CJ1 and CJWA will reduce sensitivity in the useful range (1pF≦CJ0~CJ1≦50pF, 1pF≦CJWA≦50pF). When do not use any capacitor that means open on the position of capacitor, the sensitivity is most sensitive. The capacitors CJ0~CJ1 are used to adjust the sensitivity of keys at operation mode. The capacitors CJWA is used to adjust the Wake-up sensitivity at sleep mode.

About the relation of capacitor and controlled keys please to see below table.

The capacitor	The keys-group controlled and adjusted
CJ0	K0~K3 group
CJ1	K4~K7 group
CJWA	K0~K7 group

Note：When using the value of capacitor to adjust the sensitivity, recommending to adjust the CJ0~CJ1 capacitor for K0~K7 first, then adjusting the CJWA capacitor for Wake-up sensitivity.

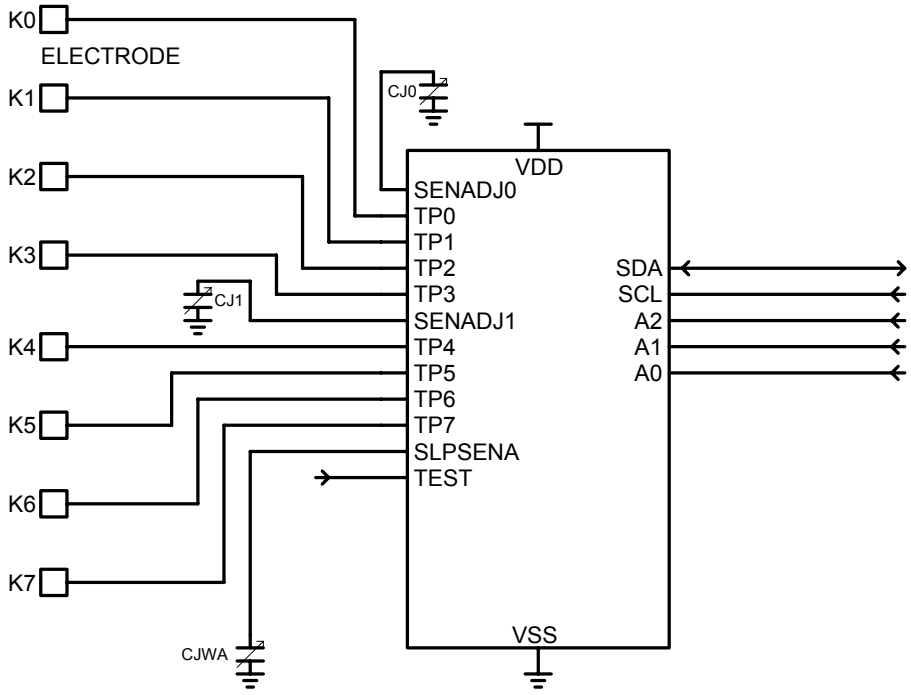


Figure 1-3-1

2. Input keys number

The TTP229-FSD has only 8 keys input mode.

3. Output mode

The TTP229-FSD only has I²C-bus slave interface mode.

At the mode the SDA pin is a serial data pin, the SCL is a serial clock input pin. The SDA and SCL pins must be pulled-high with an external resistor.

And the 4-bits identify code for the TTP229-FSD is 〝(1010)〞. The device address is defined by the state of the A0, A1 and A2 pins. The three pins have pull-high resistor internal, can be set to 0 external.

The TTP229-FSD 8-bits slave device address includes 4-bits identifier, 3-bits option address and R/W bit (see the Table 3-1).

The TTP229-FSD IC uses the I²C-bus slave interface data transmission protocol to output the data of the touch pads (TP0~TP7 pins), so the TTP229-FSD only accepts the read operation that R/W bit is 〝1〞. If it is 〝0〞, the TTP229-FSD will not respond the write operation. Otherwise, the I²C-bus slave interface of TTP229-FSD conforms to the communication protocols. It supports the fast mode that the maximum SCL clock frequency is 400KHz.

The I²C-bus slave interface supports the following communication protocols:

Bus not busy : The SDA and the SCL lines remain High level when the bus is not active.

Start condition : Start condition is SDA 1 to 0 transition when SCL=1.(see figure 3-2)

Stop condition : Stop condition is SDA 0 to 1 transition when SCL=1.(see figure 3-2)

Data valid : Following a start condition, the data on the SDA line must be stable during the High period of SCL. The High or Low state of the data line can only change when the clock signal on the SCL line is Low.(see figure 3-2)

ACK (Acknowledge) : An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the ninth clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it successfully received the eight bits of data. But the slave does not send an ACK if it does not successfully received the eight bits of data.

In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the ninth clock period. If an ACK is detected, the slave will continue to transmit next data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.

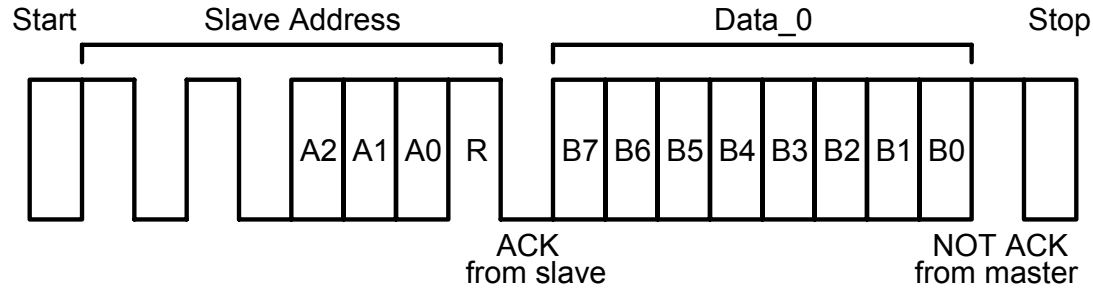
Slave Address : The identify code for the TTP229-FSD is 〝(1010)〞. The device address can be set by the state of the A2, A1 and A0 pins.

Read/Write : The final (eighth) bit of the slave address defines the type of operation to be performed. If the R/W bit is 〝1〞, a read operation is executed. If it is 〝0〞, a write operation is executed. But the TTP229-FSD only accepts read operation.

The sequence of read data operation please see figure 3-1.

Table 3-1. Slave Device Addressing

Device	Device Identifier				Device Address			R/W Bit
	B7	B6	B5	B4	B3	B2	B1	B0
TTP229-FSD	1	0	1	0	A2	A1	A0	R



Note : Data_0 : B7~B0 is TP0~TP7 on/off status. 0 is key off, 1 is key on.

Figure 3-1. Read Operation Sequence

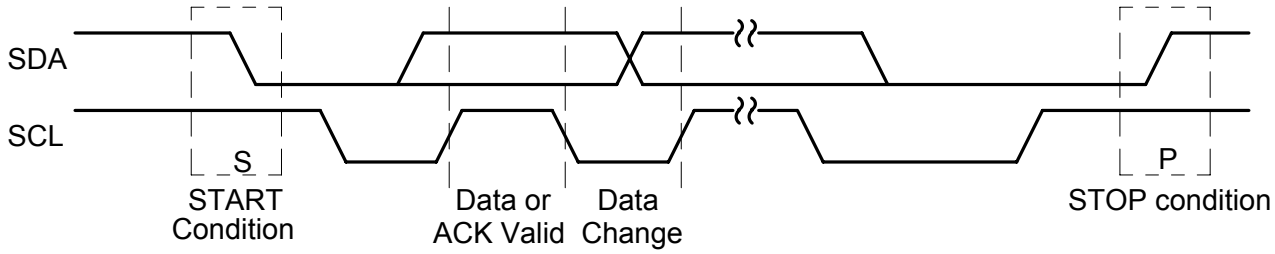


Figure 3-2. Data Transmission Sequence

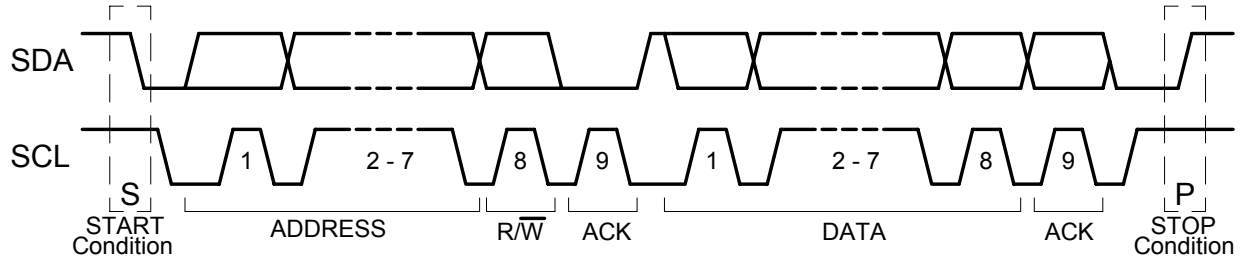


Figure 3-3. A complete data transfer

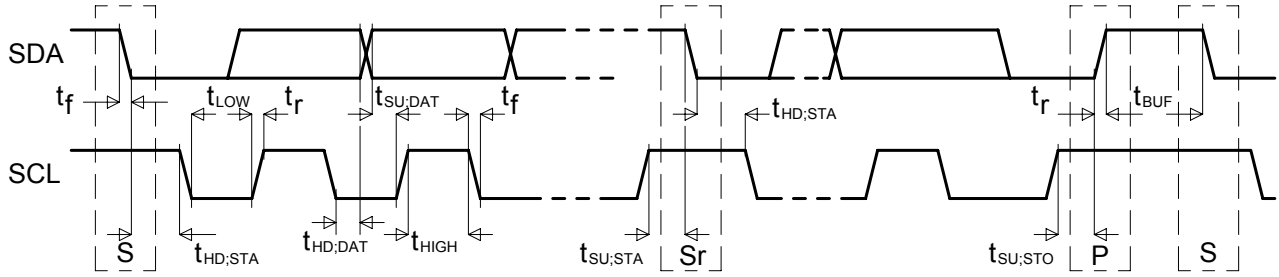


Figure 3-4. Definition of timing for F/S-mode devices on the I^2C-bus

Table 3-2. Characteristics of the SDA and SCL bus lines for F/S-mode I^2C-bus devices

Parameter	Symbol	Standard-Mode		Fast-Mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}		100		400	KHz
LOW period of the SCL clock	t_{LOW}	4.7		1.3		us
HIGH period of the SCL clock	t_{HIGH}	4.0		0.6		us
Hold time (repeated) START condition	$t_{HD;STA}$	4.0		0.6		us
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7		0.6		us
Data hold time	$t_{HD;DAT}$	0		0		us
Data set-up time	$t_{SU;DAT}$	250		100		ns
Rise time of both SDA and SCL signals	t_r		1000		300	ns
Fall time of both SDA and SCL signals	t_f		300		300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0		0.6		us
Bus free time between a STOP and START condition	t_{BUF}	4.7		1.3		us
Capacitive load for each bus line	C_b		400		400	pF

4. Key operating mode

The TTP229-FSD has the Single-key and Multi-key functions. These functions are set by TP3(SKMS1) and TP4(SKMS0) pins. The all 8 keys can use one group, or the 8 keys can distributed into two groups. The group-1 includes TP0, TP1, TP2, TP3 keys. The group-2 includes TP4, TP5, TP6, TP7 keys. How to set the function? Please see below table 4-1：

Table 4-1. The functions of TP3(SKMS1) and TP4(SKMS0) option

TP3 (SKMS1)	TP4 (SKMS0)	Operating function
1	1	All Single-keys：one group(8keys)
1	0	Two groups operate：group-1=>Single key；group-2=>Single key
0	1	Two groups operate：group-1=>Single key；group-2=>Multi key
0	0	All Multi-keys：one group(8 keys)

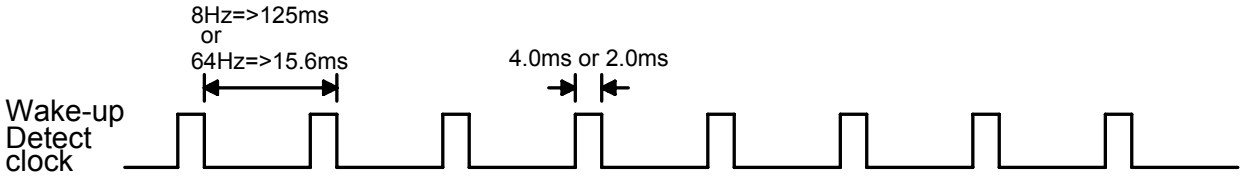
Note：1. One group：TP0~TP7.
Two groups：Group-1=>TP0,TP1,TP2,TP3.
Group-2=>TP4,TP5,TP6,TP7.

2. The option states of TP3 and TP4, the〝0〞state is used a high-value resistor connected to VSS, the〝1〞state is not used resistor connected to VSS.
3. The key detection acknowledges in Single-key function, the priority is by the key scanning order (from TP0 to TP7) when many keys are touched effectively. It is not by the key touching strength.

5. Wake-up sampling rate and sampling length at sleep mode

The TTP229-FSD has two kinds of sampling rate at sleep mode. These are 8Hz and 64Hz. The two functions are selected by TP5(SLWPTM) pin. The TP5(SLWPTM) pin has used a high-value resistor connected to VSS, it selected the 64Hz sampling rate. Another it is 8Hz that is not used resistor connected to VSS. The 8Hz sampling is the default.
And TTP229-FSD has two kinds of sampling length at sleep mode. They are 4ms and 2ms that are selected by TP6(WPSCT) pin. The default is 4ms that TP6(WPSCT) pin is not used resistor connected to VSS. Another it is 2ms that TP6 pin has used a high-value resistor connected to VSS.

Wake-up sampling timing and length in the sleep mode：



6. Maximum key-on time

If some objects cover in the sense pad, and causing the change quantity enough to be detected. To prevent this, the TTP229-FSD sets a timer to monitor the detection. The timer is the maximum key-on time. It is set about 80sec at 3V. When the detection is over the timer, the system will return to the power-on initial state, and the output becomes inactive until the next detection. The function is set via a high-value resistor connected to the TP7(SKSRT) pin to VSS. The TP7(SKSRT) pin does not has the resistor, it is set disable the maximum key-on time, then the key acts infinitely, this is the default. Another it is set enable the maximum key-on time that has a resistor.

7. Built-in regulator

The capacitive sensing touch pad IC needs stable power. So the TTP229-FSD built in regulator in the chip. It can make the internal power to keep up steady. And the sensitivity detection is normal for chip. And the stable power can avoid sensitivity anomalies and false detections.

8. Auto calibration function

The TTP229-FSD includes a full auto-calibration function. After the device is powered-on, it will calibrate the initial condition of environment first. On the duration time all the functions are disabled, so do not operate. Then the system is into stand-by mode. And all keys are not detected touch more than about 4 seconds, then the system do re-calibration automatically. The procedure is fixed and repeated. By implementing this feature the system can catch the conditions of environment changing. And let operation of the system is normal.

9. The timing from sleep mode to operation mode

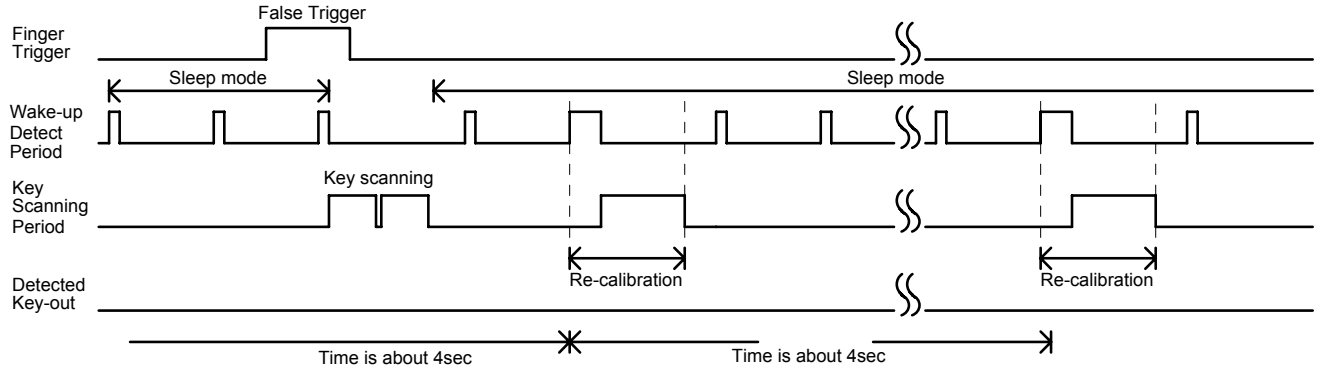


Figure 9-1. The timing for false trigger

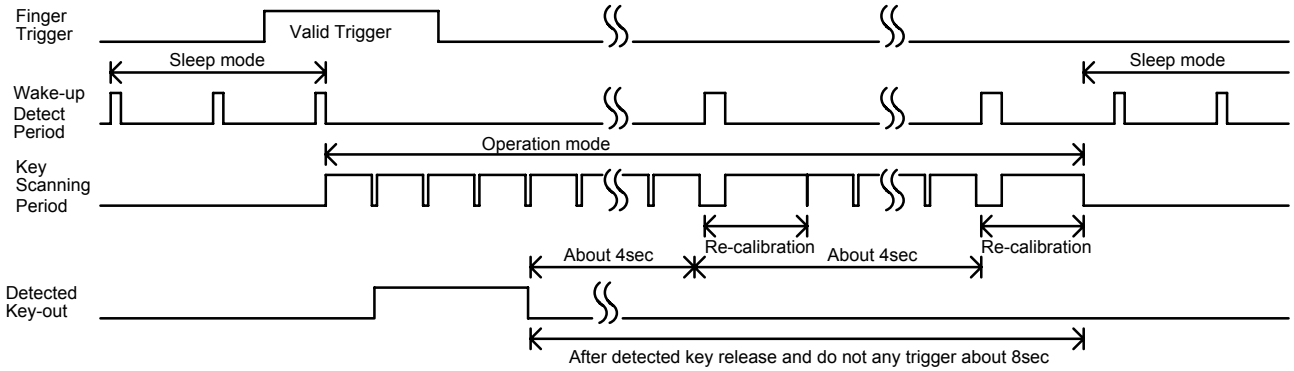


Figure 9-2. The timing for valid trigger

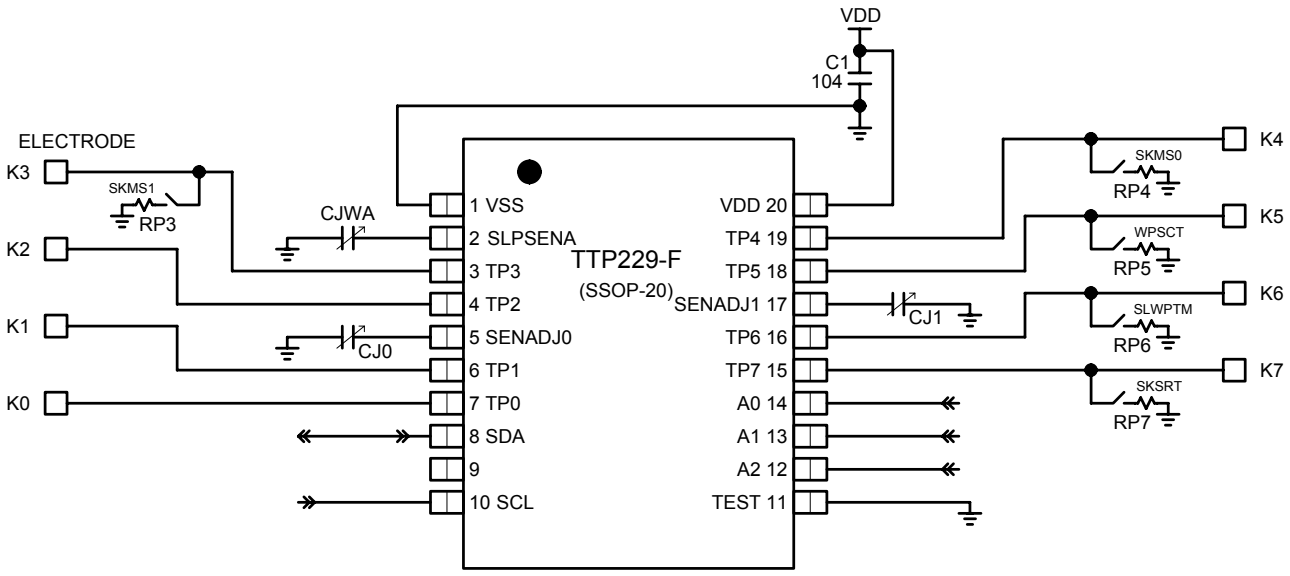
10. Option table

Option table：

Option pin	Option states		Feature	Remark
	TP3 (SKMS1)	TP4 (SKMS0)		
TP3 (SKMS1)	1	1	All Single-keys：one group(8keys)	Default
	1	0	Two groups operate： group-1=>Single key；group-2=>Single key	
TP4 (SKMS0)	0	1	Two groups operate： group-1=>Single key；group-2=>Multi key	
	0	0	All Multi-keys：one group(8 keys)	
TP5 (WPSCT)	1		8Hz sampling rate for wake-up in sleep mode	Default
	0		64Hz sampling rate for wake-up in sleep mode	
TP6 (SLWPTM)	1		Wake-up sampling length=>about 4.0ms	Default
	0		Wake-up sampling length=>about 2.0ms	
TP7 (SKSRT)	1		Maximum key-on time disable=>infinite	Default
	0		Maximum key-on time enable=>about 80sec	

Note：1. About the combinations of group-1 and group-2, please see above point-4.
2. Option states “1” mean internal pull-up (default).
3. Option states “0” mean that option pins are via high-value resistors connected to VSS.

APPLICATION CIRCUIT



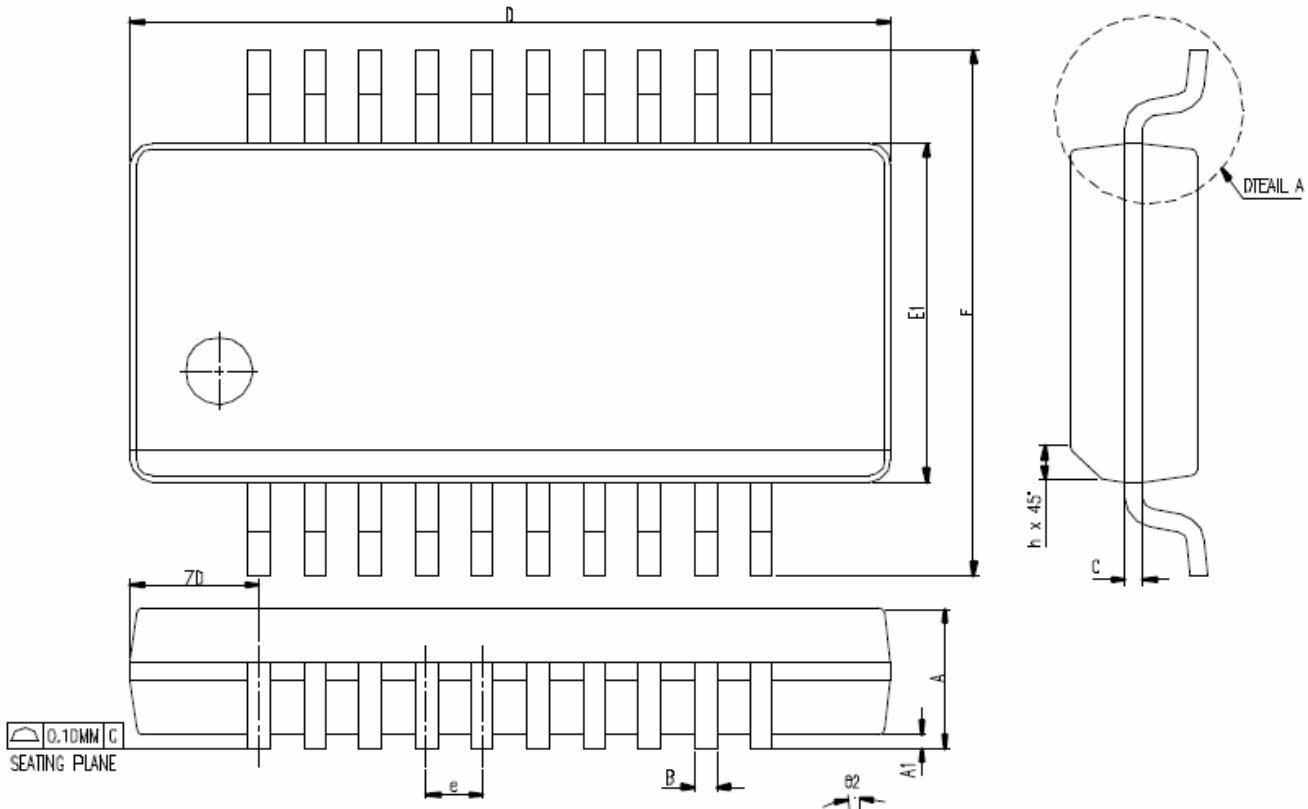
PS：1. On PCB, the length of lines from touch pad to IC pin shorter is better.
And the lines do not parallel and cross with other lines.

2. The power supply must be stable. If the supply voltage drift or shift quickly, maybe causing sensitivity anomalies or false detections.
3. The material of panel covering on the PCB can not include the metal or the electric element. The paints on the surfaces are the same.
4. The C1 capacitor must be used between VDD and VSS; and should be routed with very short tracks to the device's VDD and VSS pins (TTP229-FSD).
5. The capacitance CJ0~CJ1 and CJWA can be used to adjust the sensitivity. The value of capacitors use smaller, then the sensitivity will be better. The sensitivity adjustment must according to the practical application on PCB. The range value of capacitors are 1pF≦CJ0~CJ1≦50pF, 1pF≦CJWA≦50pF. Recommend to adjust the CJ0~CJ1 capacitor for K0~K7 first, then adjusting the CJWA capacitor for Wake-up sensitivity.
6. The sensitivity adjustment capacitors (CJ0~CJ1, CJWA) must use smaller temperature coefficient and more stable capacitors. Such are X7R, NPO for example. So for touch application, recommend to use NPO capacitor, for reducing that the temperature varies to affect sensitivity.
7. Recommend to use 820K ohm resistor for RP3~RP7 resistors.

PACKAGE OUTLINE (20 PIN SSOP)

Package Type: SSOP-20

Package Outline Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			1.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025 BASIC		
D	8.56	8.66	8.74	0.337	0.341	0.344
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25		0.50	0.010		0.020
ZD	1.4732REF			0.058 REF.		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ1	0°			0°		
θ2	5°	10°	15°	5°	10°	15°
JEDEC	MO-137 (AD)					

NOTES : DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS.
MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 INCH PER SIDE.

ORDER INFORMATION

a. Package form: TTP229-FSD

REVISE HISTORY

1. 2009/12/03
   -Original version：V_1.0
2. 2009/12/22 =>V_1.1
   -Adding some descriptions for function.
   A. Adding the description of Stand-by current at the page-4.
   B. Adding the description of Single-key function at the page-9 point 4 note 3 …….
   C. Changing and adding the Maximum Key-on Time value at the page-1, 3, 4, 9, 11.
   D. Changing the description of Table 4-1 at the page-9.
   E. Changing the values for RP3~RP7 resistors from 1M to 820K at page-12 PS: 7.