IP3053CX5; IP3053CX10; IP3053CX15; IP3053CX20

Integrated 2, 4, 6 and 8-channel passive EMI-filter network with high-level ESD protection to IEC 61000-4-2 level 4

Rev. 01 — 3 May 2010 Product data sheet

1. Product profile

1.1 General description

IP3053CX5, IP3053CX10, IP3053CX15 and IP3053CX20 is a 2, 4, 6 and 8-channel LC low-pass filter array family which is designed to provide filtering of undesired RF signals on the I/O ports of portable communication or computing devices. In addition, IP3053CX5, IP3053CX10, IP3053CX15 and IP3053CX20 incorporates diodes to provide protection to downstream components from ElectroStatic Discharge (ESD) voltages as high as ±8 kV according IEC 61000-4-2 level 4.

The devices are fabricated using monolithic silicon technology and integrate and incorporate up to 8 inductors and up to 16 diodes in a 0.5 mm pitch Wafer-Level Chip-Scale Package (WLCSP).

1.2 Features and benefits

- Pb-free, RoHS compliant and free of halogen and antimony (Dark Green compliant)
- Integrated 2, 4, 6 and 8-channel π-type LC-filter network
- 18 Ω channel series resistance; ≤ 45 pF (at 2.5 V DC) channel capacitance
- Integrated ESD protection withstanding ±8 kV contact discharge
- WLCSP with 0.5 mm pitch

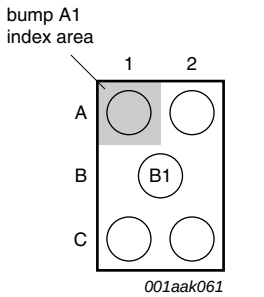
1.3 Applications

General purpose ElectroMagnetic Interference (EMI) and Radio Frequency Interference (RFI) filtering and downstream ESD protection for:

- Cellular and Personal Communication System (PCS) mobile handsets
- Cordless telephones
- Wireless data (WAN/LAN) systems

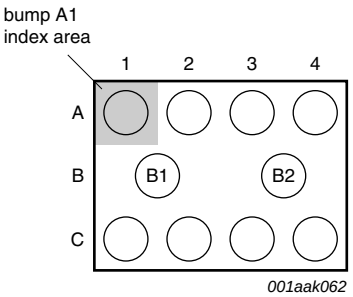
2. Pinning information

2.1 Pinning



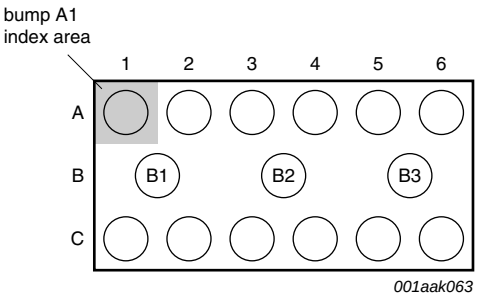
transparent top view,
solder balls facing down

Fig 1. Pin configuration IP3053CX5



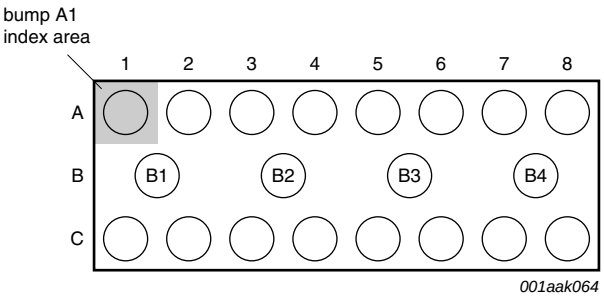
transparent top view,
solder balls facing down

Fig 2. Pin configuration IP3053CX10



transparent top view,
solder balls facing down

Fig 3. Pin configuration IP3053CX15



transparent top view,
solder balls facing down

Fig 4. Pin configuration IP3053CX20

2.2 Pin description

Table 1. Pinning

Pin				Description
IP3053CX5	**IP3053CX10**	**IP3053CX15**	**IP3053CX20**	
A1 and C1	A1 and C1	A1 and C1	A1 and C1	filter channel 1
A2 and C2	A2 and C2	A2 and C2	A2 and C2	filter channel 2
-	A3 and C3	A3 and C3	A3 and C3	filter channel 3
-	A4 and C4	A4 and C4	A4 and C4	filter channel 4
-	-	A5 and C5	A5 and C5	filter channel 5
-	-	A6 and C6	A6 and C6	filter channel 6
-	-	-	A7 and C7	filter channel 7
-	-	-	A8 and C8	filter channel 8
B1	B1 and B2	B1, B2 and B3	B1, B2, B3 and B4	ground

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP3053CX5	WLCSP5	wafer level chip-size package; 5 bumps (2-1-2)	IP3053CX5
IP3053CX10	WLCSP10	wafer level chip-size package; 10 bumps (4-2-4)	IP3053CX10
IP3053CX15	WLCSP15	wafer level chip-size package; 15 bumps (6-3-6)	IP3053CX15
IP3053CX20	WLCSP20	wafer level chip-size package; 20 bumps (8-4-8)	IP3053CX20

4. Functional diagram

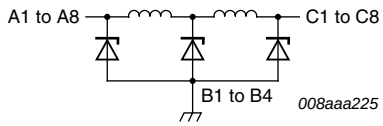


Fig 5. Schematic diagram IP3053CX5; IP3053CX10; IP3053CX15; IP3053CX20

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+5.6	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 level 4; all pins to ground			
		contact discharge	–8	+8	kV
		air discharge	–15	+15	kV
I_{ch}	channel current (DC)	per channel; T_{amb} = 85 °C	-	5	mA
$I_{ch(AC)}$	channel current (AC)	per channel; T_{amb} = 85 °C	-	50	mA
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		–40	+85	°C

6. Characteristics

Table 4. Channel characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance			-	100	-	Ω
$L_{s(ch)}$	channel series inductance			-	35	-	nH
C_{ch}	channel capacitance	$V_{bias(DC)}$ = 0 V; f = 100 kHz	[1]	-	47	-	pF
		$V_{bias(DC)}$ = 2.5 V; f = 100 kHz	[1]	-	30	-	pF
V_{BR}	breakdown voltage	positive clamp; I_{test} = 1 mA		5.8	-	10	V
V_F	forward voltage	negative clamp; I_F = −1 mA		−1.5	-	−0.4	V
I_{LR}	reverse leakage current	per channel; V_I = 3.5 V		-	-	0.1	μA

[1] Guaranteed by design.

Table 5. Frequency characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{il}	insertion loss	R_{gen} = 50 Ω; R_L = 50 Ω; 800 MHz < f < 3 GHz	30	-	-	dB
f_{-3dB}	cut-off frequency	R_{gen} = 50 Ω; R_L = 50 Ω; $V_{bias(DC)}$ = 0 V; α_{il} at 1 MHz − 3 dB	-	150	-	MHz

7. Application information

7.1 Insertion loss

IP3053CX5, IP3053CX10, IP3053CX15 and IP3053CX20 is mainly designed as an EMI and RFI filter for multichannel interfaces.

The setup for measuring insertion loss in a 50 Ω system is shown in Figure 6.

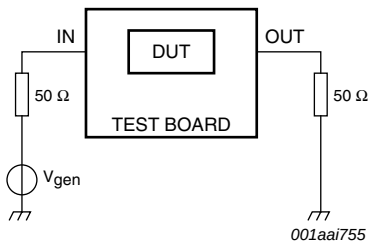
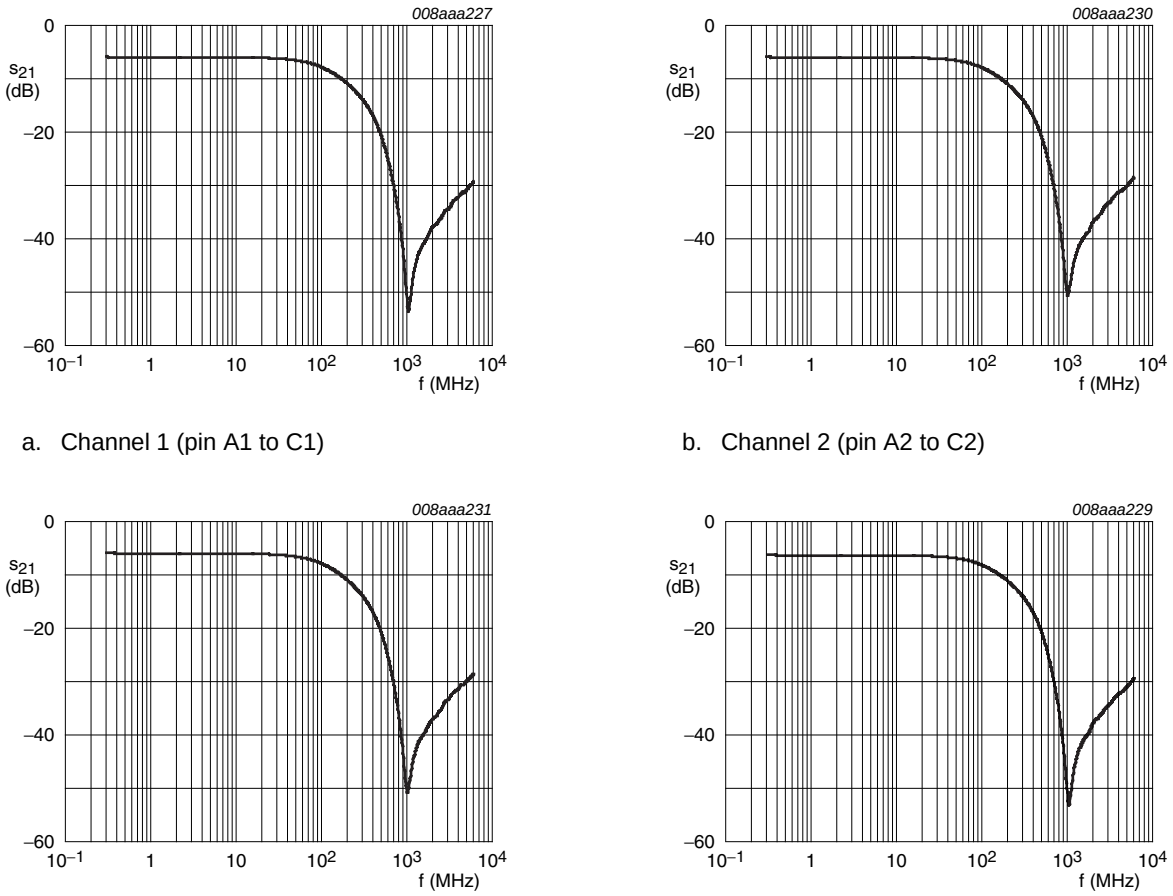


Fig 6. Frequency response measurement configuration

As an example, the measured insertion loss magnitude for all channels of the IP3053CX10 are shown in Figure 7.



a. Channel 1 (pin A1 to C1)

b. Channel 2 (pin A2 to C2)

c. Channel 3 (pin A3 to C3)

d. Channel 4 (pin A4 to C4)

Fig 7. Measured insertion loss magnitude

7.2 Crosstalk

The crosstalk measurement configuration of a typical 50 Ω NetWork Analyzer (NWA) system for evaluation of the IP3053CX5, IP3053CX10, IP3053CX15 and IP3053CX20 is shown in Figure 8.

Four typical examples of crosstalk measurement results of IP3053CX20 are depicted. Unused channels are left open.

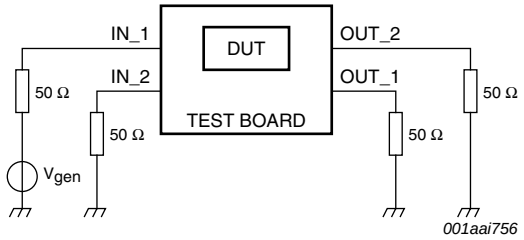
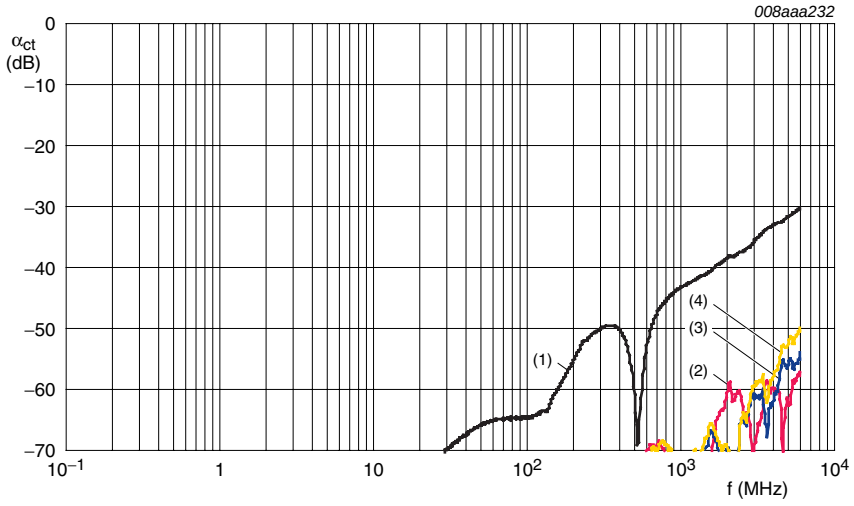


Fig 8. Crosstalk measurement configuration



(1) Channel 1 to 2 (pin A1 to C2).
(2) Channel 1 to 4 (pin A1 to C4).
(3) Channel 1 to 6 (pin A1 to C6).
(4) Channel 1 to 8 (pin A1 to C8).

Fig 9. Measured crosstalk between different channels using the example of IP3053CX20

8. Package outline

WLCSP5: wafer level chip-size package; 5 bumps (2-1-2)

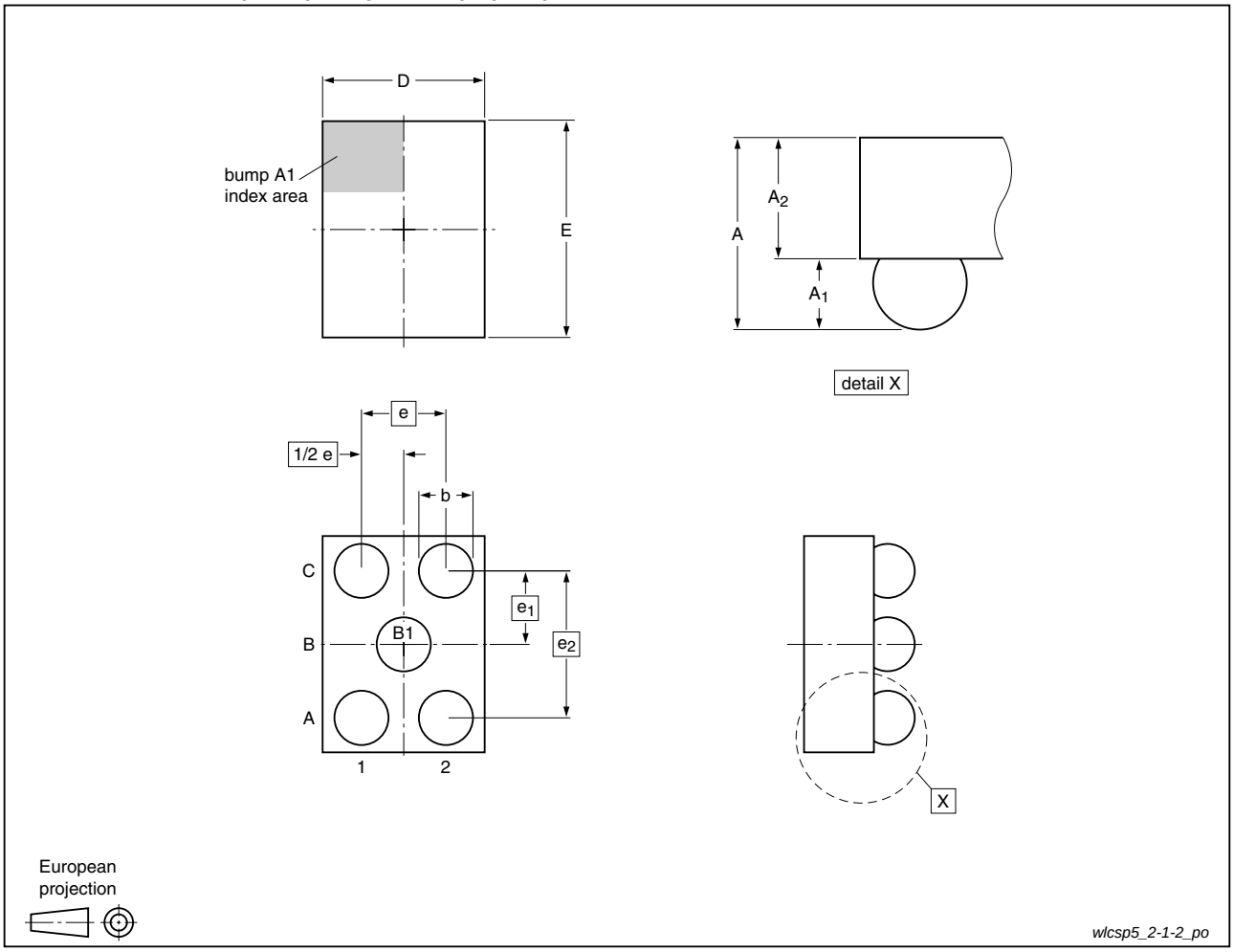


Fig 10. Package outline IP3053CX5 (WLCSP5)

Table 6. Dimensions for Figure 10

Symbol	Min	Typ	Max	Unit
A	0.60	0.65	0.70	mm
A_1	0.22	0.24	0.26	mm
A_2	0.38	0.41	0.44	mm
b	0.27	0.32	0.37	mm
D	0.91	0.96	1.01	mm
E	1.23	1.28	1.33	mm
e	-	0.5	-	mm
e_1	-	0.435	-	mm
e_2	-	0.87	-	mm

WLCSP10: wafer level chip-size package; 10 bumps (4-2-4)

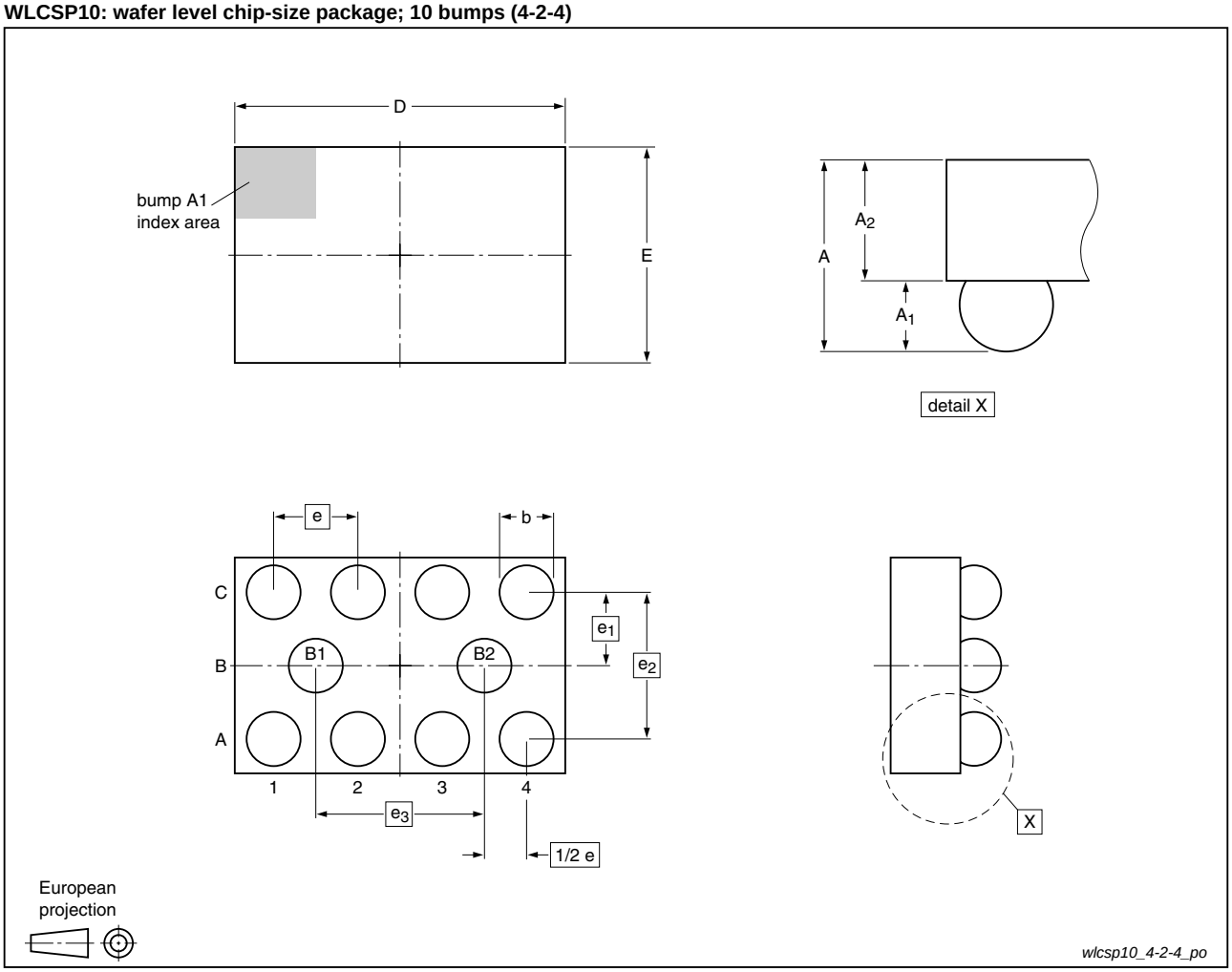


Fig 11. Package outline IP3053CX10 (WLCSP10)

Table 7. Dimensions for Figure 11

Symbol	Min	Typ	Max	Unit
A	0.60	0.65	0.70	mm
A_1	0.22	0.24	0.26	mm
A_2	0.38	0.41	0.44	mm
b	0.27	0.32	0.37	mm
D	1.91	1.96	2.01	mm
E	1.23	1.28	1.33	mm
e	-	0.5	-	mm
e_1	-	0.433	-	mm
e_2	-	0.866	-	mm
e_3	-	1.0	-	mm

WLCSP15: wafer level chip-size package; 15 bumps (6-3-6)

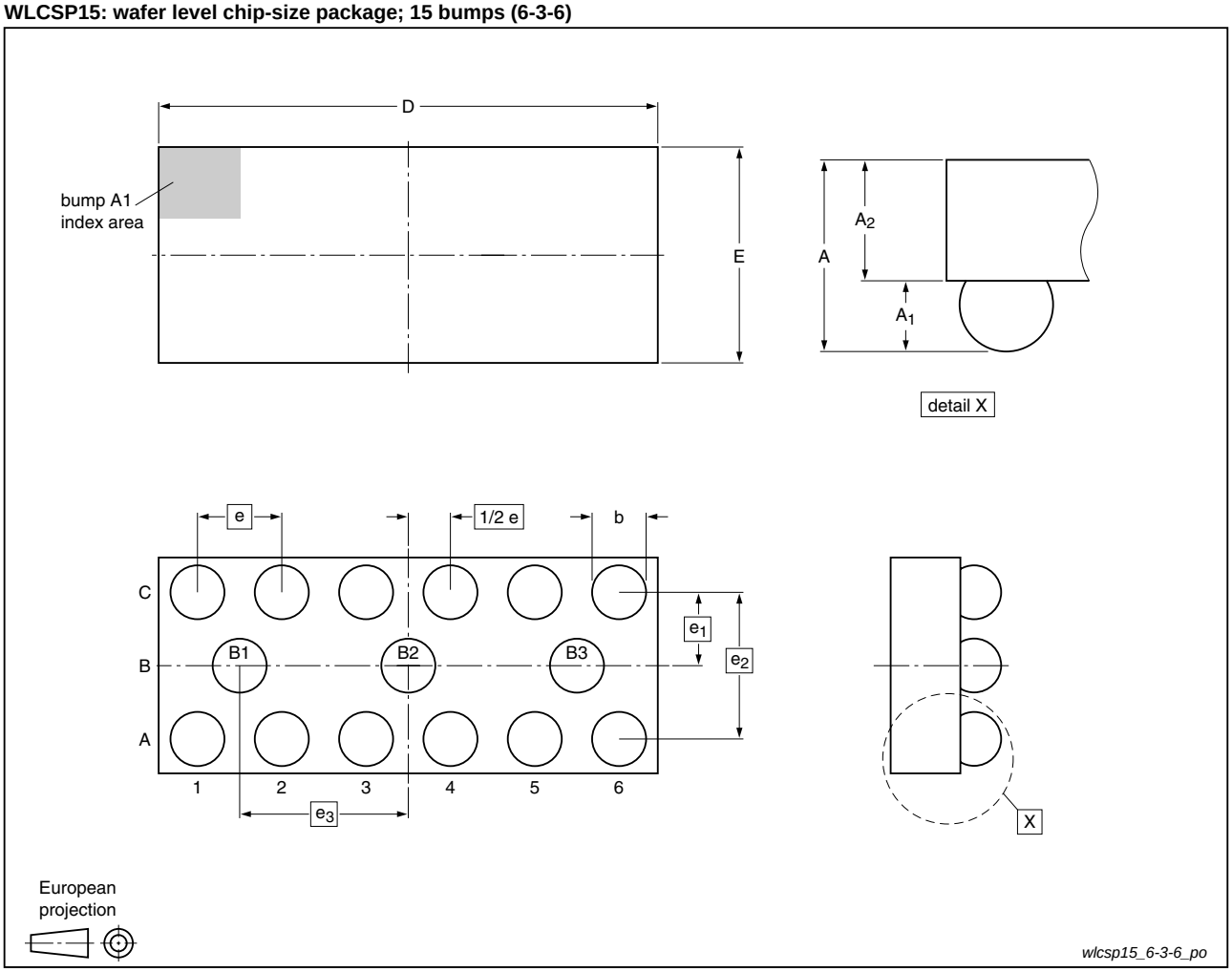


Fig 12. Package outline IP3053CX15 (WLCSP15)

Table 8. Dimensions for Figure 12

Symbol	Min	Typ	Max	Unit
A	0.60	0.65	0.70	mm
A_1	0.22	0.24	0.26	mm
A_2	0.38	0.41	0.44	mm
b	0.27	0.32	0.37	mm
D	2.91	2.96	3.01	mm
E	1.23	1.28	1.33	mm
e	-	0.5	-	mm
e_1	-	0.433	-	mm
e_2	-	0.866	-	mm
e_3	-	1.0	-	mm

WLCSP20: wafer level chip-size package; 20 bumps (8-4-8)

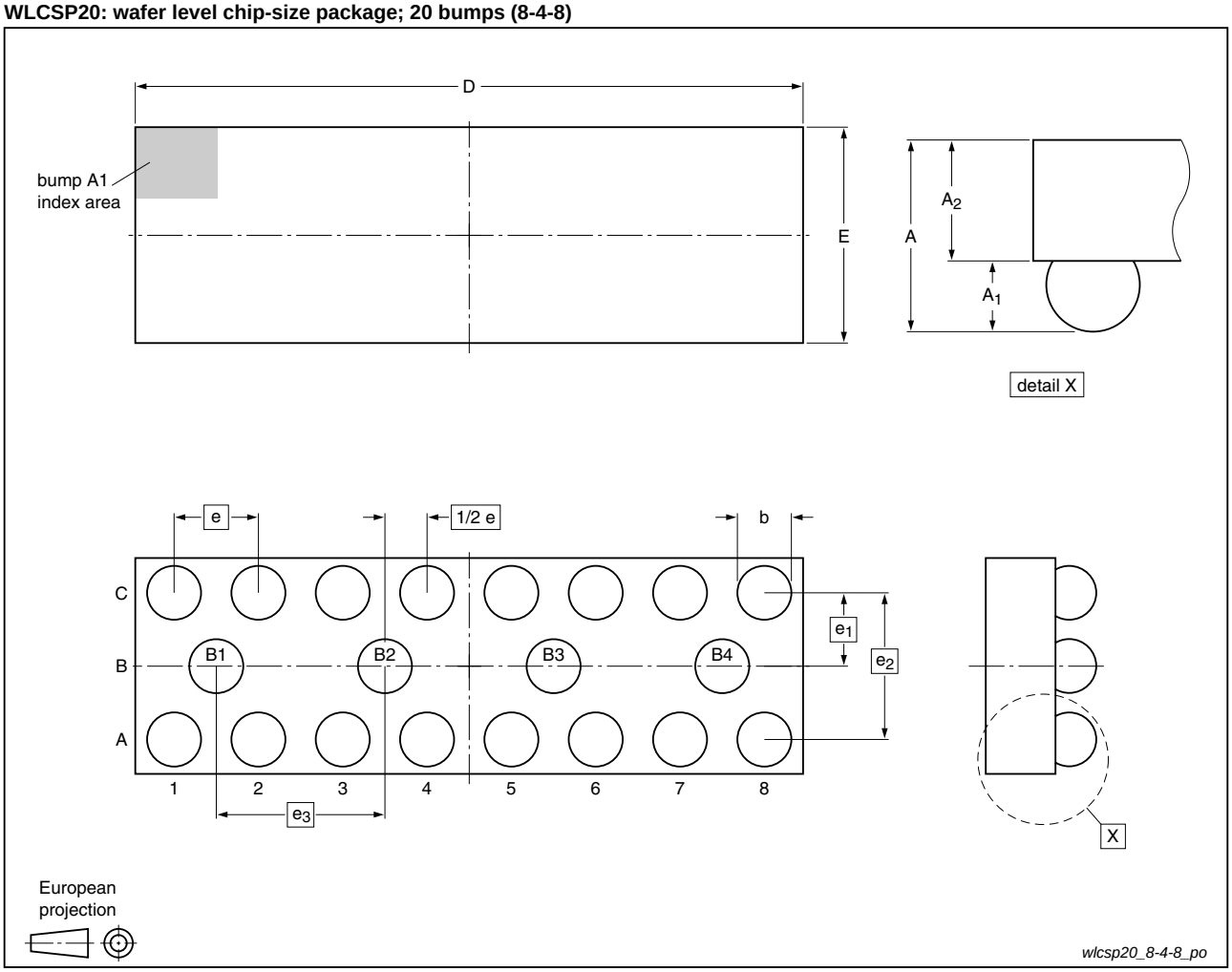


Fig 13. Package outline IP3053CX20 (WLCSP20)

Table 9. Dimensions for Figure 13

Symbol	Min	Typ	Max	Unit
A	0.60	0.65	0.70	mm
A_1	0.22	0.24	0.26	mm
A_2	0.38	0.41	0.44	mm
b	0.27	0.32	0.37	mm
D	3.91	3.96	4.01	mm
E	1.23	1.28	1.33	mm
e	-	0.5	-	mm
e_1	-	0.433	-	mm
e_2	-	0.866	-	mm
e_3	-	1.0	-	mm

9. Design and assembly recommendations

9.1 PCB design guidelines

For optimum performance it is recommended to use a Non-Solder Mask PCB Design (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. For this case, refer to Table 10 for the recommended PCB design parameters.

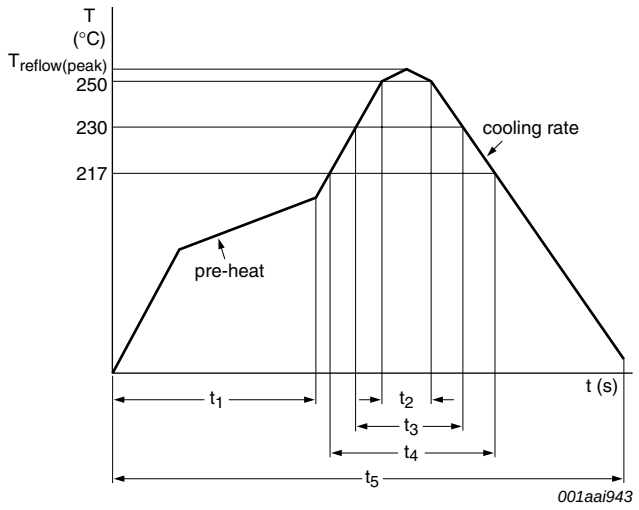
Table 10. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	200 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	370 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi
PCB material	FR4

9.2 PCB assembly guidelines for Pb-free soldering

Table 11. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	330 μm
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %) Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 14



The device is capable of withstanding at least three reflows of this profile.

Fig 14. Pb-free solder reflow profile

Table 12. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		pre-heat	2.5	-	4.0	°C/s

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
HBM	Human Body Model
LAN	Local Area Network
NWA	NetWork Analyzer
PCB	Printed-Circuit Board
PCS	Personal Communication System
PDA	Personal Digital Assistant
RFI	Radio Frequency Interference
RoHS	Restriction of Hazardous Substances
SIM	Subscriber Identity Module
WAN	Wide Area Network
WLCSP	Wafer-Level Chip-Scale Package

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP3053CX5_CX10_CX15_CX20_1	20100503	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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14. Contents

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