

# 74HC40103

## 8-bit synchronous binary down counter

Rev. 03 — 12 November 2004

Product data sheet

### 1. General description

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The 74HC40103 is a high-speed Si-gate CMOS device and are pin compatible with the 40103 of the 4000B series. The 74HC40103 is specified in compliance with JEDEC standard no. 7A.

The 74HC40103 consists of an 8-bit synchronous down counter with a single output which is active when the internal count is zero. The 74HC40103 contains a single 8-bit binary counter and has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count and for presetting the counter either synchronously or asynchronously. All control inputs and the terminal count output ( $\overline{TC}$ ) are active-LOW logic.

In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input ( $\overline{TE}$ ) is HIGH. The terminal count output ( $\overline{TC}$ ) goes LOW when the count reaches zero if  $\overline{TE}$  is LOW, and remains LOW for one full clock period.

When the synchronous preset enable input ( $\overline{PE}$ ) is LOW, data at the jam input (P0 to P7) is clocked into the counter on the next positive-going clock transition regardless of the state of  $\overline{TE}$ . When the asynchronous preset enable input ( $\overline{PL}$ ) is LOW, data at the jam input (P0 to P7) is asynchronously forced into the counter regardless of the state of  $\overline{PE}$ ,  $\overline{TE}$ , or CP. The jam inputs (P0 to P7) represent a single 8-bit binary word.

When the master reset input ( $\overline{MR}$ ) is LOW, the counter is asynchronously cleared to its maximum count (decimal 255) regardless of the state of any other input.

If all control inputs except  $\overline{TE}$  are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 256 clock pulses long.

The 74HC40103 may be cascaded using the  $\overline{TE}$  input and the  $\overline{TC}$  output, in either a synchronous or ripple mode.

**PHILIPS**

## 2. Features

- Cascadable
- Synchronous or asynchronous preset
- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM EIA/JESD22-A114-B exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+80\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ .

## 3. Applications

- Divide-by-n counters
- Programmable timers
- Interrupt timers
- Cycle/program counters.

## 4. Quick reference data

**Table 1: Quick reference data**

$GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHL}$ , $t_{PLH}$	propagation delay CP to $\overline{TC}$	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-	30	-	ns
$f_{max}$	maximum clock frequency	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	-	32	-	MHz
$C_I$	input capacitance		-	3.5	-	pF
$C_{PD}$	power dissipation capacitance	$V_I = GND\text{ to }V_{CC}$	[1] -	24	-	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

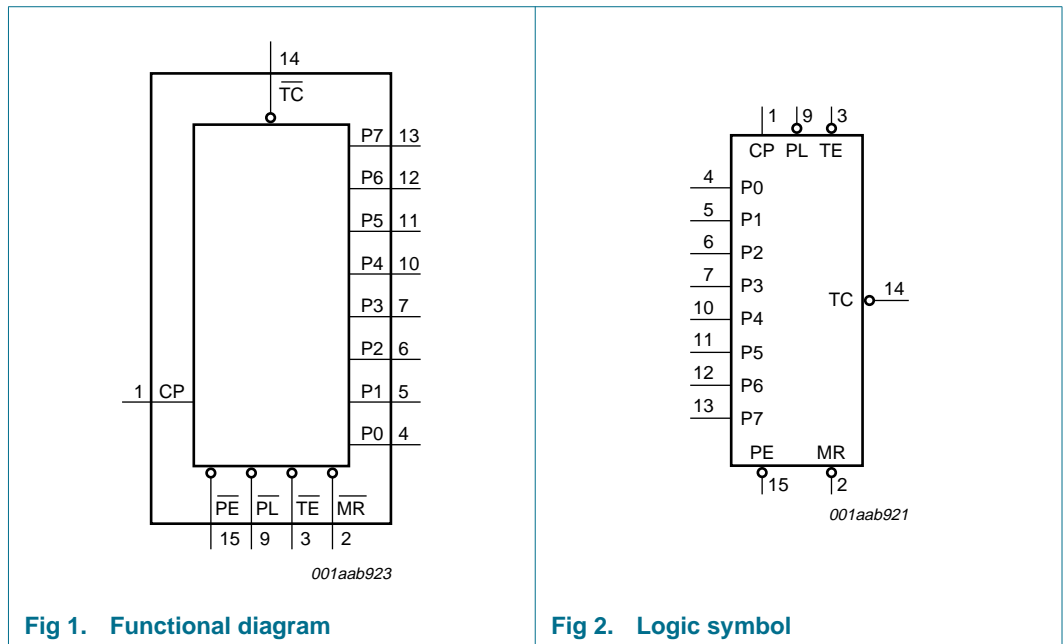
$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## 5. Ordering information

Table 2: Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC40103N	-40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC40103D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC40103DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC40103PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

## 6. Functional diagram



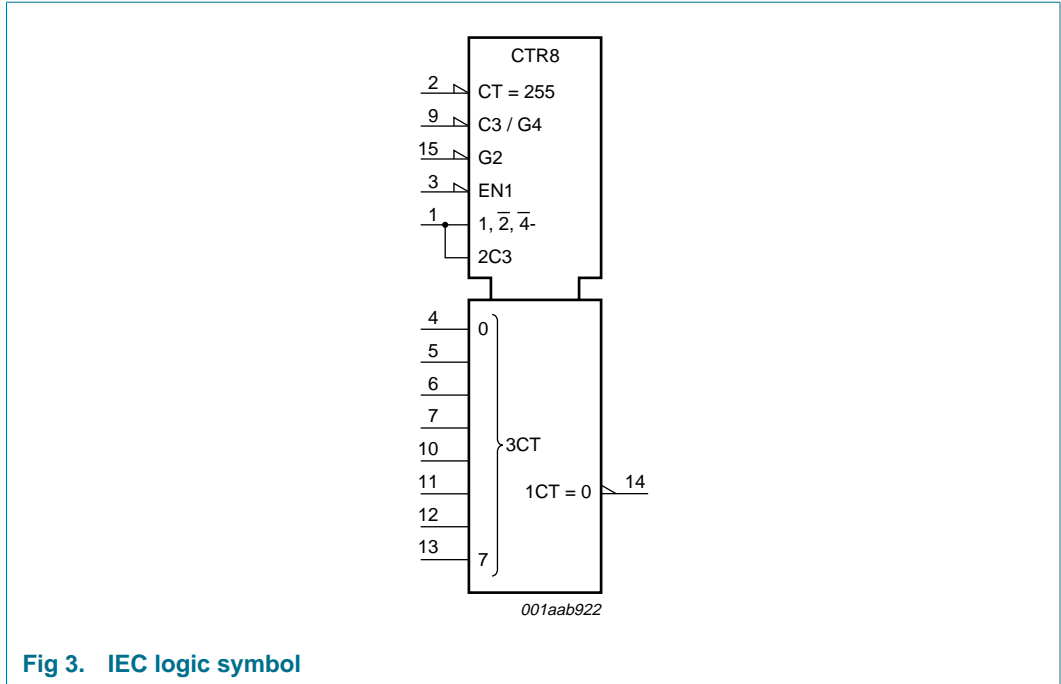


Fig 3. IEC logic symbol

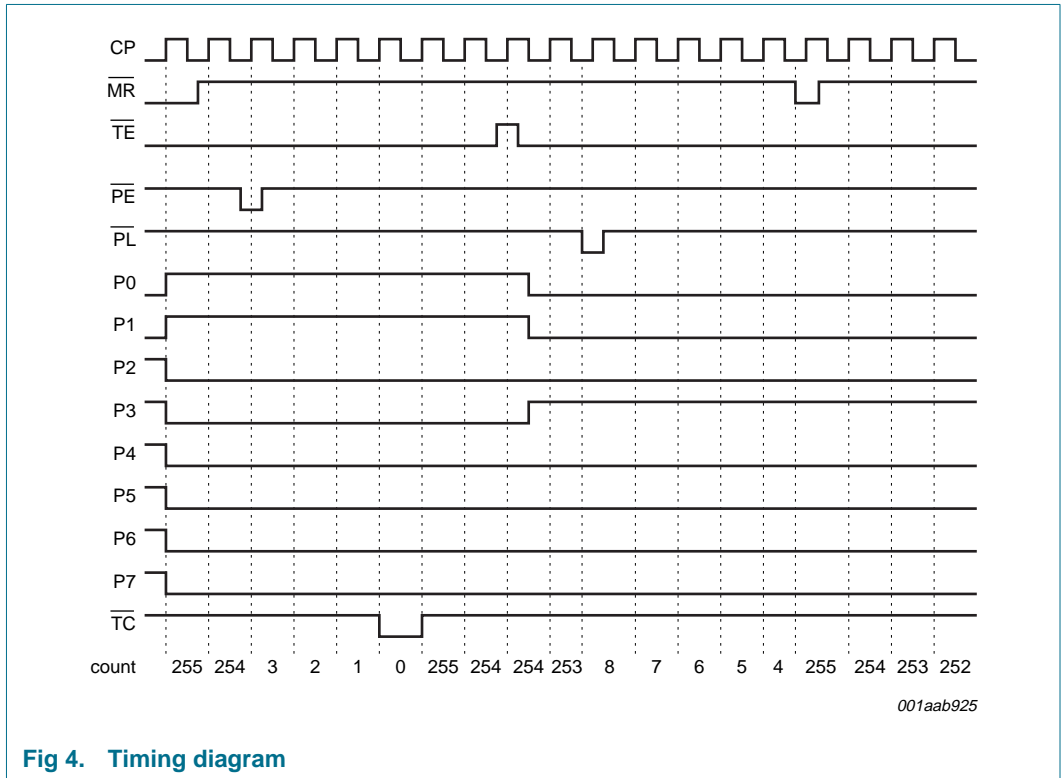
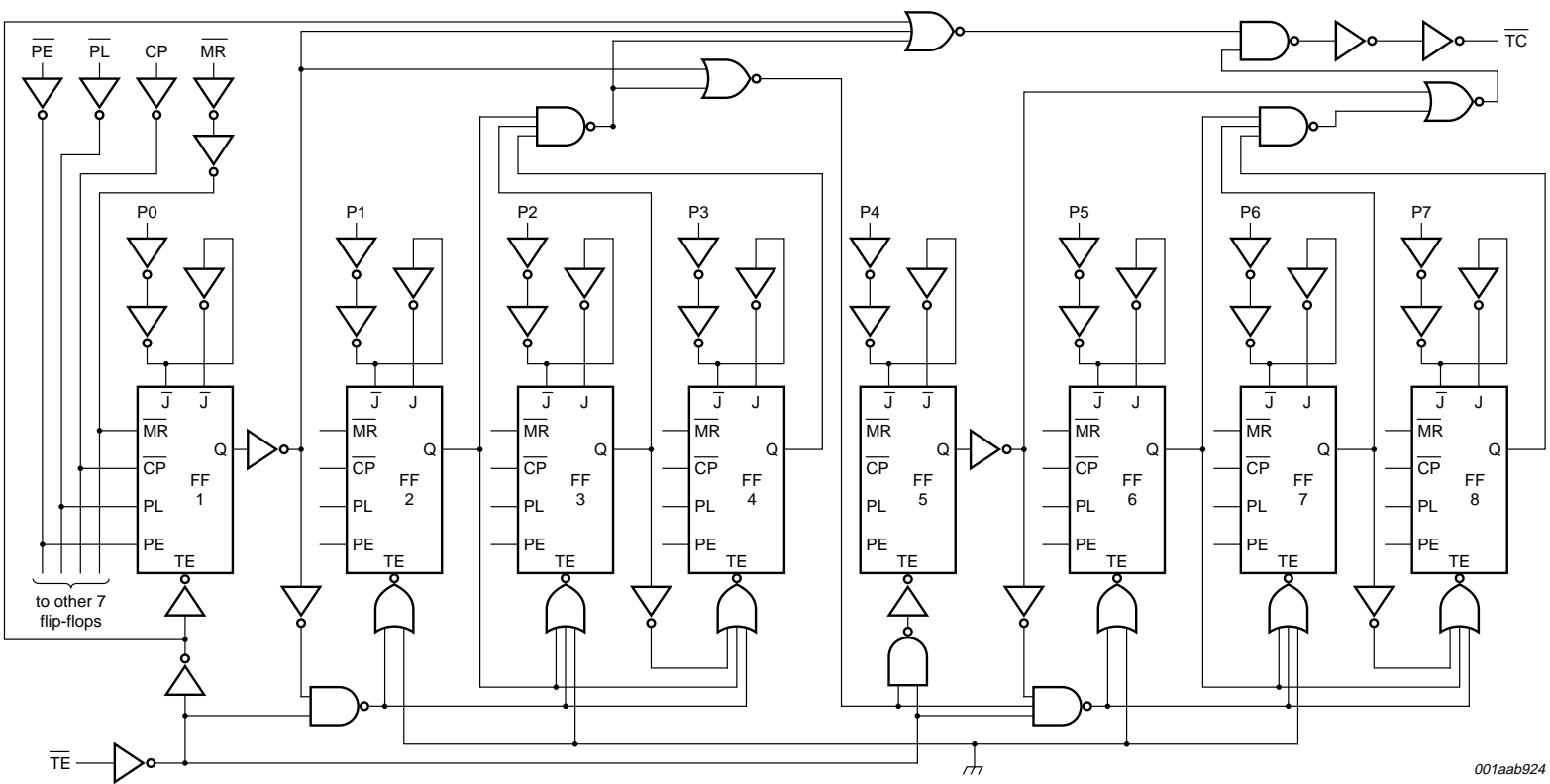


Fig 4. Timing diagram

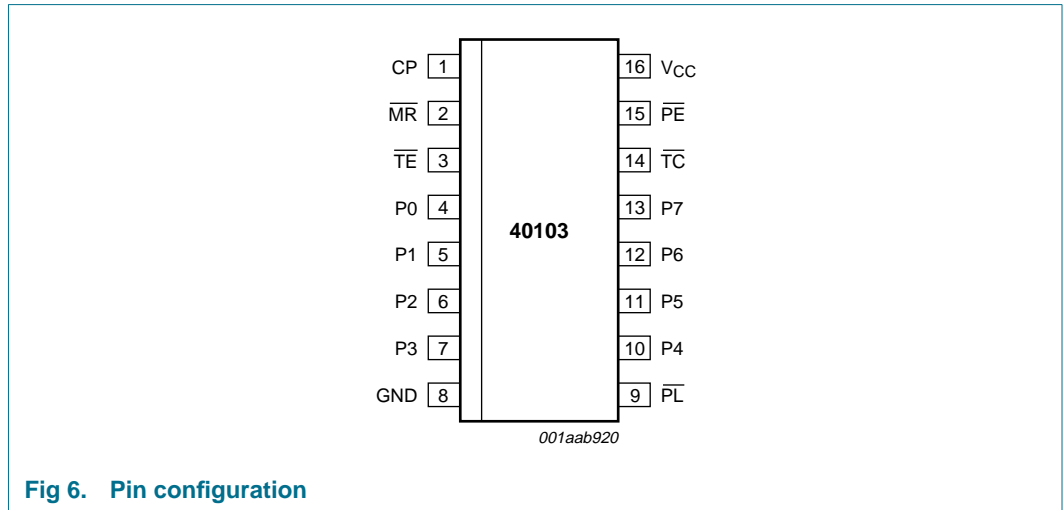


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Fig 5. Logic diagram

## 7. Pinning information

### 7.1 Pinning



### 7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
CP	1	clock input (LOW-to-HIGH, edge-triggered)
$\overline{\text{MR}}$	2	asynchronous master reset input (active LOW)
$\overline{\text{TE}}$	3	terminal enable input (active LOW)
P0	4	jam input 0
P1	5	jam input 1
P2	6	jam input 2
P3	7	jam input 3
GND	8	ground (0 V)
$\overline{\text{PL}}$	9	asynchronous preset enable input (active LOW)
P4	10	jam input 4
P5	11	jam input 5
P6	12	jam input 6
P7	13	jam input 7
$\overline{\text{TC}}$	14	terminal count output (active LOW)
$\overline{\text{PE}}$	15	synchronous preset enable input (active LOW)
V <sub>CC</sub>	16	positive supply voltage

## 8. Functional description

### 8.1 Function table

Table 4: Function table <sup>[1]</sup>

Control inputs				Preset mode	Action <sup>[2]</sup>
MR	PL	PE	TE		
L	X	X	X	asynchronous	clear to maximum count
H	L	X	X	asynchronous	preset asynchronously
		H	X	synchronous	preset on next LOW-to HIGH clock transition
	H	L	L	synchronous	count down
		H	H	synchronous	inhibit counter

[1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care.

[2] Clock connected to CP.  
Synchronous operation: changes occur on the LOW-to-HIGH CP transition.  
Jam inputs: MSD = P7, LSD = P0.

## 9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_O$	output source or sink current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	$\pm 50$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation				
	DIP16 package		<sup>[1]</sup> -	750	mW
	SO16, SSOP16 and TSSOP16 packages		<sup>[2]</sup> -	500	mW

[1] Above 70 °C:  $P_{tot}$  derates linearly with 12 mW/K.

[2] Above 70 °C:  $P_{tot}$  derates linearly with 8 mW/K.

## 10. Recommended operating conditions

**Table 6: Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	6.0	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$t_r, t_f$	input rise and fall times	$V_{CC} = 2.0\text{ V}$	-	-	1000	ns
		$V_{CC} = 4.5\text{ V}$	-	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	-	-	400	ns
$T_{amb}$	ambient temperature		-40	-	+125	°C

## 11. Static characteristics

**Table 7: Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = 25\text{ °C}</math></b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	V
		$I_O = -20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	5.9	6.0	-	V
		$I_O = -4\text{ mA}; V_{CC} = 4.5\text{ V}$	3.98	4.32	-	V
		$I_O = -5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	5.48	5.81	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.1	V
		$I_O = 20\text{ }\mu\text{A}; V_{CC} = 6.0\text{ V}$	-	0	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.15	0.26	V
		$I_O = 5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	-	0.16	0.26	V
$I_{LI}$	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	$\pm 0.1$	$\mu\text{A}$
$I_{CC}$	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0\text{ A}; V_{CC} = 6.0\text{ V}$	-	-	8.0	$\mu\text{A}$
$C_I$	input capacitance		-	3.5	-	pF



**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	V
		V <sub>CC</sub> = 4.5 V	3.15	-	-	V
		V <sub>CC</sub> = 6.0 V	4.2	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 4.5 V	3.84	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	-	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 4.5 V	-	-	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±1.0	μA
		I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	80	μA
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	V
		V <sub>CC</sub> = 4.5 V	3.15	-	-	V
		V <sub>CC</sub> = 6.0 V	4.2	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	-	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 4.5 V	3.7	-	-	V
I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V		5.2	-	-	V	

**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	-	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 4.5 V	-	-	0.4	V
	I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	-	0.4	V	
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	160	μA

## 12. Dynamic characteristics

**Table 8: Dynamic characteristics**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF; see [Figure 13](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>T<sub>amb</sub> = 25 °C</b>							
t <sub>PHL</sub> , t <sub>PLH</sub>	propagation delay CP to $\overline{TC}$	see <a href="#">Figure 7</a>					
		V <sub>CC</sub> = 2.0 V	-	96	300	ns	
		V <sub>CC</sub> = 4.5 V	-	35	60	ns	
		V <sub>CC</sub> = 6.0 V	-	28	51	ns	
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF	-	30	-	ns	
	propagation delay $\overline{TE}$ to $\overline{TC}$	see <a href="#">Figure 8</a>					
		V <sub>CC</sub> = 2.0 V	-	50	175	ns	
		V <sub>CC</sub> = 4.5 V	-	18	35	ns	
	propagation delay $\overline{PL}$ to $\overline{TC}$	see <a href="#">Figure 9</a>					
		V <sub>CC</sub> = 2.0 V	-	102	315	ns	
		V <sub>CC</sub> = 4.5 V	-	37	63	ns	
	t <sub>PHL</sub>	propagation delay $\overline{MR}$ to $\overline{TC}$	see <a href="#">Figure 9</a>				
			V <sub>CC</sub> = 2.0 V	-	83	275	ns
V <sub>CC</sub> = 4.5 V			-	30	55	ns	
t <sub>THL</sub> , t <sub>TLH</sub>	output transition time	see <a href="#">Figure 8</a>					
		V <sub>CC</sub> = 2.0 V	-	19	75	ns	
		V <sub>CC</sub> = 4.5 V	-	7	15	ns	
		V <sub>CC</sub> = 6.0 V	-	6	13	ns	

**Table 8: Dynamic characteristics ...continued**  
*GND = 0 V;  $t_r = t_f = 6 \text{ ns}$ ;  $C_L = 50 \text{ pF}$ ; see [Figure 13](#).*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$t_{W}$	CP clock pulse width HIGH or LOW	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0 \text{ V}$	165	22	-	ns	
		$V_{CC} = 4.5 \text{ V}$	33	8	-	ns	
			$V_{CC} = 6.0 \text{ V}$	28	6	-	ns
	MR master reset pulse width LOW	see <a href="#">Figure 9</a>					
		$V_{CC} = 2.0 \text{ V}$	125	39	-	ns	
		$V_{CC} = 4.5 \text{ V}$	25	14	-	ns	
			$V_{CC} = 6.0 \text{ V}$	21	11	-	ns
	PL preset enable pulse width LOW	see <a href="#">Figure 9</a>					
$V_{CC} = 2.0 \text{ V}$		125	33	-	ns		
$V_{CC} = 4.5 \text{ V}$		25	12	-	ns		
		$V_{CC} = 6.0 \text{ V}$	21	10	-	ns	
$t_{rem}$	removal time MR to CP, PL to CP	see <a href="#">Figure 10</a>					
		$V_{CC} = 2.0 \text{ V}$	50	14	-	ns	
		$V_{CC} = 4.5 \text{ V}$	10	5	-	ns	
		$V_{CC} = 6.0 \text{ V}$	9	4	-	ns	
$t_{su}$	set-up time PE to CP	see <a href="#">Figure 11</a>					
		$V_{CC} = 2.0 \text{ V}$	75	22	-	ns	
		$V_{CC} = 4.5 \text{ V}$	15	8	-	ns	
			$V_{CC} = 6.0 \text{ V}$	13	6	-	ns
	set-up time TE to CP	see <a href="#">Figure 12</a>					
		$V_{CC} = 2.0 \text{ V}$	150	44	-	ns	
		$V_{CC} = 4.5 \text{ V}$	30	16	-	ns	
			$V_{CC} = 6.0 \text{ V}$	26	13	-	ns
	set-up time Pn to CP	see <a href="#">Figure 11</a>					
		$V_{CC} = 2.0 \text{ V}$	75	22	-	ns	
		$V_{CC} = 4.5 \text{ V}$	15	8	-	ns	
			$V_{CC} = 6.0 \text{ V}$	13	6	-	ns
$t_h$	hold time PE to CP	see <a href="#">Figure 11</a>					
		$V_{CC} = 2.0 \text{ V}$	0	-14	-	ns	
		$V_{CC} = 4.5 \text{ V}$	0	-5	-	ns	
			$V_{CC} = 6.0 \text{ V}$	0	-4	-	ns
	hold time TE to CP	see <a href="#">Figure 12</a>					
		$V_{CC} = 2.0 \text{ V}$	0	-30	-	ns	
		$V_{CC} = 4.5 \text{ V}$	0	-11	-	ns	
			$V_{CC} = 6.0 \text{ V}$	0	-9	-	ns
	hold time Pn to CP	see <a href="#">Figure 11</a>					
$V_{CC} = 2.0 \text{ V}$		0	-17	-	ns		
$V_{CC} = 4.5 \text{ V}$		0	-6	-	ns		
		$V_{CC} = 6.0 \text{ V}$	0	-5	-	ns	

**Table 8: Dynamic characteristics ...continued**  
 $GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$ ; see [Figure 13](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$f_{\max}$	maximum clock frequency	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0\text{ V}$	3.0	10	-	MHz	
		$V_{CC} = 4.5\text{ V}$	15	29	-	MHz	
		$V_{CC} = 6.0\text{ V}$	18	35	-	MHz	
		$V_{CC} = 5.0\text{ V}$ ; $C_L = 15\text{ pF}$	-	32	-	MHz	
$C_{PD}$	power dissipation capacitance	$V_I = GND$ to $V_{CC}$	[1] -	24	-	pF	
<b><math>T_{\text{amb}} = -40\text{ °C}</math> to <math>+85\text{ °C}</math></b>							
$t_{PHL}$ , $t_{PLH}$	propagation delay CP to $\overline{TC}$	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0\text{ V}$	-	-	375	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	75	ns	
			$V_{CC} = 6.0\text{ V}$	-	-	64	ns
	propagation delay $\overline{TE}$ to $\overline{TC}$	see <a href="#">Figure 8</a>					
		$V_{CC} = 2.0\text{ V}$	-	-	220	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	44	ns	
			$V_{CC} = 6.0\text{ V}$	-	-	37	ns
	propagation delay $\overline{PL}$ to $\overline{TC}$	see <a href="#">Figure 9</a>					
		$V_{CC} = 2.0\text{ V}$	-	-	395	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	79	ns	
			$V_{CC} = 6.0\text{ V}$	-	-	40	ns
$t_{PHL}$	propagation delay $\overline{MR}$ to $\overline{TC}$	see <a href="#">Figure 9</a>					
		$V_{CC} = 2.0\text{ V}$	-	-	345	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	69	ns	
		$V_{CC} = 6.0\text{ V}$	-	-	59	ns	
$t_{THL}$ , $t_{TLH}$	output transition time	see <a href="#">Figure 8</a>					
		$V_{CC} = 2.0\text{ V}$	-	-	95	ns	
		$V_{CC} = 4.5\text{ V}$	-	-	19	ns	
		$V_{CC} = 6.0\text{ V}$	-	-	16	ns	
$t_w$	CP clock pulse width HIGH or LOW	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0\text{ V}$	205	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	41	-	-	ns	
			$V_{CC} = 6.0\text{ V}$	35	-	-	ns
	$\overline{MR}$ master reset pulse width LOW	see <a href="#">Figure 9</a>					
		$V_{CC} = 2.0\text{ V}$	155	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	31	-	-	ns	
			$V_{CC} = 6.0\text{ V}$	26	-	-	ns
	$\overline{PL}$ preset enable pulse width LOW	see <a href="#">Figure 9</a>					
		$V_{CC} = 2.0\text{ V}$	155	-	-	ns	
		$V_{CC} = 4.5\text{ V}$	31	-	-	ns	
			$V_{CC} = 6.0\text{ V}$	26	-	-	ns

**Table 8: Dynamic characteristics ...continued**  
*GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF; see [Figure 13](#).*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$t_{rem}$	removal time $\overline{MR}$ to CP, $\overline{PL}$ to CP	see <a href="#">Figure 10</a>					
		$V_{CC} = 2.0$ V	65	-	-	ns	
		$V_{CC} = 4.5$ V	13	-	-	ns	
		$V_{CC} = 6.0$ V	11	-	-	ns	
$t_{su}$	set-up time $\overline{PE}$ to CP	see <a href="#">Figure 11</a>					
		$V_{CC} = 2.0$ V	95	-	-	ns	
		$V_{CC} = 4.5$ V	19	-	-	ns	
			$V_{CC} = 6.0$ V	16	-	-	ns
	set-up time $\overline{TE}$ to CP	see <a href="#">Figure 12</a>					
		$V_{CC} = 2.0$ V	190	-	-	ns	
		$V_{CC} = 4.5$ V	38	-	-	ns	
			$V_{CC} = 6.0$ V	33	-	-	ns
	set-up time Pn to CP	see <a href="#">Figure 11</a>					
		$V_{CC} = 2.0$ V	95	-	-	ns	
		$V_{CC} = 4.5$ V	19	-	-	ns	
			$V_{CC} = 6.0$ V	16	-	-	ns
$t_h$	hold time $\overline{PE}$ to CP	see <a href="#">Figure 11</a>					
		$V_{CC} = 2.0$ V	0	-	-	ns	
		$V_{CC} = 4.5$ V	0	-	-	ns	
			$V_{CC} = 6.0$ V	0	-	-	ns
	hold time $\overline{TE}$ to CP	see <a href="#">Figure 12</a>					
		$V_{CC} = 2.0$ V	0	-	-	ns	
		$V_{CC} = 4.5$ V	0	-	-	ns	
			$V_{CC} = 6.0$ V	0	-	-	ns
	hold time Pn to CP	see <a href="#">Figure 11</a>					
		$V_{CC} = 2.0$ V	0	-	-	ns	
		$V_{CC} = 4.5$ V	0	-	-	ns	
			$V_{CC} = 6.0$ V	0	-	-	ns
$f_{max}$	maximum clock frequency	see <a href="#">Figure 7</a>					
		$V_{CC} = 2.0$ V	2.4	-	-	MHz	
		$V_{CC} = 4.5$ V	12	-	-	MHz	
		$V_{CC} = 6.0$ V	14	-	-	MHz	

**Table 8: Dynamic characteristics ...continued**  
 $GND = 0\text{ V}$ ;  $t_r = t_f = 6\text{ ns}$ ;  $C_L = 50\text{ pF}$ ; see [Figure 13](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b><math>T_{\text{amb}} = -40\text{ °C to }+125\text{ °C}</math></b>							
$t_{\text{PHL}}/t_{\text{PLH}}$	propagation delay CP to $\overline{\text{TC}}$	see <a href="#">Figure 7</a>					
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	450	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	90	ns	
			$V_{\text{CC}} = 6.0\text{ V}$	-	-	77	ns
	propagation delay $\overline{\text{TE}}$ to $\overline{\text{TC}}$	see <a href="#">Figure 8</a>					
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	265	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	53	ns	
			$V_{\text{CC}} = 6.0\text{ V}$	-	-	45	ns
	propagation delay $\overline{\text{PL}}$ to $\overline{\text{TC}}$	see <a href="#">Figure 9</a>					
$V_{\text{CC}} = 2.0\text{ V}$		-	-	475	ns		
$V_{\text{CC}} = 4.5\text{ V}$		-	-	95	ns		
		$V_{\text{CC}} = 6.0\text{ V}$	-	-	81	ns	
$t_{\text{PHL}}$	propagation delay $\overline{\text{MR}}$ to $\overline{\text{TC}}$	see <a href="#">Figure 9</a>					
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	415	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	83	ns	
		$V_{\text{CC}} = 6.0\text{ V}$	-	-	71	ns	
$t_{\text{THL}}/t_{\text{TLH}}$	output transition time	see <a href="#">Figure 8</a>					
		$V_{\text{CC}} = 2.0\text{ V}$	-	-	110	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	-	-	22	ns	
		$V_{\text{CC}} = 6.0\text{ V}$	-	-	19	ns	
$t_{\text{w}}$	CP clock pulse width HIGH or LOW	see <a href="#">Figure 7</a>					
		$V_{\text{CC}} = 2.0\text{ V}$	250	-	-	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	50	-	-	ns	
			$V_{\text{CC}} = 6.0\text{ V}$	43	-	-	ns
	$\overline{\text{MR}}$ master reset pulse width LOW	see <a href="#">Figure 9</a>					
		$V_{\text{CC}} = 2.0\text{ V}$	190	-	-	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	38	-	-	ns	
			$V_{\text{CC}} = 6.0\text{ V}$	32	-	-	ns
	$\overline{\text{PL}}$ preset enable pulse width LOW	see <a href="#">Figure 9</a>					
$V_{\text{CC}} = 2.0\text{ V}$		190	-	-	ns		
$V_{\text{CC}} = 4.5\text{ V}$		38	-	-	ns		
		$V_{\text{CC}} = 6.0\text{ V}$	32	-	-	ns	
$t_{\text{rem}}$	removal time $\overline{\text{MR}}$ to CP, $\overline{\text{PL}}$ to CP	see <a href="#">Figure 10</a>					
		$V_{\text{CC}} = 2.0\text{ V}$	75	-	-	ns	
		$V_{\text{CC}} = 4.5\text{ V}$	15	-	-	ns	
		$V_{\text{CC}} = 6.0\text{ V}$	13	-	-	ns	

**Table 8: Dynamic characteristics ...continued**  
*GND = 0 V;  $t_r = t_f = 6 \text{ ns}$ ;  $C_L = 50 \text{ pF}$ ; see [Figure 13](#).*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su}$	set-up time $\overline{PE}$ to CP	see <a href="#">Figure 11</a>				
		$V_{CC} = 2.0 \text{ V}$	110	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	22	-	-	ns
	set-up time $\overline{TE}$ to CP	$V_{CC} = 6.0 \text{ V}$	19	-	-	ns
		see <a href="#">Figure 12</a>				
		$V_{CC} = 2.0 \text{ V}$	225	-	-	ns
	set-up time Pn to CP	$V_{CC} = 4.5 \text{ V}$	45	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	38	-	-	ns
		see <a href="#">Figure 11</a>				
$t_h$	hold time $\overline{PE}$ to CP	$V_{CC} = 2.0 \text{ V}$	110	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	22	-	-	ns
		$V_{CC} = 6.0 \text{ V}$	19	-	-	ns
	hold time $\overline{TE}$ to CP	see <a href="#">Figure 11</a>				
		$V_{CC} = 2.0 \text{ V}$	0	-	-	ns
		$V_{CC} = 4.5 \text{ V}$	0	-	-	ns
	hold time Pn to CP	$V_{CC} = 6.0 \text{ V}$	0	-	-	ns
		see <a href="#">Figure 12</a>				
		$V_{CC} = 2.0 \text{ V}$	0	-	-	ns
hold time Pn to CP	$V_{CC} = 4.5 \text{ V}$	0	-	-	ns	
	$V_{CC} = 6.0 \text{ V}$	0	-	-	ns	
	see <a href="#">Figure 11</a>					
$f_{max}$	maximum clock frequency	see <a href="#">Figure 7</a>				
		$V_{CC} = 2.0 \text{ V}$	2.0	-	-	MHz
		$V_{CC} = 4.5 \text{ V}$	10	-	-	MHz
		$V_{CC} = 6.0 \text{ V}$	12	-	-	MHz

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

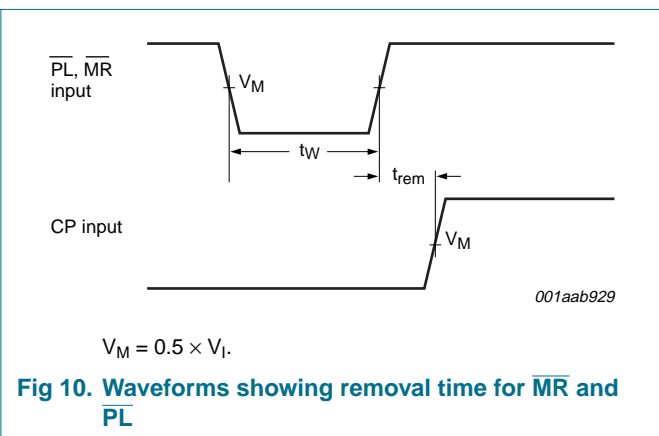
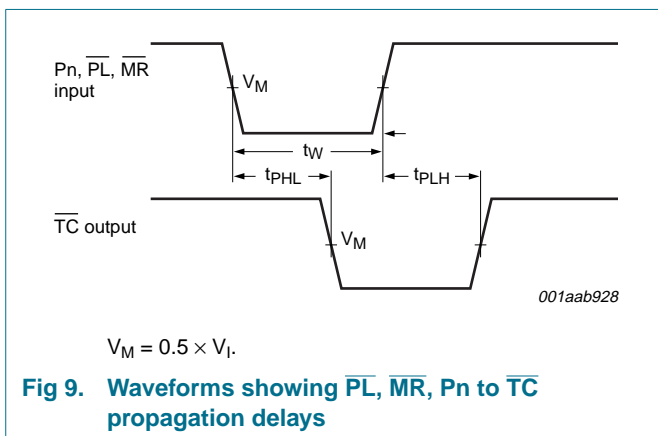
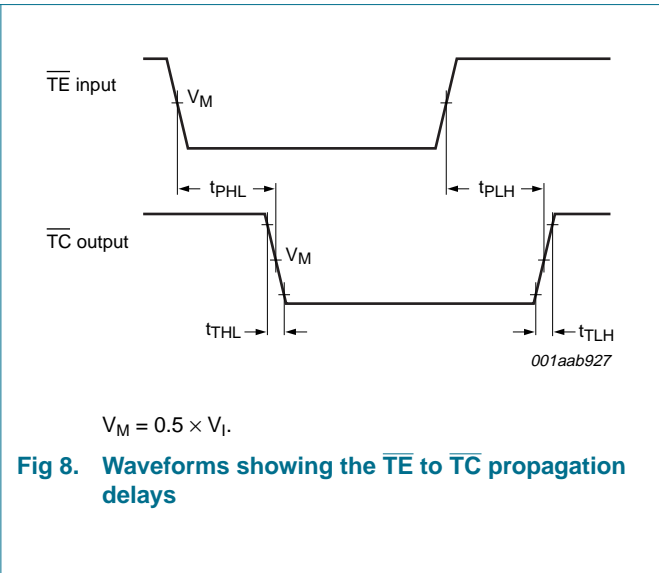
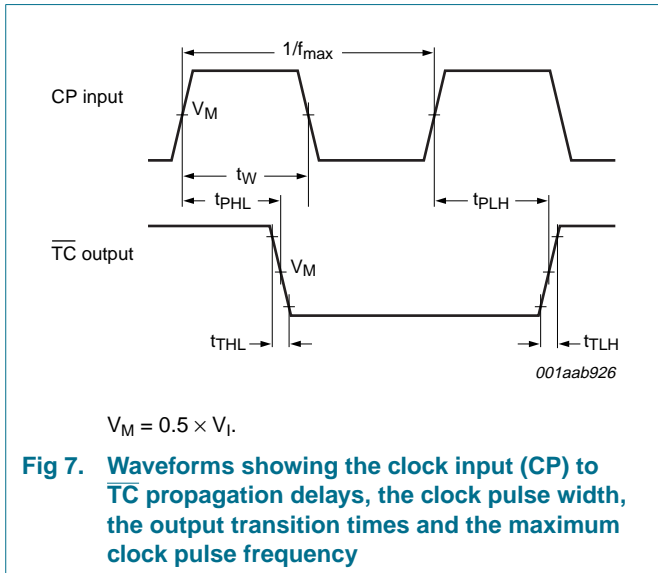
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

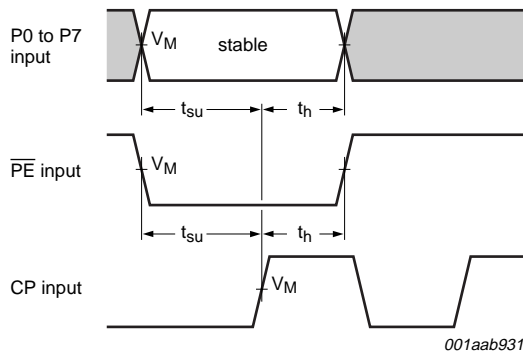
$N$  = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

13. Waveforms

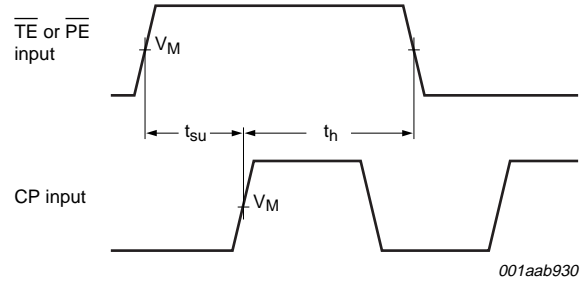






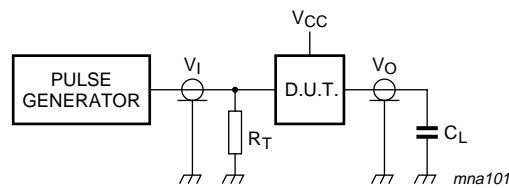
The shaded areas indicate when the input is permitted to change for predictable output performance.  
 $V_M = 0.5 \times V_I$ .

Fig 11. Waveforms showing hold and set-up times for Pn, PE to CP



$V_M = 0.5 \times V_I$ .

Fig 12. Waveforms showing hold and set-up times for MR or PE to CP



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

Fig 13. Load circuitry for switching times

Table 9: Test data

Supply	Input	Load
$V_{CC}$	$V_I$ $t_r, t_f$	$C_L$
2.0 V	$V_{CC}$ 6 ns	50 pF
4.5 V	$V_{CC}$ 6 ns	50 pF
6.0 V	$V_{CC}$ 6 ns	50 pF
5.0 V	$V_{CC}$ 6 ns	15 pF

14. Application information

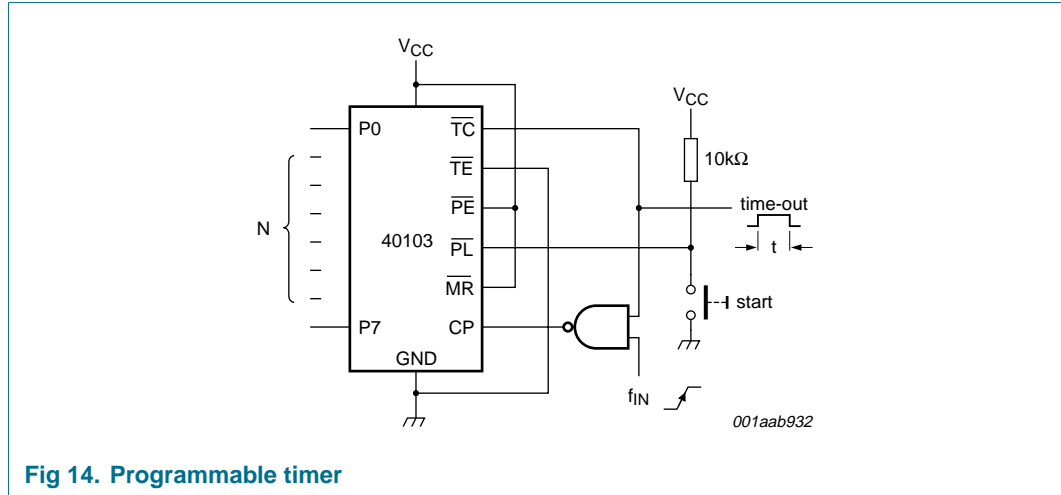


Fig 14. Programmable timer

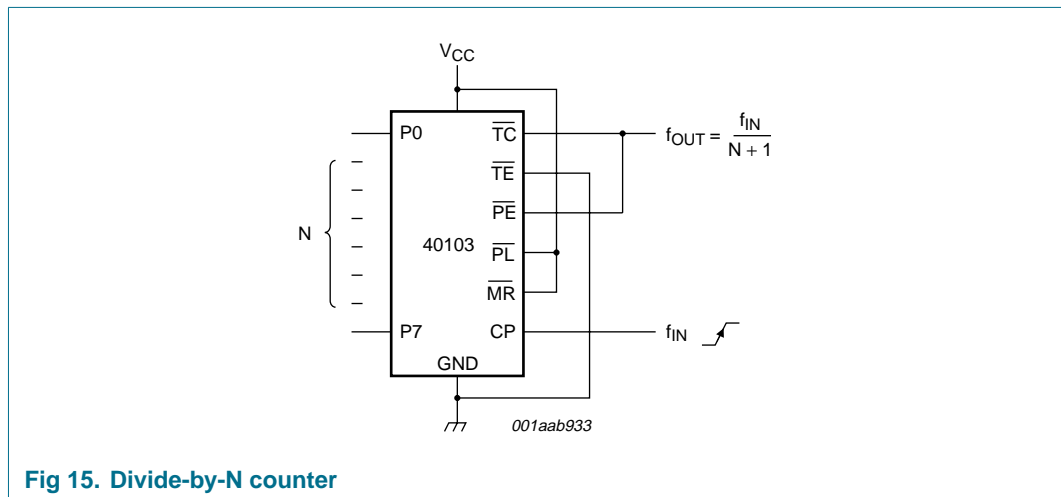


Fig 15. Divide-by-N counter

15. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

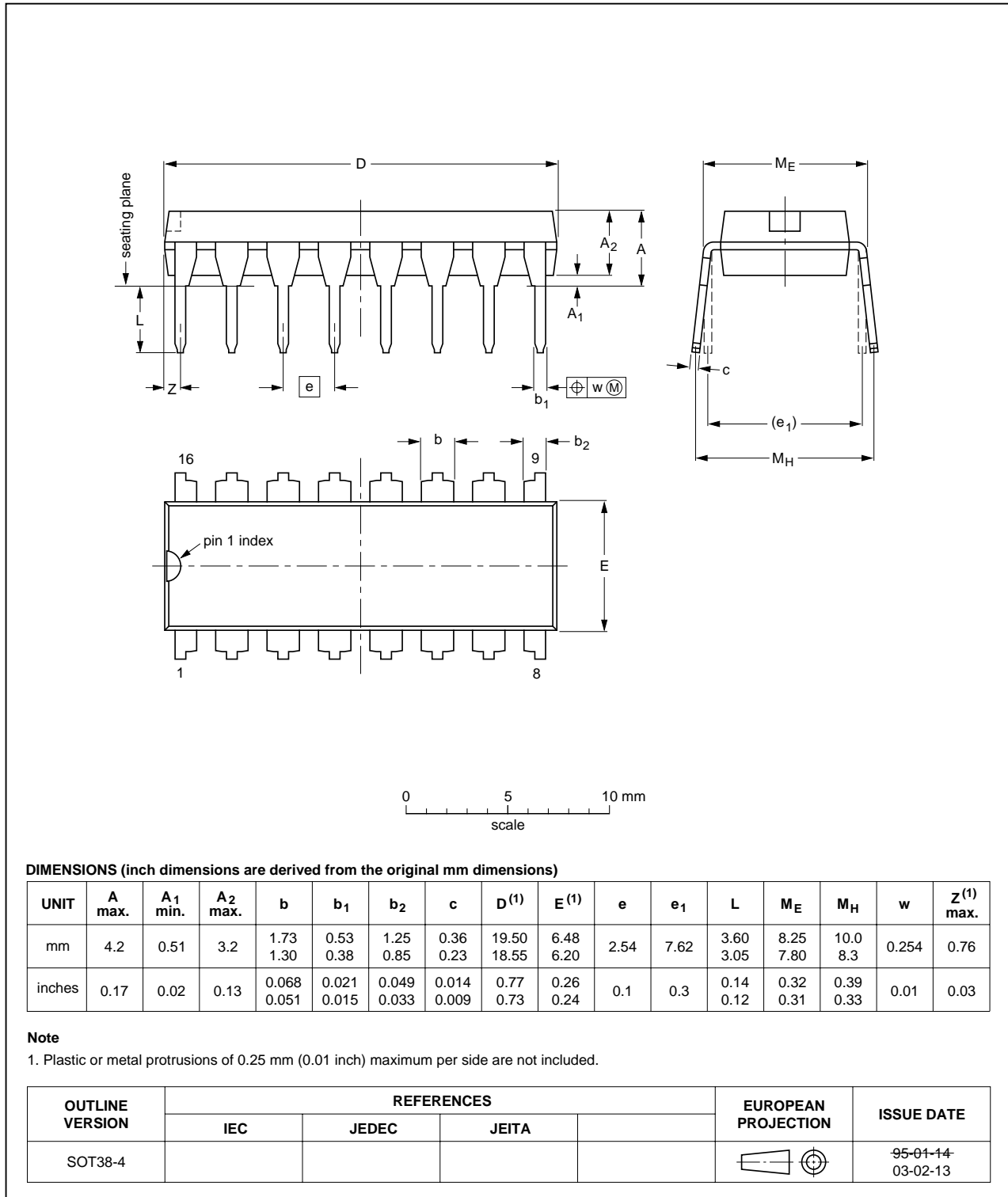


Fig 16. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

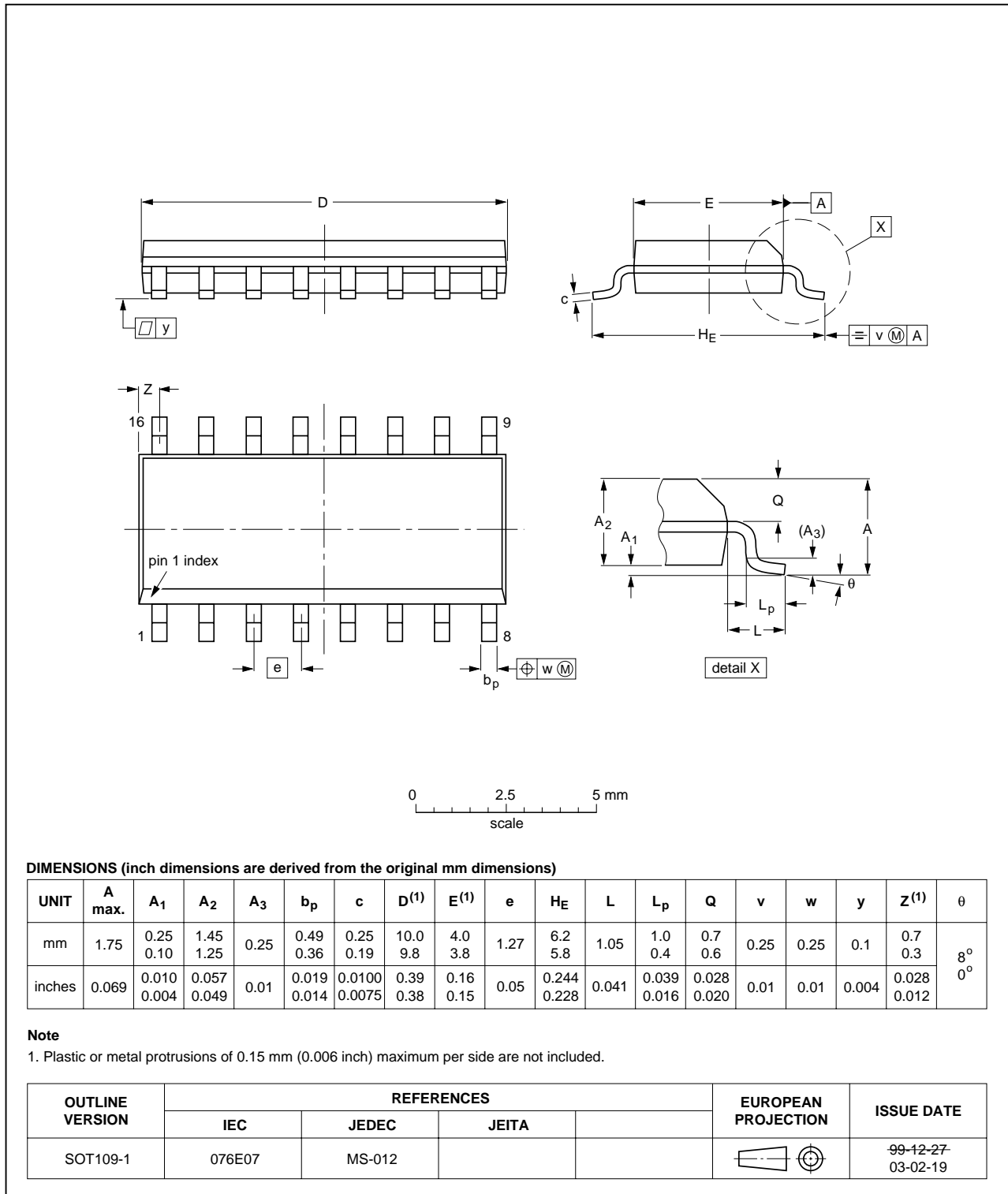


Fig 17. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

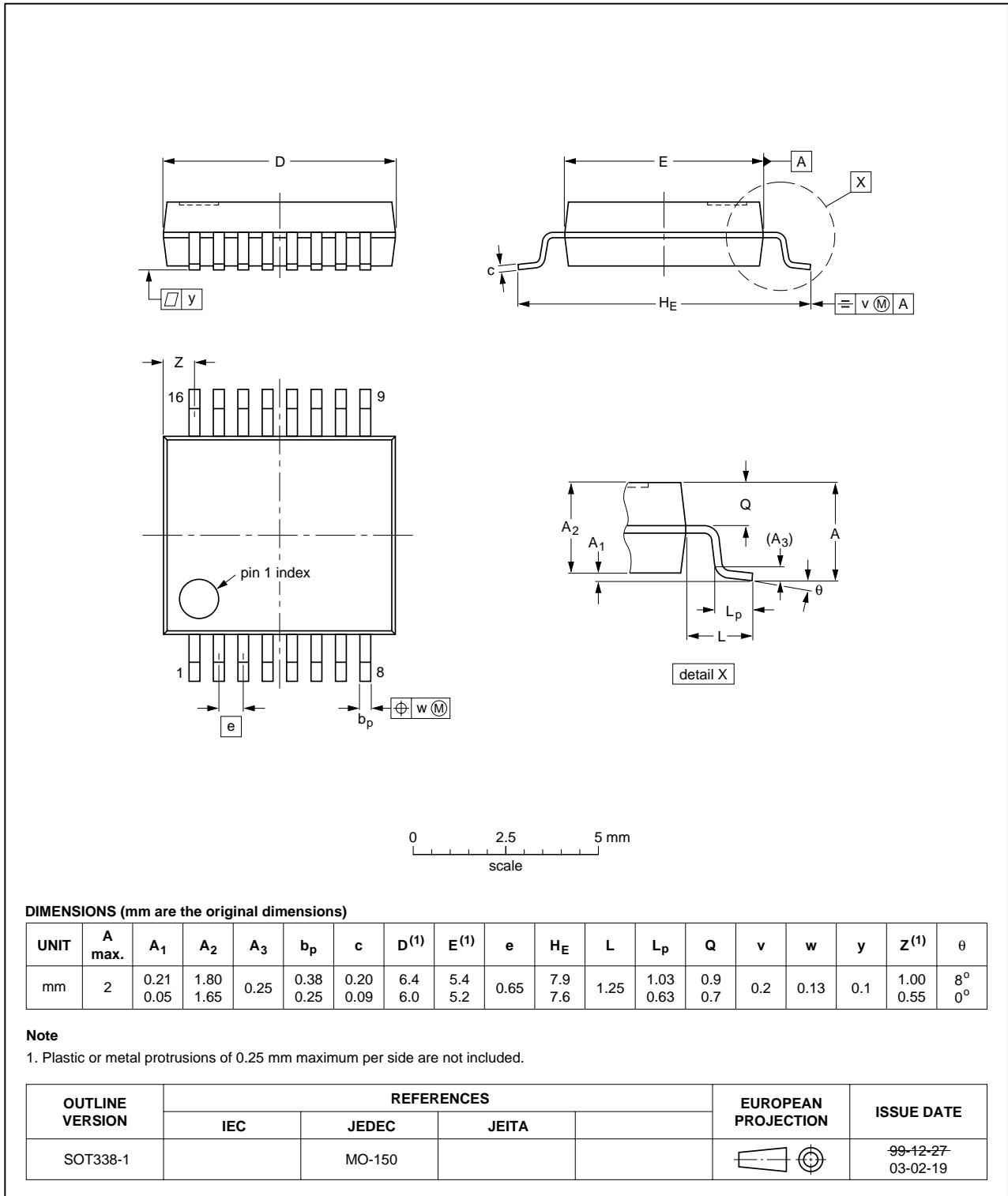


Fig 18. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

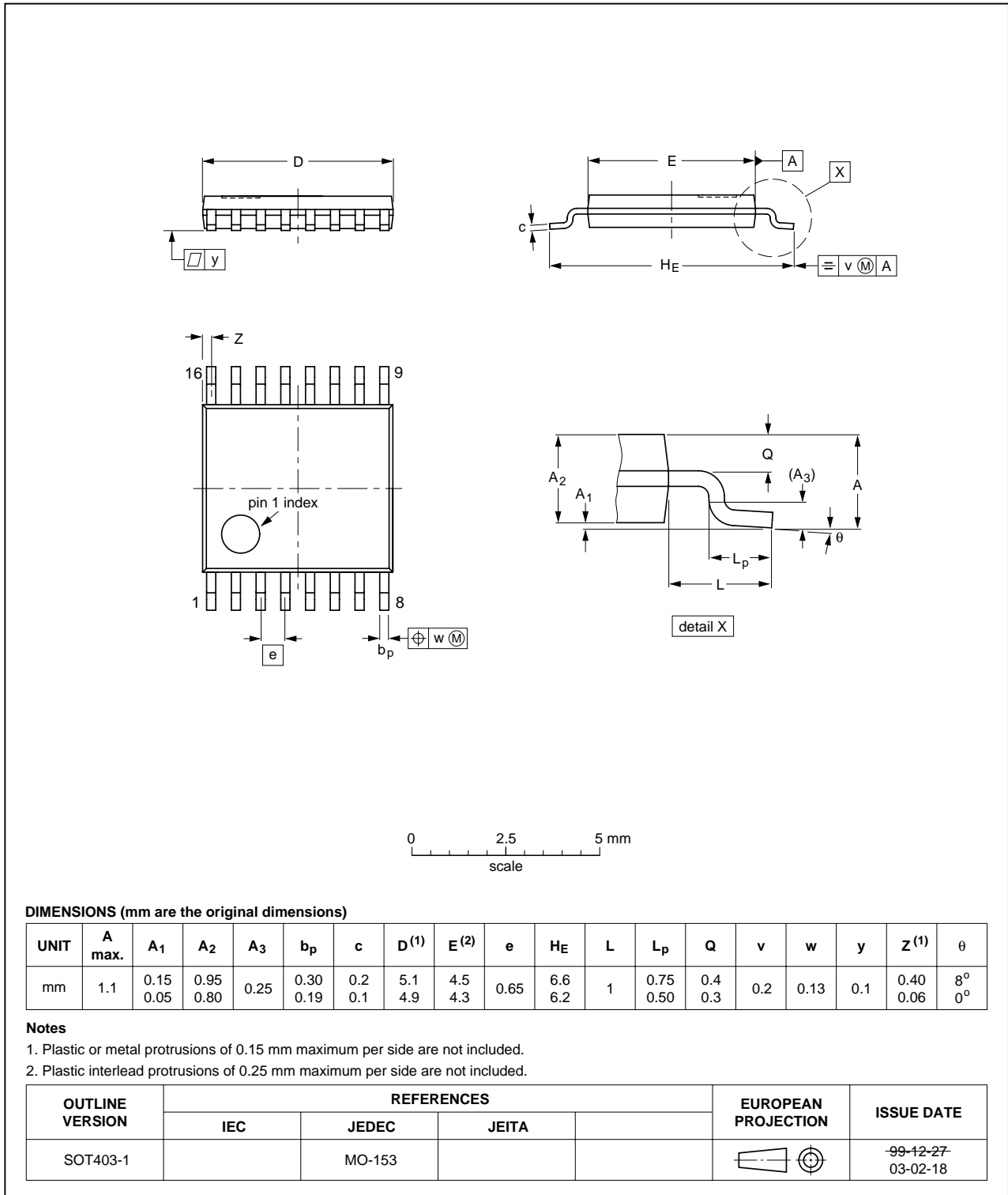


Fig 19. Package outline SOT403-1 (TSSOP16)

## 16. Revision history

**Table 10: Revision history**

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC40103_3	20041112	Product data sheet	-	9397 750 13812	74HC_HCT40103_CNV_2
Modifications:			<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors.</li><li>• Removed type number 74HCT40103.</li><li>• Inserted family specification.</li></ul>		
74HC_HCT40103_CNV_2	19970918	Product specification	-	-	74HC_HCT40103_1
74HC_HCT40103_1	19901201	Product specification	-	-	-

## 17. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 18. Definitions

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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## 20. Contact information

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## 21. Contents

1	General description . . . . .	1
2	Features . . . . .	2
3	Applications . . . . .	2
4	Quick reference data . . . . .	2
5	Ordering information . . . . .	3
6	Functional diagram . . . . .	3
7	Pinning information . . . . .	6
7.1	Pinning . . . . .	6
7.2	Pin description . . . . .	6
8	Functional description . . . . .	7
8.1	Function table . . . . .	7
9	Limiting values . . . . .	7
10	Recommended operating conditions . . . . .	8
11	Static characteristics . . . . .	8
12	Dynamic characteristics . . . . .	10
13	Waveforms . . . . .	16
14	Application information . . . . .	18
15	Package outline . . . . .	19
16	Revision history . . . . .	23
17	Data sheet status . . . . .	24
18	Definitions . . . . .	24
19	Disclaimers . . . . .	24
20	Contact information . . . . .	24



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