

Silicon PNP Power Transistors

2SB532

DESCRIPTION

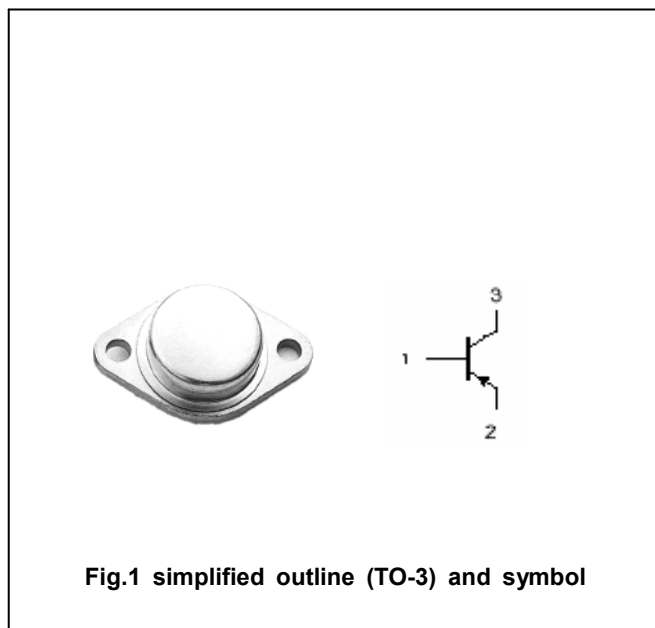
- With TO-3 package
- High power dissipation

APPLICATIONS

- Power amplifier applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

**Absolute maximum ratings(Ta=□)**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-80	V
V _{CEO}	Collector-emitter voltage	Open base	-80	V
V _{EBO}	Emitter-base voltage	Open collector	-5	V
I _C	Collector current		-5	A
P _C	Collector power dissipation	T _C =25□	60	W
T _j	Junction temperature		150	□
T _{stg}	Storage temperature		-65~150	□

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-30mA ; I _B =0	-80			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =-1mA ; I _C =0	-5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-4A ; I _B =-0.4A			-2.0	V
V _{BE}	Base-emitter on voltage	I _C =-4A ; V _{CE} =-5V			-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-80V ; I _E =0			-0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =-5V ; I _C =0			-0.1	mA
h _{FE-1}	DC current gain	I _C =-1A ; V _{CE} =-4V	80			
h _{FE-2}	DC current gain	I _C =-4A ; V _{CE} =-4V	20			
f _T	Transition frequency	I _C =-1A ; V _{CE} =-4V		10		MHz

PACKAGE OUTLINE

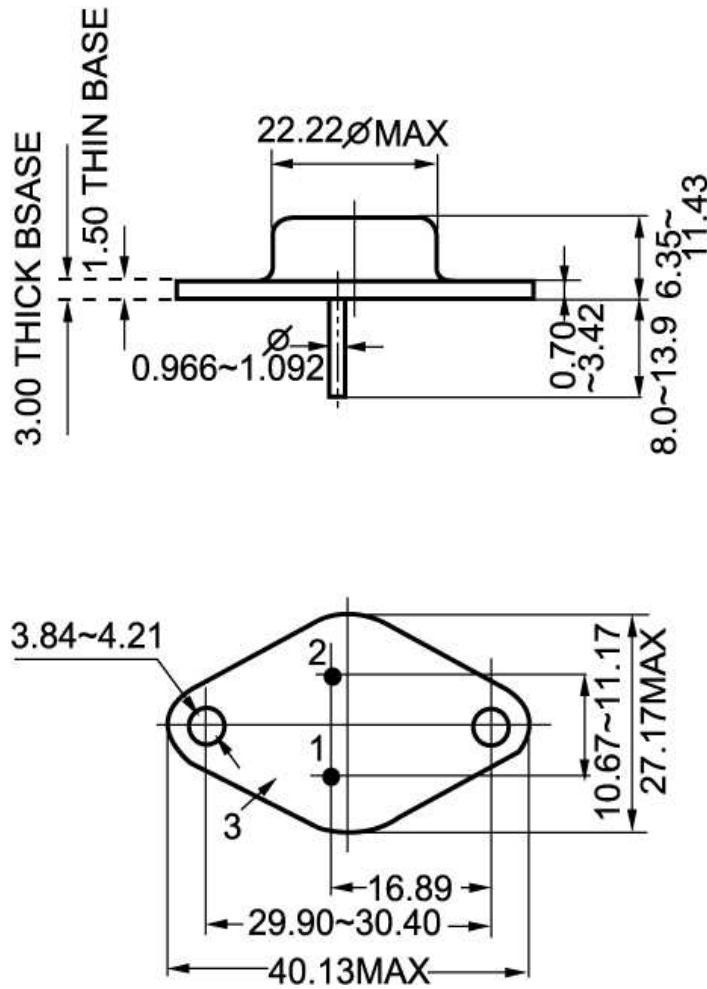


Fig.2 outline dimensions (unindicated tolerance:±0.1mm)