KS8995E

5-Port 10/100 Integrated Switch with PHY and Frame Buffer

Rev. 1.10

General Description

The KS8995E contains five 10/100 physical layer transceivers, five MAC (Media Access Control) units with an integrated layer 2 switch. The device runs in two modes. The first mode is a five port integrated switch and the second is as a five port switch with the fifth port decoupled from the physical port. In this mode access to the fifth MAC is provided using an MII (Media Independent Interface).

Useful configurations include a stand alone five port switch as well as a four port switch with a routing element connected to the extra MII port. The additional port is also useful for a public network interfacing.

The KS8995E is designed to reside in an unmanaged design not requiring processor intervention. This is achieved through I/O strapping or EEPROM programming at system reset time.

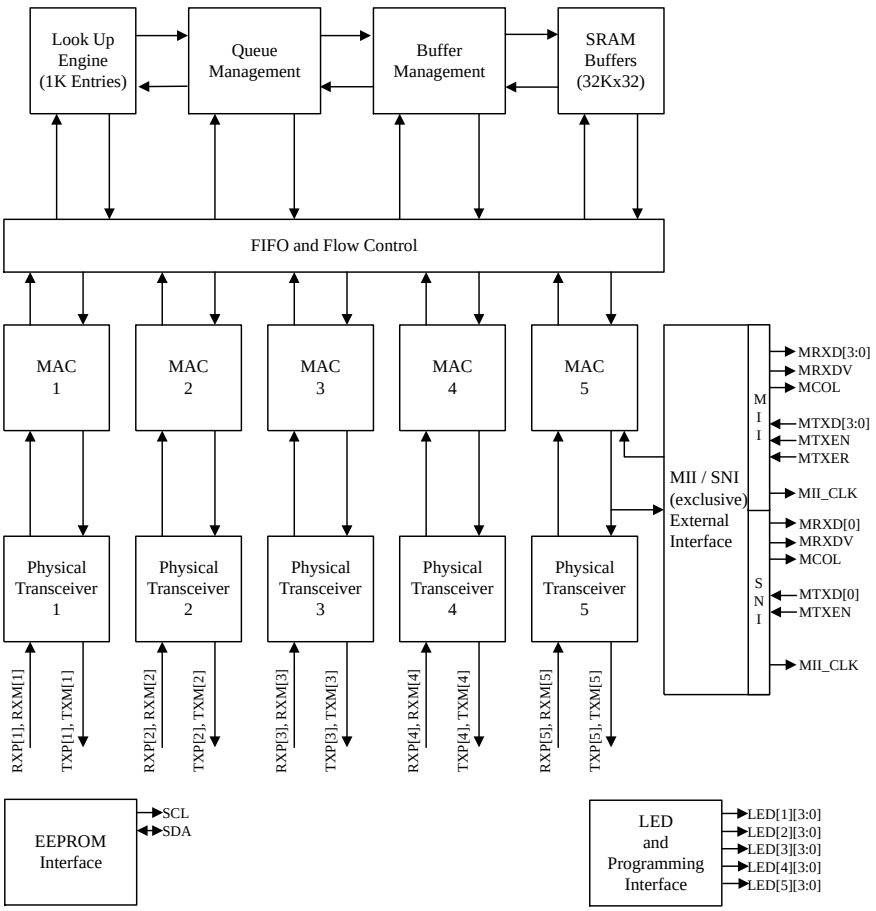
On the media side, the KS8995E supports 10BaseT, 100BaseTX and 100BaseFX as specified by the IEEE 802.3 committee.

Physical signal transmission and reception are enhanced through use of analog circuitry that makes the design more efficient and allows for lower power consumption and smaller chip die size.

The major enhancements from the KS8995 to the KS8995E are support for VLAN, traffic priority queuing, EEPROM programming for expanded control, MDI/MDI-X auto cross-over.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

Functional Diagram



Features

- 5-port 10/100 integrated switch with physical layer transceivers
- 128k Byte of SRAM on chip for frame buffering
- 1.4Gbps high performance memory bandwidth
- 10BaseT, 100BaseTX and 100BaseFX modes of operation
- Superior analog technology for reduced power and die size
- Supports port based VLAN
- QoS feature!! Supports DiffServ priority, 802.1p based priority or port-based priority
- Support for UTP or fiber installations
- Indicators for link, activity, full/half-duplex and speed
- Unmanaged operation via strapping or EEPROM at system reset time
- Hardware based 10/100, full/half, flow control and auto-negotiation
- Individual port forced modes (full-duplex, 100BaseTX) when auto-negotiation is disabled
- Wire speed reception and transmission
- Integrated address look-up engine, supports 1K absolute MAC addresses
- Automatic address learning, address aging and address migration
- Broadcast storm protection
- Full duplex IEEE 802.3x flow control
- Half duplex back pressure flow control
- Comprehensive LED support
- External MAC interface (MII or SNI) for router applications
- Supports MDI/MDI-X auto crossover
- Single 2.5V power supply
- 700mA (1.75W) including physical transmit drivers
- Commercial temperature range: 0°C to +70°C
- Available in 128-pin PQFP package

Ordering Information

Part Number	Temperature Range	Package
KS8995E	0°C to +70°C	128-Pin PQFP

Revision History

Revision	Date	Summary of Changes
1.00	7/28/00	Document origination.
1.01	8/21/00	Change LED programming.
1.02	10/30/00	Update voltage ratings.
1.03	2/02/01	Update transformer recommendations.
1.04	3/27/01	Update maximum frame length values.
1.05	4/20/01	Correct timing information.
1.06	5/03/01	Correct I/O definition.
1.07	5/11/01	Add MDI/MDI-X description.
1.08	7/25/01	Update timing information.
1.09	8/09/01	Add appendix D & MII timing. Add 10BaseTX power dissipation.
1.10	8/29/03	Convert to new format.

Table of Contents

System Level Applications

The KS8995E can be configured to fit either in a five port 10/100 application or as a four port 10/100 network interface with an extra MII / SNI port. This MII / SNI port can be connected to an external processor and used for routing purposes or public network access. The major benefits of using the KS8995E are the lower power consumption, unmanaged operation, flexible configuration, built in frame buffering, VLAN abilities and traffic priority control. Two such applications are depicted below.

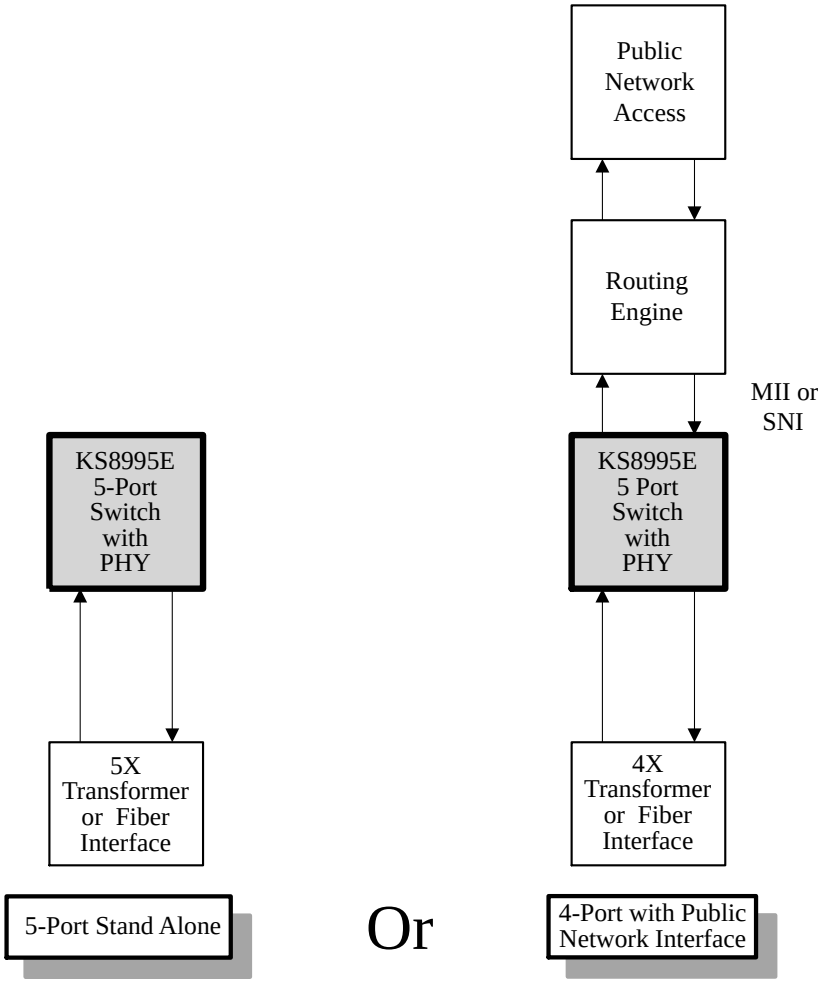


Figure 1. KS8995E Applications

Pin Description

Pin Number	Pin Name	Type(Note 1)	Port	Pin Function
1	N/C			Not used - float for normal operation (no connect)
2	TXP[1]	O	1	Physical transmit signal + (differential)
3	TXM[1]	O	1	Physical transmit signal - (differential)
4	GND_TX[1]	GND	1	Ground for transmit circuitry
5	VDD_TX[1:2]	P		2.5V for transmit circuitry
6	GND_TX[2]	GND	2	Ground for transmit circuitry
7	TXP[2]	O	2	Physical transmit signal + (differential)
8	TXM[2]	O	2	Physical transmit signal - (differential)
9	N/C			Not used - float for normal operation (no connect)
10	VDD_RX[2]	P	2	2.5V for equalizer
11	RXP[2]	I	2	Physical receive signal + (differential)
12	RXM[2]	I	2	Physical receive signal - (differential)
13	GND_RX[2]	GND	2	Ground for equalizer
14	VDD_BG	P		2.5V for analog circuitry
15	ISET	O		Set physical transmit output current
16	GND_BG	GND		Ground for analog circuitry
17	GND_RX[3]	GND	3	Ground for equalizer
18	RXP[3]	I	3	Physical receive signal + (differential)
19	RXM[3]	I	3	Physical receive signal - (differential)
20	VDD_RX[3]	P	3	2.5V for equalizer
21	N/C			Not used - float for normal operation (no connect)
22	TXP[3]	O	3	Physical transmit signal + (differential)
23	TXM[3]	O	3	Physical transmit signal - (differential)
24	GND_TX[3]	GND	3	Ground for transmit circuitry
25	VDD_TX[3:4]	P		2.5V for transmit circuitry
26	GND_TX[4]	GND	4	Ground for transmit circuitry
27	TXP[4]	O	4	Physical transmit signal + (differential)
28	TXM[4]	O	4	Physical transmit signal - (differential)
29	N/C			Not used - float for normal operation (no connect)
30	VDD_RX[4]	P	4	2.5V for equalizer
31	RXP[4]	I	4	Physical receive signal + (differential)
32	RXM[4]	I	4	Physical receive signal - (differential)
33	GND_RX[4]	GND	4	Ground for equalizer
34	GND_RX[5]	GND	5	Ground for equalizer
35	RXP[5]	I	5	Physical receive signal + (differential)
36	RXM[5]	I	5	Physical receive signal - (differential)
37	VDD_RX[5]	P	5	2.5V for equalizer
38	GND_ANA	GND		Analog ground

Note 1. P = power supply
GND = ground
I = input
O = output
I/O = bi-directional

Pin Number	Pin Name	Type(Note 1)	Port	Pin Function
39	N/C			Not used - float for normal operation (no connect)
40	TXP[5]	O	5	Physical transmit signal + (differential)
41	TXM[5]	O	5	Physical transmit signal - (differential)
42	GND_TX[5]	GND	5	Ground for transmit circuitry
43	VDD_TX[5]	P	5	2.5V for transmit circuitry
44	FXSD[2]	I	2	Fiber signal detect
45	FXSD[3]	I	3	Fiber signal detect
46	FXSD[4]	I	4	Fiber signal detect
47	FXSD[5]	I	5	Fiber signal detect
48	GND_RCV[5]	GND	5	Ground for clock recovery circuitry
49	VDD_RCV[5]	P	5	2.5V for clock recovery circuitry
50	VDD_RCV[4]	P	4	2.5V for clock recovery circuitry
51	GND_RCV[4]	GND	4	Ground for clock recovery circuitry
52	GND_RCV[3]	GND	3	Ground for clock recovery circuitry
53	VDD_RCV[3]	P	3	2.5V for clock recovery circuitry
54	TEST[1]	I		Factory test pin – float for normal operation
55	TEST[2]	I		Factory test pin – float for normal operation
56	SCL	O		Clock for EEPROM
57	SDA	I/O		Serial data for EEPROM
58	VDD	P		2.5V for core digital circuitry
59	GND	GND		Ground for digital circuitry
60	MTXEN	I	5	MII transmit enable
61	MTXD[3]	I	5	MII transmit bit 3
62	MTXD[2]	I	5	MII transmit bit 2
63	MTXD[1]	I	5	MII transmit bit 1
64	MTXD[0]	I	5	MII transmit bit 0
65	MTXER	I	5	MII transmit error
66	MII_CLK	O	5	MII clock
67	MRXDV	O	5	MII receive data valid
68	MRXD[3]	O	5	MII receive bit 3
69	MRXD[2]	O	5	MII receive bit 2
70	MRXD[1]	O	5	MII receive bit 1
71	MRXD[0]	O	5	MII receive bit 0
72	MCOL	O		MII collision detect
73	VDD-IO	P		2.5V or 3.3V for MII interface
74	GND	GND		Ground for digital circuitry
75	P5EXT	I	5	External port 5 selector
76	P5SNI	I	5	External port 5 mode selector

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Pin Number	Pin Name	Type(Note 1)	Port	Pin Function
77	MODESEL[3]	I		Selects LED and test modes
78	MODESEL[2]	I		Selects LED and test modes
79	VDD	P		2.5V for core digital circuitry
80	GND	GND		Ground for digital circuitry
81	MODESEL[1]	I		Selects LED and test modes
82	MODESEL[0]	I		Selects LED and test modes
83	TESTEN	I		Factory test pin – tie to ground for normal operation
84	SCANEN	I		Factory test pin – tie to ground for normal operation
85	RST#	I		Reset – active low
86	LED[1][3]	I/O	1	LED indicator 3
87	LED[1][2]	I/O	1	LED indicator 2
88	LED[1][1]	I/O	1	LED indicator 1
89	LED[1][0]	I/O	1	LED indicator 0
90	LED[2][3]	I/O	2	LED indicator 3
91	LED[2][2]	I/O	2	LED indicator 2
92	LED[2][1]	I/O	2	LED indicator 1
93	LED[2][0]	I/O	2	LED indicator 0
94	VDD	P		2.5V for core digital circuitry
95	GND	GND		Ground for digital circuitry
96	LED[3][3]	I/O	3	LED indicator 3
97	LED[3][2]	I/O	3	LED indicator 2
98	LED[3][1]	I/O	3	LED indicator 1
99	LED[3][0]	I/O	3	LED indicator 0
100	VDD-IO	P		2.5V or 3.3V for MII interface
101	GND	GND		Ground for digital circuitry
102	LED[4][3]	I/O	4	LED indicator 3
103	LED[4][2]	I/O	4	LED indicator 2
104	LED[4][1]	I/O	4	LED indicator 1
105	LED[4][0]	I/O	4	LED indicator 0
106	LED[5][3]	I/O	5	LED indicator 3
107	LED[5][2]	I/O	5	LED indicator 2
108	LED[5][1]	I/O	5	LED indicator 1 /
109	LED[5][0]	I/O	5	LED indicator 0 /
110	VDD	P		2.5V for core digital circuitry
111	GND	GND		Ground for digital circuitry
112	X2	O		Connect to crystal
113	X1	I		Crystal or clock input
114	VDD_PLL	P		2.5V for phase locked loop circuitry
115	GND_PLL	GND		Ground for phase locked loop circuitry

Note 1. P = power supply
GND = ground
I = input
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Pin Number	Pin Name	Type(Note 1)	Port	Pin Function
116	GND_RCV[2]	GND	2	Ground for clock recovery circuitry
117	VDD_RCV[2]	P	2	2.5V for clock recovery circuitry
118	VDD_RCV[1]	P	1	2.5V for clock recovery circuitry
119	GND_RCV[1]	GND	1	Ground for clock recovery circuitry
120	MUX[2]	I		Factory test pin – float for normal operation
121	MUX[1]	I		Factory test pin – float for normal operation
122	FXSD[1]	I		Fiber signal detect
123	AOUT	O		Factory test output – float for normal operation
124	GND_RX[1]	GND	1	Ground for equalizer
125	RXP[1]	I	1	Physical receive signal + (differential)
126	RXM[1]	I	1	Physical receive signal - (differential)
127	VDD_RX[1]	P	1	2.5V for equalizer
128	GND_ANA	GND		Analog ground

Note 1. P = power supply
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I = input
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I/O = bi-directional

I/O Grouping

Group Name	Description
PHY	Physical Interface
MII	Media Independant Interface
SNI	Serial Network Interface
IND	LED Indicators
UP	Unmanaged Programmable
CTRL	Control and Miscellaneous
TEST	Test (Factory)
PWR/GND	Power and Ground

I/O Descriptions

Group	I/O Names	Active Status	Description
PHY	RXP[1:5] RXM[1:5]	Analog	Differential inputs (receive) for connection to media (transformer or fiber module)
	TXP[1:5] TXM[1:5]	Analog	Differential outputs (transmit) for connection to media (transformer or fiber module)
	FXSD[1:5]	H	Fiber signal detect - connect to fiber signal detect output on fiber module. Tie low for 100TX mode.
	ISET	Analog	Transmit Current Set. Connecting an external reference resistor to set transmitter output current. This pin connects a 1% 3KΩ resistor if a transformer of turns ratio of 1:1 is used.
MII	MRXD[0:3]	H	Four bit wide data bus for receiving MAC frames
	MRXDV	H	Receive data valid
	MCOL	H	Receive collision detection
	MTXD[0:3]	H	Four bit wide data bus for transmitting MAC frames
	MTXEN	H	Transmit enable
	MTXER	H	Transmit error
	MII_CLK	Clock	MII interface clock
SNI	MTXD[0]	H	Serial transmit data
	MTXEN	H	Transmit enable
	MRXD[0]	H	Serial receive data
	MRXDV	H	Receive carrier sense/data valid
	MCOL	H	Collision detection
	MII_CLK	Clock	SNI interface clock
IND	LED[1:5][0]	L	Output (after reset) Mode 0: Speed (on = 100/off = 10) Mode 1: Speed (on = 100/off = 10) Mode 2: Speed (on = 100/off = 10) Mode 3: Speed (on = 100/off = 10)
	LED[1:5][1]	L	Output (after reset) Mode 0: Full Duplex (on = full/off = half) Mode 1: Link (on = connected/off = not connected) Mode 2: Link (on = connected/off = not connected) Mode 3: Reserved
	LED[1:5][2]	L	Output (after reset) Mode 0: Collision (on = collision / off = no collision) Mode 1: Transmit Activity (on during transmission) Mode 2: Full Duplex + Collision (constant on = full-duplex / intermittent on = collision/off = half-duplex with no collision) Mode 3: Full Duplex + Collision (constant on = full-duplex / intermittent on = collision/off = half-duplex with no collision)
	LED[1:5][3]	L	Output (after reset) Mode 0: Link + Activity Mode 1: Receive Activity (on = receiving/off = not receiving) Mode 2: Activity (on = transmit or receive activity/off = no activity) Mode 3: Link + Activity *Note: Mode is set by MODESEL[3:0] ; please see description in UP (unmanaged programming) section.*

<table>
<tr><th>Group</th><th>I/O Names</th><th>Active Status</th><th>Description(Note 1)</th></tr>
<tr><td>UP</td><td>MODESEL[3:0]</td><td>H</td><td>Mode select at reset time. LED mode is selected by using the table below. Note that under normal operation MODESEL[3:2] must be tied low.
<table>
<tr><th colspan="4">MODESEL</th><th></th></tr>
<tr><th>3</th><th>2</th><th>1</th><th>0</th><th>Operation</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>LED mode 0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>LED mode 1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>LED mode 2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>LED mode 3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Used for factory testing</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Used for factory testing</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Used for factory testing</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Used for factory testing</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Used for factory testing</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Used for factory testing</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Used for factory testing</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Used for factory testing</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Used for factory testing</td></tr>
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<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Used for factory testing</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Used for factory testing</td></tr>
</table></td></tr>
<tr><td></td><td>LED[1][3]</td><td></td><td>Programs flow control on all PHY ports at reset time.
D = No flow control
F/U = Flow control</td></tr>
<tr><td></td><td>LED[1][2]</td><td></td><td>Programs flow control on the external MAC port at reset time.
D = No flow control
U = Flow control</td></tr>
<tr><td></td><td>LED[1][1:0]</td><td></td><td>Programs buffer allocation per port at reset time. Use the following table to select the option:
<table>
<tr><th colspan="2">LED[1]</th><th></th></tr>
<tr><th>0</th><th>1</th><th>Description</th></tr>
<tr><td>D</td><td>D</td><td>205 buffers max per port (default)</td></tr>
<tr><td>D</td><td>U</td><td>512 buffers max per port</td></tr>
<tr><td>U</td><td>D</td><td>768 buffers max per port</td></tr>
<tr><td>U</td><td>U</td><td>512 buffers (adaptive) per port</td></tr>
</table></td></tr>
<tr><td></td><td>LED[2][3]</td><td></td><td>Programs MAC address aging in the address look-up table at reset time. Aging eliminates old entries from the table.
D = No aging
F/U = 5 minute aging</td></tr>
<tr><td></td><td>LED[2][2]</td><td></td><td>Pull-down for normal operation.</td></tr>
<tr><td></td><td>LED[2][1]</td><td></td><td>Programs back pressure in half-duplex at reset time.
D = No back pressure
F/U = Back pressure enabled</td></tr>
<tr><td></td><td>LED[2][0]</td><td></td><td>Programs aggressive back off in half-duplex at reset time.
D = Standard back off
F/U = Aggressive mode enabled</td></tr>
<tr><td></td><td>LED[3][3]</td><td></td><td>Programs no excessive collision drop at reset time.
D = Drop after 16 collisions
F/U = No drop after 16 collisions</td></tr>
<tr><td></td><td>LED[3][2]</td><td></td><td>Programs a limit for broadcast frames at reset time.
D = No limit
U = 25% - 3% limit of broadcast frames
Note: EEPROM programming can limit broadcast frames at 25%, 12%, 6% or 3%.
See “EEPROM Register” 7 bits 7-6.</td></tr>
</table>

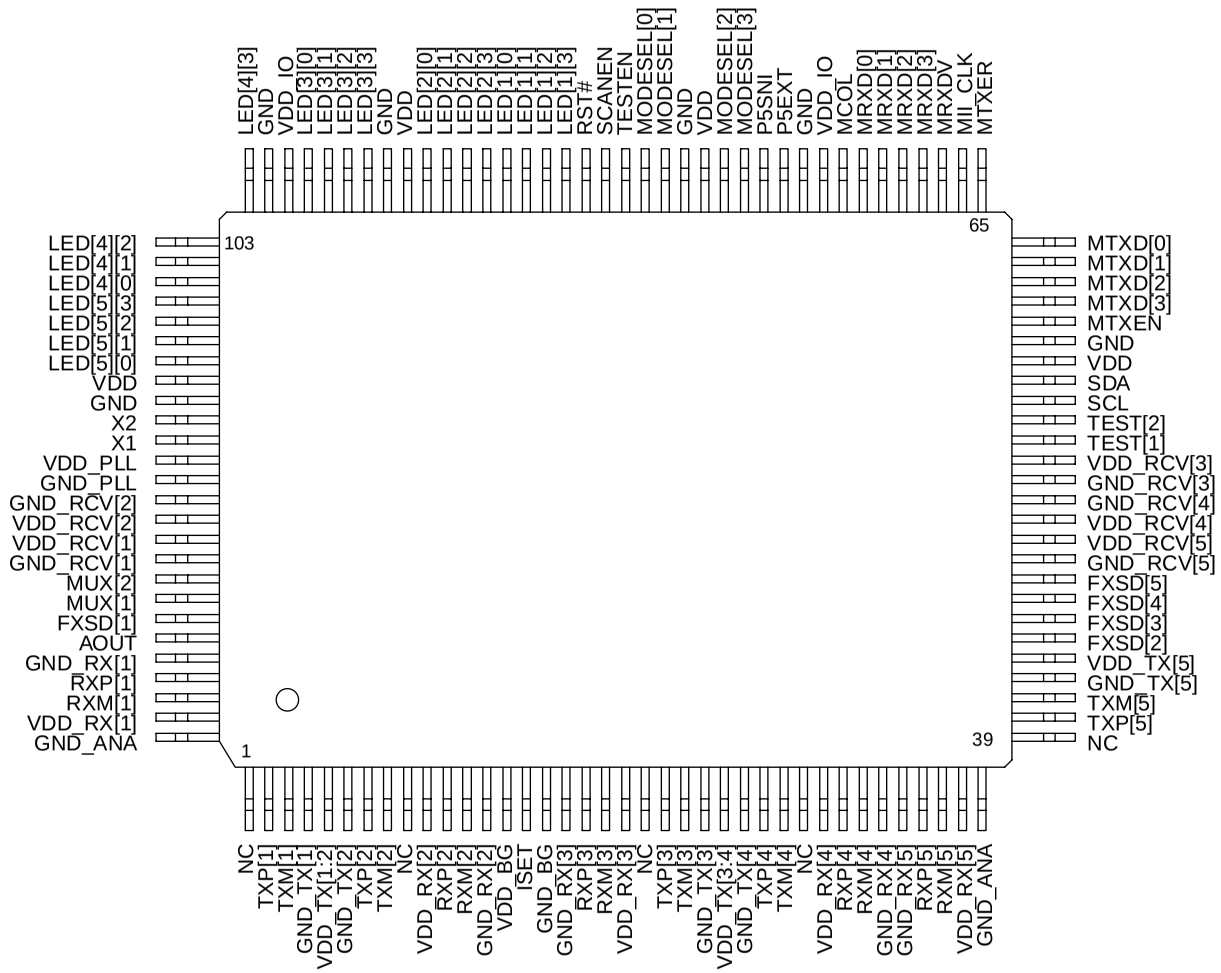
Note 1. All unmanaged programming takes place at reset time only. For unmanaged programming: F = Float, D = Pull-down, U = Pull-up. See *“Reference Circuits”* section.

<table>
<tr><th>Group</th><th>I/O Names</th><th>Active Status</th><th>Description(Note 1)</th></tr>
<tr><td></td><td>LED[3][1:0]
LED[4][3:1]</td><td></td><td>Programs force 100BaseTX / 10BaseT mode at reset time. Disable auto-negotiation to use this force mode. Use the table below to set this mode on the appropriate port.
<table>
<tr><th>Signal</th><th>Port</th><th>Force 10BaseT w/o Auto-negotiation</th><th>Force 100BaseTX w/o Auto-negotiation</th><th>Auto-negotiation enabled</th></tr>
<tr><td>LED[3][1]
LED[3][0]
LED[4][3]
LED[4][2]
LED[4][1]</td><td>5
4
3
2
1</td><td>D
D
D
D
D</td><td>U
U
U
U
U</td><td>F
F
F
F
F</td></tr>
</table></td></tr>
<tr><td></td><td>LED[4][0]
LED[5][3:0]</td><td></td><td>Programs force full / half-duplex mode at reset time. Disable auto-negotiation to use this force mode. Use the table below to set this mode on the appropriate port.
<table>
<tr><th>Signal</th><th>Port</th><th>Force half-duplex w/o Auto-negotiation</th><th>Force full-duplex w/o Auto-negotiation</th><th>Auto-negotiation enabled</th></tr>
<tr><td>LED[4][0]
LED[5][3]
LED[5][2]
LED[5][1]
LED[5][0]</td><td>5
4
3
2
1</td><td>D
D
D
D
D</td><td>U
U
U
U
U</td><td>F
F
F
F
F</td></tr>
</table></td></tr>
<tr><td></td><td>MRXD[0:3]
MCOL</td><td></td><td>Programs auto-negotiation enable / disable at reset time. Use the table below to set this mode on the appropriate port.
<table>
<tr><th>Signal</th><th>Port</th><th>Enable auto-negotiation</th><th>Disable auto-negotiation</th></tr>
<tr><td>MRXD[3]
MRXD[2]
MRXD[1]
MRXD[0]
MCOL</td><td>5
4
3
2
1</td><td>D
D
D
D
D</td><td>U
U
U
U
U</td></tr>
</table>
Note 1. To use external MII on port 5 disable auto-negotiation by pulling MRXD[3] up.
Note 2. Use the “disable auto-negotiation” mode in conjunction with force 10/100 and force full/half-duplex to get the desired configuration. See above descriptions for force modes.</td></tr>
<tr><td>CTRL</td><td>P5EXT</td><td>H</td><td>Port 5 external selection.
D = 5 port IS mode
U = External MAC interface enabled and no longer connected to internal port 5 PHY.</td></tr>
<tr><td></td><td>P5SNI</td><td>H</td><td>Port 5 interface protocol. This is only relevant when P5EXT is tied high.
D = MII interface
U = SNI interface</td></tr>
<tr><td></td><td>X1</td><td>Clock</td><td>External crystal or clock input.</td></tr>
<tr><td></td><td>X2</td><td>Clock</td><td>Used when other polarity of crystal is needed. This is unused for a normal clock input.</td></tr>
<tr><td></td><td>SCL</td><td>Clock</td><td>Clock for EEPROM.</td></tr>
<tr><td></td><td>SDA</td><td></td><td>Serial data for EEPROM.</td></tr>
<tr><td></td><td>RST#</td><td>L</td><td>System reset.</td></tr>
<tr><td>TEST</td><td>TESTEN</td><td>H</td><td>Factory test input: tie to ground for normal operation.</td></tr>
<tr><td></td><td>SCANEN</td><td>H</td><td>Factory test input: tie to ground for normal operation.</td></tr>
<tr><td></td><td>MUX[1:2]</td><td>H</td><td>Factory test input: leave open.</td></tr>
<tr><td></td><td>AOUT</td><td>H</td><td>Factory test output: leave open.</td></tr>
<tr><td></td><td>TEST[1:2]</td><td>H</td><td>Factory test inputs: leave open.</td></tr>
</table>

Note 1. All unmanaged programming takes place at reset time only. For unmanaged programming: F = Float, D = Pull-down, U = Pull-up. See *“Reference Circuits”* section.

Group	I/O Names	Active Status	Description
PWR	VDD-RX[1:5]		2.5V for equalizer.
	GND-RX[1:5]		Ground for equalizer.
	VDD-TX[1:2]		2.5V for transmit circuitry.
	VDD-TX[3:4]		2.5V for transmit circuitry.
	VDD-TX[5]		2.5V for transmit circuitry.
	GND-TX[1:5]		Ground for transmit circuitry.
	VDD-RCV[1:5]		2.5V for clock recovery circuitry.
	GND-RCV[1:5]		Ground for clock recovery.
	VDD-PLL		2.5V for phase locked loop circuitry.
	GND-PLL		Ground for phase locked loop circuitry.
	GND-ANA		Analog ground.
	VDD_BG		2.5V for analog circuits.
	GND-BG		Analog ground.
	VDD		2.5V for core digital circuitry.
	VDD-IO		2.5V or 3.3V for MII interface.
	GND		Ground for digital circuitry.

Pin Configuration



128-Pin PQFP (PQ)

Functional Overview: Physical Layer Transceiver

100BaseTX Transmit

The 100BaseTX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ to NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel to serial conversion, which converts the RMII or SMII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ to NRZI format, then transmitted in MLT3 current output. The output current is set by an external 1% 3.01kΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4 ns and complies to the ANSI TP-PMD standard regarding amplitude balance, overshoot and timing jitters. The wave-shaped 10BaseT output is also incorporated into the 100BaseTX transmitter.

100BaseTX Receive

The 100BaseTX receiver function performs adaptive equalization, DC restoration, MLT3 to NRZI conversion, data and clock recovery, NRZI to NRZ conversion, de-scrambling, 4B/5B decoding and serial to parallel conversion. The receiving side starts with the equalization filter to compensate inter-symbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and can self adjust against the environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of base line wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the RMII or SMII formats and provided as the input data to the MAC.

PLL Clock Synthesizer

The KS8995E generates 125MHz, 42MHz, 25MHz and 10MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal.

Scrambler/De-Scrambler (100BaseTX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled by the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then de-scramble the incoming data stream with the same sequence at the transmitter.

100BaseFX Operation

100BaseFX operation is very similar to 100BaseTX operation with the differences being that the scrambler / de-scrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In this mode the auto-negotiation feature is bypassed since there is no standard that supports fiber auto-negotiation.

100BaseFX Signal Detection

The physical port runs in 100BaseFX mode if FXSDx >0.6V. This signal is referenced to VREFx which is set at 1/2 Vdd but can be overridden by an external level. VREFx can be connected to the “minus” signal of a differential pair coming from the fiber module (“plus connects to FXSDx) used to convey signal detect. When FXSDx is below 0.6V then 100BaseFX mode is disabled.

100BaseFX Far End Fault

Far end fault occurs when the signal detection is logically false from the receive fiber module. When this occurs, the transmission side signals the other end of the link by sending 84 1’s followed by a zero in the idle period between frames.

10BaseT Transmit

The output 10BaseT driver is incorporated into the 100BaseT driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental when driven by an all-ones Manchester-encoded signal.

10BaseT Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulse widths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KS8995E decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

Power Management

Power Save Mode

The KS8995E will turn off everything except for the Energy Detect and PLL circuits when the cable is not installed on an individual port basis. In other words, the KS8995E will shutdown most of the internal circuits to save power if there is no link.

MDI/MDI-X Auto Crossover

The KS8995E supports MDI/MDI-X auto crossover. This facilitates the use of either a straight connection CAT-5 cable or a crossover CAT-5 cable. The auto-sense function will detect remote transmit and receive pairs, and correctly assign the transmit and receive pairs from the Micrel device. This can be highly useful when end users are unaware of cable types and can also save on an additional uplink configuration connection.

The auto MDI/MDI-X is achieved by the Micrel device listening for the far end transmission channel and assigning transmit/receive pairs accordingly.

Auto-Negotiation

The KS8995E conforms to the auto-negotiation protocol as described by the 802.3 committee. Auto-negotiation allows UTP (Unshielded Twisted Pair) link partners to select the best common mode of operation. In auto-negotiation the link partners advertise capabilities across the link to each other. If auto-negotiation is not supported or the link partner to the KS8995E is forced to bypass auto-negotiation, then the mode is set by observing the signal at the receiver. This is known as parallel mode because while the transmitter is sending auto-negotiation advertisements, the receiver is listening for advertisements or a fixed signal protocol.

The flow for the link set up is depicted below.

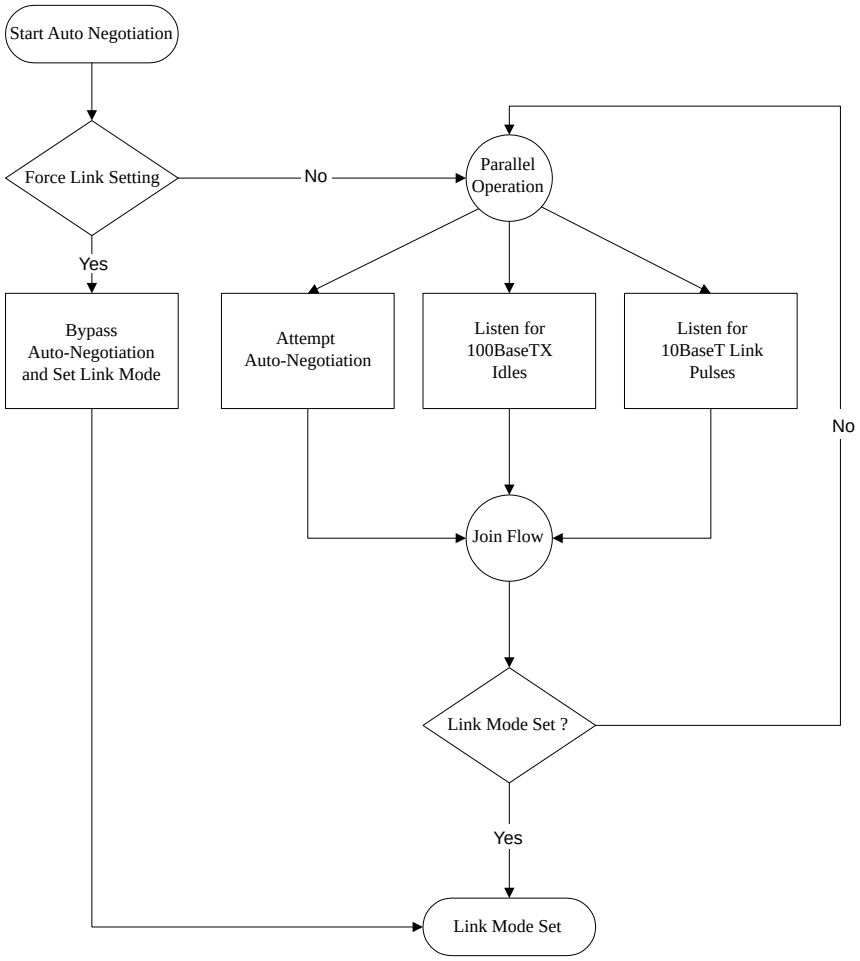


Figure 2. Auto-Negotiation

Functional Overview: Switch Core

Address Look Up

The internal look-up table stores MAC addresses and their associated information. It contains 1K full CAM with 48-bit address plus switching information. The KS8995E is guaranteed to learn 1K addresses and distinguishes itself from hash-based look-up tables which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

Learning

The internal look-up engine will update its table with a new entry if the following conditions are met:

- The received packet's SA does not exist in the look-up table.
- The received packet is good; the packet has no receiving errors, and is of legal length.

The look-up engine will insert the qualified SA into the table, along with the port number, time stamp. If the table is full, the last entry of the table will be deleted first to make room for the new entry.

Migration

The internal look-up engine also monitors whether a station is moved. If it happens, it will update the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet is good; the packet has no receiving errors, and is of legal length.

The look-up engine will update the existing record in the table with the new source port information.

Aging

The look-up engine will update time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look-up engine will then remove the record from the table. The look-up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300 seconds. This feature can be enabled or disabled by external pull-up or pull-down resistors.

Forwarding

The KS8995E will forward packets as follows:

- If the DA look-up results is a "match", the KS8995E will use the destination port information to determine where the packet goes.
- If the DA look-up result is a "miss", the KS8995E will forward the packet to all other ports except the port that received the packet.
- All the multicast and broadcast packets will be forwarded to all other ports except the source port.

The KS8995E will not forward the following packets:

- Error packets. These include framing errors, FCS errors, alignment errors, and illegal size packet errors.
- 802.3x pause frames. The KS8995E will intercept these packets and do the appropriate actions.
- "Local" packets. Based on destination address (DA) look-up. If the destination port from the look-up table matches the port where the packet was from, the packet is defined as "local".

Switching Engine

The KS8995E has a very high performance switching engine to move data to and from the MAC's, packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency.

The KS8995E has in internal buffer for frames that is 32Kx32 (128KB). This resource is shared between the five ports. Buffer sizing per port can be programmed at system reset time by using the unmanaged program mode (I/O strapping).

Each buffer is sized at 128B and therefore there are a total of 1024 buffers available. A per port maximum can be set at 205 (equal allocation), 512 or 768. There is also an adaptive 512 size mode that reacts to port traffic.

MAC (Media Access Controller) Operation

The KS8995E strictly abides by IEEE 802.3 standard to maximize compatibility.

Inter Packet Gap (IPG)

If a frame is successfully transmitted, the 96-bit time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96-bit time IPG is measured from MCRS and the next MTXEN.

Backoff Algorithm

The KS8995E implements the IEEE Std 802.3 binary exponential back-off algorithm, and optional "aggressive mode" back off. After 16 collisions, the packet will be optionally dropped depending on the chip configuration.

Late Collision

If a transmit packet experiences collisions after 512-bit times of the transmission, the packet will be dropped.

Illegal Frames

The KS8995E discards frames less than 64 bytes and can be programmed to accept frames up to 1536 bytes. Since the KS8995E supports VLAN tags, the maximum sizing is adjusted when these tags are present. See the “EEPROM” section for programming options.

Flow Control

The KS8995E supports standard 802.3x flow control frames on both transmit and receive sides.

On the receive side, if the KS8995E receives a pause control frame, the KS8995E will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (being flow controlled), only flow control packets from the KS8995E will be transmitted.

On the transmit side, the KS8995E has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KS8995E will flow control a port, which just received a packet, if the destination port resource is being used up. The KS8995E will issue a flow control frame (XOFF), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KS8995E will send out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysterisis feature is provided to prevent flow control mechanism from being activated and deactivated too many times.

The KS8995E will flow control all ports if the receive queue becomes full.

Half Duplex Back Pressure

Half duplex back pressure option (Note: not in 802.3 standards) is also provided. The activation and deactivation conditions are the same as the above in full-duplex mode. If back pressure is required, the KS8995E will send preambles to defer other stations’ transmission (carrier sense deference). To avoid jabber and excessive deference defined in 802.3 standard, after a certain time it will discontinue the carrier sense but it will raise the carrier sense quickly. This short silent time (no carrier sense) is to prevent other stations from sending out packets and keeps other stations in carrier sense deferred state. If the port has packets to send during a back pressure situation, the carrier sense type back pressure will be interrupted and those packets will be transmitted instead. If there are no more packets to send, carrier sense type back pressure will be active again until switch resources free up. If a collision occurs, the binary exponential back-off algorithm is skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets.

Broadcast Storm Protection

The KS8995E has an intelligent option to protect the switch system from receiving too many broadcast packets. Broadcast packets will be forwarded to all ports except the source port, and thus will use too many switch resources (bandwidth and available space in transmit queues). The KS8995E will discard broadcast or multicast packets if the number of those packets exceeds the threshold (configured by strapping during reset and EEPROM settings) in a preset period of time. If the preset period expires it will then resume receiving broadcast or multicast packets until the threshold is reached. The options are 25%, 12%, 6% or 3% of network line rate for the maximum broadcast/multicast receiving threshold or unlimited (feature off).

MII Interface Operation

The MII (Media Independent Interface) is specified by the IEEE 802.3 committee and provides a common interface between physical layer and MAC layer devices. The KS8995E MII behaves like a physical layer device. There are two distinct groups, one being for transmission and the other for receiving. The table below describes the signals used in this interface.

MII Signal	Description	KS8995E Signal
MTXEN	Transmit enable	MTXEN
MTXER	Transmit error	MTXER
MTXD3	Transmit data bit 3	MTXD[3]
MTXD2	Transmit data bit 2	MTXD[2]
MTXD1	Transmit data bit 1	MTXD[1]
MTXD0	Transmit data bit 0	MTXD[0]
MTXC	Transmit clock	MII_CLK
MCOL	Collision detection	MCOL
MCRS	Carrier sense	MRXDV
MRXDV	Receive data valid	MRXDV
MRXER	Receive error	Not used
MRXD3	Receive data bit 3	MRXD[3]
MRXD2	Receive data bit 2	MRXD[2]
MRXD1	Receive data bit 1	MRXD[1]
MRXD0	Receive data bit 0	MRXD[0]
MRXC	Receive clock	MII_CLK

Table 1. MII Signals

This interface is a nibble wide data interface and therefore runs at 1/4 the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Likewise, the receive side has indicators that convey when the data is valid and without physical layer errors.

For half-duplex operation there is a signal that indicate a collision has occurred during transmission.

Note that the signal MRXER is not provided on the MII interface for the KS8995E. Normally this would indicate a receive error coming from the physical layer device, but since this port connects to a MAC device it is not appropriate. If the connecting device has a MRXER pin, this should be tied low on the other device.

SNI Interface (7-wire) Operation

The SNI (Serial Network Interface) is compatible with some controllers used for network layer protocol processing. KS8995E acts like a PHY device to external controllers. This interface can be directly connected to these types of devices. The signals are divided into two groups, one being for transmission and the other being the receive side. The signals involved are described in the table below.

SNI Signal	Description	KS8995E SNI Signal	KS8995E Input/Output
TXEN	Transmit enable	MTXEN	Input
TXD	Serial transmit data	MTXD[0]	Input
TXC	Transmit clock	MII_CLK	Output
COL	Collision detection	MCOL	Output
CRS	Carrier sense	MRXDV	Output
RXD	Serial receive data	MRXD[0]	Output
RXC	Receive clock	MII_CLK	Output

Table 2. SNI Signal

This interface is a bit wide data interface and therefore runs at the network bit rate (not encoded). An additional signal on the transmit side indicates when data is valid. Likewise, the receive side has an indicator that conveys when the data is valid.

For half-duplex operation there is a signal that indicate a collision has occurred during transmission.

8995E Improvements

Priority Schemes

The KS8995E can determine priority through three different means. The first method is a simple per port method, the second is via the 802.1p frame tag and the third is by viewing the DSCP (TOS) field in the IPv4 header. Of course for the priority to be effective, the high and low priority queues must be enabled on the destination port or egress point.

Per Port Method

General priority can be specified on a per port basis. In this type of priority all traffic from the specified input port is considered high priority in the destination queue. This can be useful in IP phone applications mixed with other data types of traffic where the IP phone connects to a specific port. The IP phone traffic would be high priority (outbound) to the wide area network. The inbound traffic to the IP phone is all of the same priority to the IP phone.

802.1p Method

This method works well when used with ports that have mixed data and media flows. The inbound port examines the priority field in the tag and determines the high or low priority. Priority profiles are setup in the Priority Classification Control in the EEPROM.

IPv4 DSCP Method

This is another per frame way of determining outbound priority. The DSCP (Differentiated Services Code Point–RFC#2474) method uses the TOS field in the IP header to determine high and low priority on a per code point basis. Each fully decoded code point can have either a high or low priority. A larger spectrum of priority flows can be defined with this larger code space.

More specific to implementation, the most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bit in the DSCP register. If the register bit is a 1, the priority is high and if 0, the priority is low.

Other Priority Considerations

When setting up the priority scheme, one should consider other available controls to regulate the traffic. One of these is Priority Control Scheme (register 3 bits 7-6) which controls the interleaving of high and low priority frames. Options allow from a 2:1 ratio up to a setting that sends all the high priority first. This setting controls all ports globally. Another global feature is Priority Buffer Reserve (register 5 bit 7). If this is set, there is a 12KB (10%) buffer dedicated to high priority traffic, otherwise if cleared the buffer is shared between all traffic.

On an individual port basis there are controls that enable DSCP, 802.1p, port based and high/low priority queues. These are contained in registers 3-7 bits 5-3 and 0.

The table below briefly summarizes priority features. For more detailed settings see the EEPROM register description.

Register(s)	Bit(s)	Global/Port	Description
			General
3	7-6	Global	Priority Control Scheme: Transmit buffer high/low interleave control.
5	7	Global	Priority Buffer Reserve: Reserves 12KB of the buffer for high priority traffic.
3-7	0	Port	Enable Port Queue Split: Splits the transmit queue on the desired port for high and low priority traffic.
			DSCP Priority
3-7	5	Port	Enable Port DSCP: Looks at DSCP field in IP header to decide high or low priority.
23-30	7-0	Global	DSCP Priority Points: Fully decoded 64 bit register used to determine priority from DSCP field (6 bits) in the IP header.
			802.1p Priority
3-7	4	Port	Enable Port 802.1p Priority: Uses the 802.1p priority tag (3 bits) to determine frame priority.
2	7-0	Global	Priority Classification: Determines which tag values have high priority.
			Per Port Priority
3-7	3	Port	Enable Port Priority: Determines which ports have high priority traffic.

Table 3. Priority Control

VLAN Operation

The VLAN's are setup by programming the VLAN Mask Registers in the EEPROM. The perspective of the VLAN is from the input port and which output ports it sees directly through the switch. For example if port 1 only participated in a VLAN with ports 2 and 5 then one would set bits 1 and 4 in register 8 (Port 1 VLAN Mask Register). Note that different ports can be setup independently. An example of this would be where a router is connected to port 5 and each of the other ports would work autonomously. In this configuration ports 1 through 4 would only set the mask for port 5 and port 5 would set the mask for ports 1 through 4. In this way the router could see all ports and each of the other individual ports would only communicate with the router.

All multicast and broadcast frames adhere to the VLAN configuration. Unicast frame treatment is a function of register 5 bit 6. If this bit is set then unicast frames only see ports within their VLAN. If this bit is cleared unicast frames can traverse VLAN's.

VLAN tags can be added or removed on a per port basis. Further, there are provisions to specify the tag value to be inserted on a per port basis.

The table below briefly summarizes VLAN features. For more detailed settings see *"EEPROM Memory Map"* section.

Register(s)	Bit(s)	Global/Port	Description
3-7	2	Port	Insert VLAN Tags: If specified, will add VLAN tags to frames without existing tags
3-7	1	Port	Strip VLAN Tags: If specified, will remove VLAN tags from frames if they exist
5	6	Global	VLAN Enforcement: Allows unicast frames to adhere or ignore the VLAN configuration
8-12	4-0	Port	VLAN Mask Registers: Allows configuration of individual VLAN grouping. Note reserved bit in each of the registers (sliding position).
13-22	7-0	Port	VLAN Tag Insertion Values: Specifies the VLAN tag to be inserted if enabled (see above)

Table 4. VLAN Control

Other Programmable Features

Other available features include port aggregation, frame length enforcement and broadcast storm protection. Additionally the MAC source address can be programmed as used in flow control frames.

Port aggregation is used when additional bandwidth is desired to a specific path or end unit. This can turn a 100Mb path into either a 200Mb or 400Mb path. This allows high throughput where needed.

The frame length enforcement control allows filtering of frames that exceed 1518 bytes for non-VLAN or 1522 bytes for VLAN. The maximum frame size is capped at 1536 bytes. Of course minimum frame size of 64 bytes is always enforced.

The broadcast storm control prevents excessive broadcast frames from bogging down the switch. Broadcast frames are restricted to their VLAN and can further be controlled down to as low as 3% of the traffic. The maximum level for broadcast frames is at 25% when the broadcast storm control is enabled. The feature is generally enabled by strapping LED[3][2] at reset time.

The table below briefly summarizes other programmable features. For more detailed settings see *"EEPROM Memory Map"* section.

Register(s)	Bit(s)	Global/Port	Description
4	7-6	Global	Port Trunk Control: Allows ports to be aggregated together for higher throughput.
6	6	Global	Maximum Frame Length Enforcement: Allows frames up to 1536 bytes to be passed.
7	7-6	Global	Broadcast Storm Protection: Allows as much as 25% to as little as 3% broadcast frames.
31-36	7-0	Global	Station MAC Address: Used as source address for MAC control frames as used in full duplex flow control mechanisms.

Table 5. Misc Control

EEPROM Operation

The EEPROM interface utilizes 2 pins that provide a clock and a serial data path. As part of the initialization sequence, the KS8995E reads the contents of the EEPROM and loads the values into the appropriate registers. Note that the first two bytes in the EEPROM must be "55" and "95" respectively for the loading to occur properly. If these first two values are not correct, all other data will be ignored.

Data start and stop conditions are signaled on the data line as a state transition during clock high time. A high to low transition indicates start of data and a low to high transition indicates a stop condition. The actual data that traverses the serial line changes during the clock low time.

The KS8995E EEPROM interface is compatible with the Atmel AT24C01A part. Further timing and data sequences can be found in the Atmel AT24C01A specification.

Compatibility with the KS8995

The KS8995E supports the same I/O strapping and I/O configuration as the KS8995 for existing designs. Two I/O definition changes were necessary to provide for the EEPROM interface. This effects pins 56 and 57 and relates to the switch core clocking. Switch core clocking is now fixed at 42MHz and is no longer adjustable.

EEPROM Memory Map

Register	Bit(s)	Description	Default (chip) Value
0	7-0	Signature byte 1. Value = “55”	0x55
1	7-0	Signature byte 2. Value = “95”	0x95
Priority Classification Control - 802.1p tag field			
2	7	1 = State “111” is high priority 0 = State “111” is low priority	0
2	6	1 = State “110” is high priority 0 = State “110” is low priority	0
2	5	1 = State “101” is high priority 0 = State “101” is low priority	0
2	4	1 = State “100” is high priority 0 = State “100” is low priority	0
2	3	1 = State “011” is high priority 0 = State “011” is low priority	0
2	2	1 = State “010” is high priority 0 = State “010” is low priority	0
2	1	1 = State “001” is high priority 0 = State “001” is low priority	0
2	0	1 = State “000” is high priority 0 = State “000” is low priority	0
Control Register 1			
3	7-6	Priority control scheme (all ports) 00 = Transmit all high priority before any low priority 01= Transmit high and low priority at a 10:1 ratio 10 = Transmit high and low priority at a 5:1 ratio 11 = Transmit high and low priority at a 2:1 ratio	00
3	5	TOS priority classification enable for port 1 1 = Enable, 0 = Disable	0
3	4	802.1p priority classification enable for port 1 1 = Enable, 0 = Disable	0
3	3	Port based priority classification for port 1 1 = Enable, 0 = Disable	0
3	2	Insert VLAN tags for port 1 if non-existent 1 = Enable, 0 = Disable	0
3	1	Strip VLAN tags for port 1 if existent 1 = Enable, 0 = Disable	0
3	0	Enable high and low output priority queues for port 1 1 = Enable, 0 = Disable	0
Control Register 2			
4	7-6	Port trunk (link aggregation) control 00 = Disable 01 = Ports 1 and 2 are trunked 10 = Ports 1 and 2 are trunked, ports 3 and 4 are trunked 11 = Ports 1, 2, 3, 4 are trunked	00
4	5	TOS priority classification enable for port 2 1 = Enable, 0 = Disable	0
4	4	802.1p priority classification enable for port 2 1 = Enable, 0 = Disable	0
4	3	Port based priority classification for port 2 1 = Enable, 0 = Disable	0

Register	Bit(s)	Description	Default (chip) Value
4	2	Insert VLAN tags for port 2 if non-existent 1 = Enable, 0 = Disable	0
4	1	Strip VLAN tags for port 2 if existent 1 = Enable, 0 = Disable	0
4	0	Enable high and low output priority queues for port 2 1 = Enable, 0 = Disable	0
Control Register 3			
5	7	Priority buffer reserve for high priority traffic 1 = Reserve 12KB of buffer space for high priority 0 = None reserved	0
5	6	VLAN enforcement 1 = All unicast frames adhere to VLAN configuration 0 = Unicast frames ignore VLAN configuration	0
5	5	TOS priority classification enable for port 3 1 = Enable, 0 = Disable	0
5	4	802.1p priority classification enable for port 3 1 = Enable, 0 = Disable	0
5	3	Port based priority classification for port 3 1 = Enable, 0 = Disable	0
5	2	Insert VLAN tags for port 3 if non-existent 1 = Enable, 0 = Disable	0
5	1	Strip VLAN tags for port 3 if existent 1 = Enable, 0 = Disable	0
5	0	Enable high and low output priority queues for port 3 1 = Enable, 0 = Disable	0
Control Register 4			
6	7	Reserved	0
6	6	Maximum frame length enforcement 1 = Pass non-VLAN frames between 64-1518 bytes and VLAN frames between 64-1522 bytes 0 = Pass any frame between 64-1536 bytes	1
6	5	TOS priority classification enable for port 4 1 = Enable, 0 = Disable	0
6	4	802.1p priority classification enable for port 4 1 = Enable, 0 = Disable	0
6	3	Port based priority classification for port 4 1 = Enable, 0 = Disable	0
6	2	Insert VLAN tags for port 4 if non-existent 1 = Enable, 0 = Disable	0
6	1	Strip VLAN tags for port 4 if existent 1 = Enable, 0 = Disable	0
6	0	Enable high and low output priority queues for port 4 1 = Enable, 0 = Disable	0
Control Register 5			
7	7-6	Broadcast storm protection control 00 = Allow 25% broadcast frames 01 = Allow 12% broadcast frames 10 = Allow 6% broadcast frames 11 = Allow 3% broadcast frames	00
7	5	TOS priority classification enable for port 5 1 = Enable, 0 = Disable	0

Register	Bit(s)	Description	Default (chip) Value
7	4	802.1p priority classification enable for port 5 1 = Enable, 0 = Disable	0
7	3	Port based priority classification for port 5 1 = Enable, 0 = Disable	0
7	2	Insert VLAN tags for port 5 if non-existent 1 = Enable, 0 = Disable	0
7	1	Strip VLAN tags for port 5 if existent 1 = Enable, 0 = Disable	0
7	0	Enable high and low output priority queues for port 5 1 = Enable, 0 = Disable	0
Port 1 VLAN Mask Register			
8	7-5	Reserved	000
8	4	Port 5 inclusion 1 = Port 5 in the same VLAN as port 1 0 = Port 5 not in the same VLAN as port 1	1
8	3	Port 4 inclusion 1 = Port 4 in the same VLAN as port 1 0 = Port 4 not in the same VLAN as port 1	1
8	2	Port 3 inclusion 1 = Port 3 in the same VLAN as port 1 0 = Port 3 not in the same VLAN as port 1	1
8	1	Port 2 inclusion 1 = Port 2 in the same VLAN as port 1 0 = Port 2 not in the same VLAN as port 1	1
8	0	Reserved	1
Port 2 VLAN Mask Register			
9	7-5	Reserved	000
9	4	Port 5 inclusion 1 = Port 5 in the same VLAN as port 2 0 = Port 5 not in the same VLAN as port 2	1
9	3	Port 4 inclusion 1 = Port 4 in the same VLAN as port 2 0 = Port 4 not in the same VLAN as port 2	1
9	2	Port 3 inclusion 1 = Port 3 in the same VLAN as port 2 0 = Port 3 not in the same VLAN as port 2	1
9	1	Reserved	1
9	0	Port 1 inclusion 1 = Port 1 in the same VLAN as port 2 0 = Port 1 not in the same VLAN as port 2	1
Port 3 VLAN Mask Register			
10	7-5	Reserved	000
10	4	Port 5 inclusion 1 = Port 5 in the same VLAN as port 3 0 = Port 5 not in the same VLAN as port 3	1
10	3	Port 4 inclusion 1 = Port 4 in the same VLAN as port 3 0 = Port 4 not in the same VLAN as port 3	1
10	2	Reserved	1

Register	Bit(s)	Description	Default (chip) Value
10	1	Port 2 inclusion 1 = Port 2 in the same VLAN as port 3 0 = Port 2 not in the same VLAN as port 3	1
10	0	Port 1 inclusion 1 = Port 1 in the same VLAN as port 3 0 = Port 1 not in the same VLAN as port 3	1
Port 4 VLAN Mask Register			
11	7-5	Reserved	000
11	4	Port 5 inclusion 1 = Port 5 in the same VLAN as port 4 0 = Port 5 not in the same VLAN as port 4	1
11	3	Reserved	1
11	2	Port 3 inclusion 1 = Port 3 in the same VLAN as port 4 0 = Port 3 not in the same VLAN as port 4	1
11	1	Port 2 inclusion 1 = Port 2 in the same VLAN as port 4 0 = Port 2 not in the same VLAN as port 4	1
11	0	Port 1 inclusion 1 = Port 1 in the same VLAN as port 4 0 = Port 1 not in the same VLAN as port 4	1
Port 5 VLAN Mask Register			
12	7-5	Reserved	000
12	4	Reserved	1
12	3	Port 4 inclusion 1 = Port 4 in the same VLAN as port 5 0 = Port 4 not in the same VLAN as port 5	1
12	2	Port 3 inclusion 1 = Port 3 in the same VLAN as port 5 0 = Port 3 not in the same VLAN as port 5	1
12	1	Port 2 inclusion 1 = Port 2 in the same VLAN as port 5 0 = Port 2 not in the same VLAN as port 5	1
12	0	Port 1 inclusion 1 = Port 1 in the same VLAN as port 5 0 = Port 1 not in the same VLAN as port 5	1
Port 1 VLAN Tag Insertion Value Registers			
13	7-5	User priority [2:0]	000
13	4	CFI	0
13	3-0	VID [11:8]	0x0
14	7-0	VID [7:0]	0x00
Port 2 VLAN Tag Insertion Value Registers			
15	7-5	User priority [2:0]	000
15	4	CFI	0
15	3-0	VID [11:8]	0x0
16	7-0	VID [7:0]	0x00

Register	Bit(s)	Description	Default (chip) Value
Port 3 VLAN Tag Insertion Value Registers			
17	7-5	User priority [2:0]	000
17	4	CFI	0
17	3-0	VID [11:8]	0x0
18	7-0	VID [7:0]	0x00
Port 4 VLAN Tag Insertion Value Registers			
19	7-5	User priority [2:0]	000
19	4	CFI	0
19	3-0	VID [11:8]	0x0
20	7-0	VID [7:0]	0x00
Port 5 VLAN Tag Insertion Value Registers			
21	7-5	User priority [2:0]	000
21	4	CFI	0
21	3-0	VID [11:8]	0x0
22	7-0	VID [7:0]	0x00
Diff Serv Code Point Registers			
23	7-0	DSCP[63:56]	0x00
24	7-0	DSCP[55:48]	0x00
25	7-0	DSCP[47:40]	0x00
26	7-0	DSCP[39:32]	0x00
27	7-0	DSCP[31:24]	0x00
28	7-0	DSCP[23:16]	0x00
29	7-0	DSCP[15:8]	0x00
30	7-0	DSCP[7:0]	0x00
Station MAC Address Registers (all ports - MAC control frames only)			
31	7-0	MAC address [47:40]	0x00
32	7-0	MAC address [39:32]	0x40
33	7-0	MAC address [31:24]	0x05
34	7-0	MAC address [23:16]	0x43
35	7-0	MAC address [15:8]	0x5E
36	7-0	MAC address [7:0]	0xFE

Note. The MAC address is reset to the value in the above table, but can set to any value via the EEPROM interface. This MAC address is used as the source address in MAC control frames that execute flow control between link peers.

Absolute Maximum Ratings (Note 1)

Supply Voltage
(V_{DDAR}, V_{DDAP}, V_{DDC}) ..... –0.5V to +2.4V
(V_{DDAT}, V_{DDIO}) ..... –0.5V to +4.0V
Input Voltage ..... –0.5V to +4.0V
Output Voltage ..... –0.5V to +4.0V
Lead Temperature (soldering, 10 sec.) ..... 270°C
Storage Temperature (T_S) ..... –55°C to +150°C

Operating Ratings (Note 2)

Supply Voltage (V_{IN}) ..... +2.375V to +2.625V
Ambient Temperature (T_A) ..... –0°C to +70°C
Package Thermal Resistance **(Note 3)**
PQFP (θ_{JA}) No Air Flow ..... 42.91°C/W

Electrical Characteristics (Note 4)

V_{DD} = 2.5V to 2.75V; T_A = 0°C to +70°C; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Supply Voltage		2.375	2.5	2.625	V
Total Supply Current (including TX output driver current)						
I_{DD1}	Normal 100BaseTX			0.5		A
I_{DD2}	Normal 10BaseT			0.7		A
TTL Inputs						
V_{IH}	Input High Voltage		V_{DD} (I/O) –0.8			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current	V_{IN} = GND ~ V_{DD}	–10		10	µA
TTL Outputs						
V_{OH}	Output High Voltage	I_{OH} = –4mA	V_{DD} (I/O) –0.4			V
V_{OL}	Output Low Voltage	I_{OL} = 4mA			0.4	V
$\|I_{OZ}\|$	Output Tri-State Leakage				10	µA
100BaseTX Receive						
V_B	RXP/RXM Input Bias Voltage			1.9		V
100BaseTX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	50Ω from each output to V_{DD}	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	50Ω from each output to V_{DD}			2	%
t_r, t_t	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance				0.5	ns
	Duty Cycle Distortion				±0.5	ns
	Overshoot				5	%
V_{SET}	Reference Voltage of ISET			0.75		V
	Output Jitters	Peak-to-peak		0.7	1.4	ns
10BaseTX Receive						
V_{SQ}	Squelch Threshold	5MHz square wave		400		mV

Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to an appropriate logic voltage level (Ground to V_{DD}).

Note 3. No HS (heat spreader) in package.

Note 4. Specification for packaged product only.

Symbol	Parameter	Condition	Min	Typ	Max	Units
10BaseTX Transmit (measured differentially after 1:1 transformer)						
V_P	Peak Differential Output Voltage	50Ω from each output to V_{DD}		2.3		V
	Jitters Added	50Ω from each output to V_{DD}			±3.5	ns
	Rise/Fall Time			25		ns

Timing Diagrams

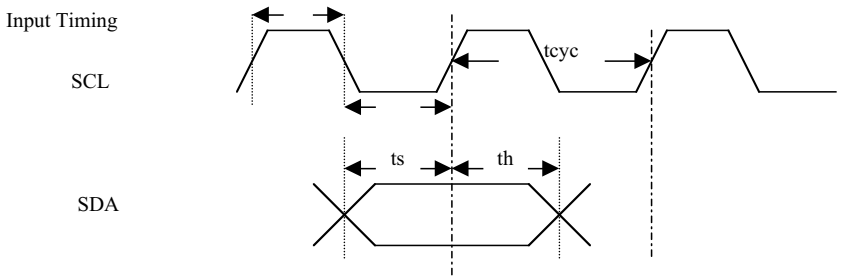


Figure 2. EEPROM Input Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{CYC}	Clock Cycle		12288		ns
t_S	Set-Up Time	10			ns
t_H	Hold Time	5			ns

Table 6. EEPROM Input Timing Parameters

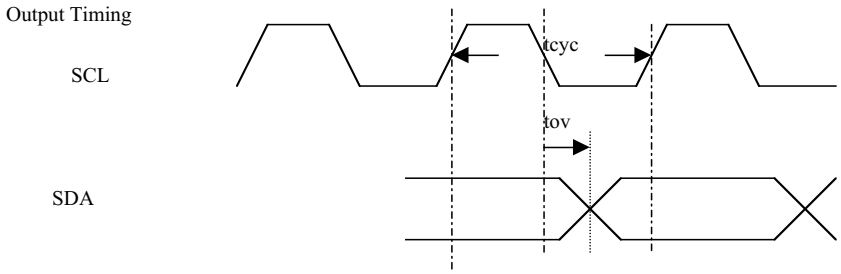


Figure 3. EEPROM Output Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{CYC}	Clock Cycle		12288		ns
t_{OV}	Output Valid	3056	3072	3088	ns

Table 7. EEPROM Output Timing Parameters

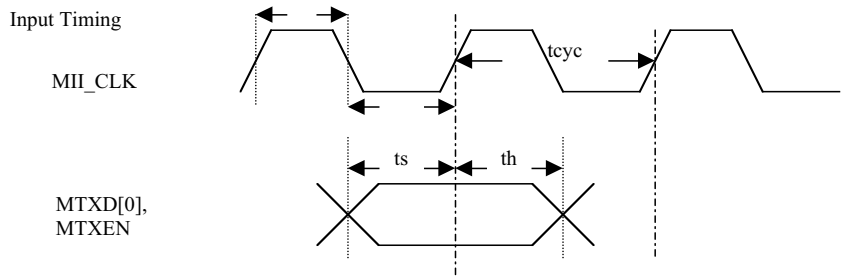


Figure 4. SNI (7-Wire) Input Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{CYC}	Clock Cycle		100		ns
t_S	Set-Up Time	10			ns
t_H	Hold Time	0			ns

Table 8. SNI (7-Wire) Input Timing Parameters

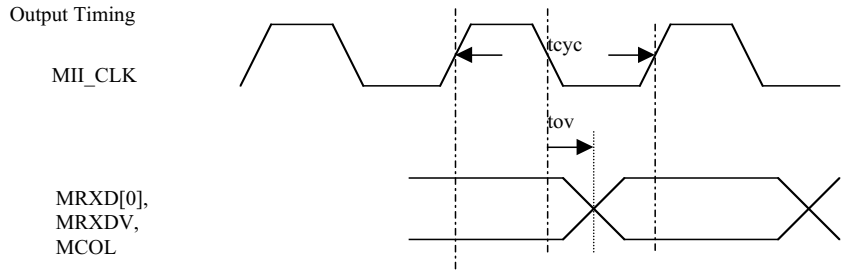


Figure 5. SNI (7-Wire) Output Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{CYC}	Clock Cycle		100		ns
t_{OV}	Output Valid	0	3	6	ns

Table 9. SNI (7-Wire) Output Timing Parameters

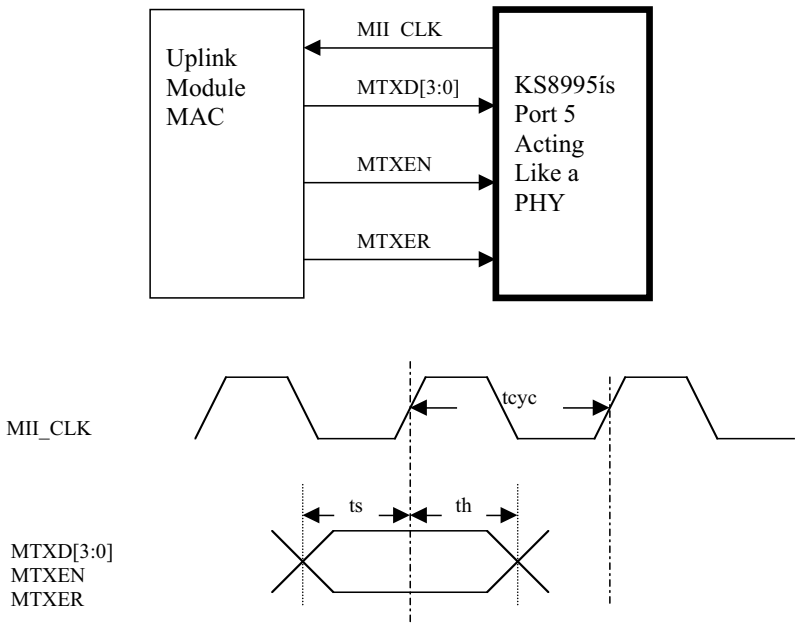


Figure 6. Reverse MII Timing–Receive Data from MII

Symbol	Parameter		Min	Typ	Max	Units
t_{CYC}	Clock Cycle	(100BaseT) (10BaseT)		40 400		ns
t_S	Set-Up Time		10			ns
t_H	Hold Time		0			ns

Table 10. Reverse MII Timing–Receive Data from MII Parameters

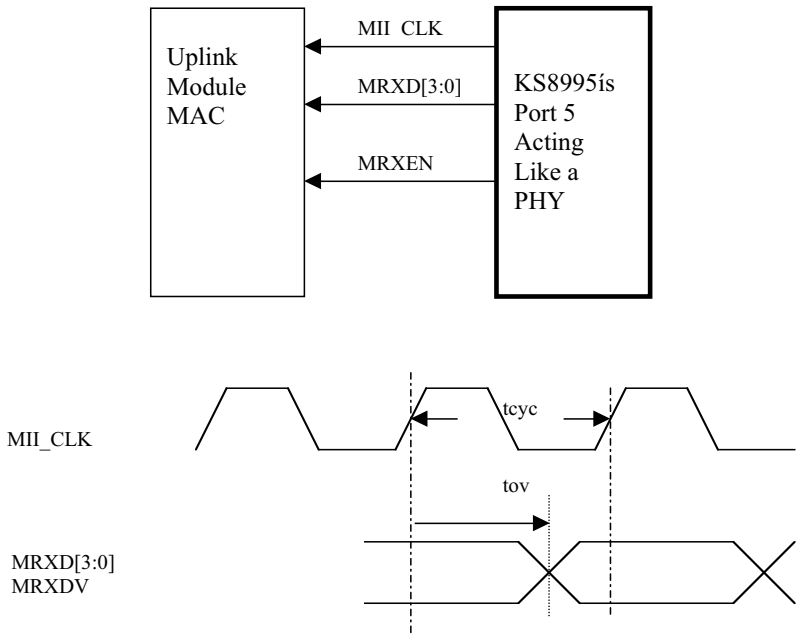


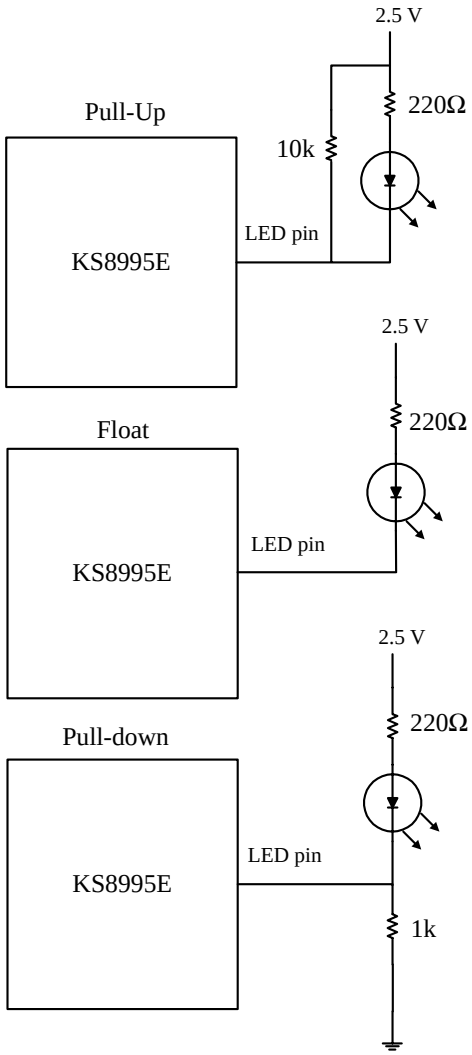
Figure 7. Reverse MII Timing–Transmit Data to MII

Symbol	Parameter		Min	Typ	Max	Units
t_{CYC}	Clock Cycle	(100BaseT) (10BaseT)		40 400		ns
t_{OV}	Output Valid		18	25	28	ns

Table 11. Reverse MII Timing–Transmit Data to MII Parameters

Reference Circuit

See *"I/O Description"* section for pull-up/pull-down and float information.



Reference circuits for unmanaged programming through LED ports

Figure 8. Unmanaged Programming Circuit

The following transformer vendors provide pin-to-pin compatible parts for Micrel's device:

Magnetics Vendor	Transformer Only		Integrated RJ4 & 5 Transformer
	Quad	Single	
Transformer www.trans-power.com	HB826-2	HB726-1	1x8 (4-port) RJG4-726 1x5 (5-port) RJG5-726
Pulse www.pulse.com	H1164	H1102	
Bel Fuse	558-5999-Q9	S558-5999-U7	
YCL	PH406466	PT163020	

Table 12. Magnetic Vendor List

4B/5B Coding

In 100BaseTX and 100BaseFX the data and frame control are encoded in the transmitter (and decoded in the receiver) using a 4B/5B code. The extra code space is required to encode extra control (frame delineation) points. It is also used to reduce run length as well as supply sufficient transitions for clock recovery. The table below provides the translation for the 4B/5B coding.

Code Type	4B Code	5B Code	Value
Data	0000	11110	Data value 0
	0001	01001	Data value 1
	0010	10100	Data value 2
	0011	10101	Data value 3
	0100	01010	Data value 4
	0101	01011	Data value 5
	0110	01110	Data value 6
	0111	01111	Data value 7
	1000	10010	Data value 8
	1001	10011	Data value 9
	1010	10110	Data value A
	1011	10111	Data value B
	1100	11010	Data value C
	1101	11011	Data value D
	1110	11100	Data value E
	1111	11101	Data value F
Control	Not defined	11111	Idle
	0101	11000	Start delimiter part 1
	0101	10001	Start delimiter part 2
	Not defined	01101	End delimiter part 1
	Not defined	00111	End delimiter part 2
	Not defined	00100	Transmit error
Invalid	Not defined	00000	Invalid code
	Not defined	00001	Invalid code
	Not defined	00010	Invalid code
	Not defined	00011	Invalid code
	Not defined	00101	Invalid code
	Not defined	00110	Invalid code
	Not defined	01000	Invalid code
	Not defined	01100	Invalid code
	Not defined	10000	Invalid code
	Not defined	11001	Invalid code

Table 13. 4B/5B Coding

MLT3 Coding

For 100BaseTX operation the NRZI (Non-Return to Zero Invert on ones) signal is line coded as MLT3. The net result of using MLT3 is to reduce the EMI (Electro Magnetic Interference) of the signal over twisted pair media. In NRZI coding, the level changes from high to low or low to high for every “1” bit. For a “0” bit there is no transition. MLT3 line coding transitions through three distinct levels. For every transition of the NRZI signal the MLT3 signal either increments or decrements depending on the current state of the signal. For instance if the MLT3 level is at its lowest point the next two NRZI transitions will change the MLT3 signal initially to the middle level followed by the highest level (second NRZI transition). On the next NRZI change, the MLT3 level will decrease to the middle level. On the following transition of the NRZI signal the MLT3 level will move to the lowest level where the cycle repeats. The diagram below describes the level changes. Note that in the actual 100BaseTX circuit there is a scrambling circuit and that scrambling is not shown in this diagram.

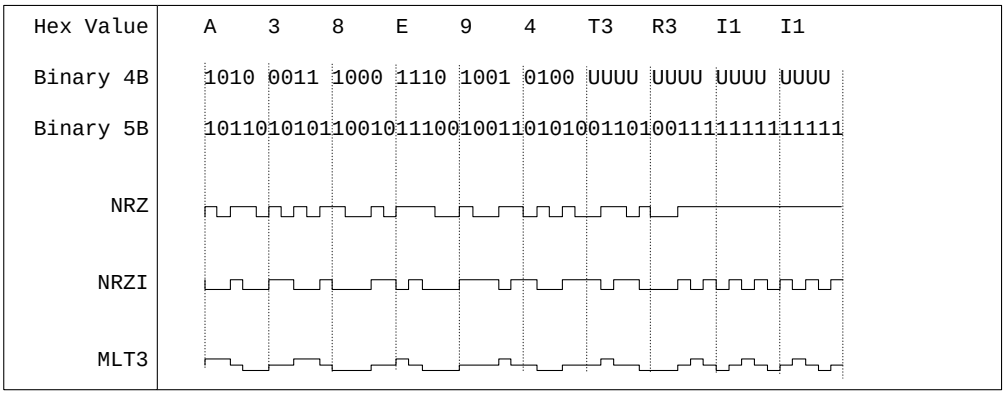


Figure 9. MLT3 coding

The MAC (Media Access Control) fields are described in the table below.

Field	Octect Length	Description
Preamble/SFD	8	Preamble and Start of Frame Delimiter
DA	6	48-bit Destination MAC Address
SA	6	48-bit Source MAC Address
802.1p tag	4	VLAN and priority tag (optional)
Length	2	Frame Length
Protocol/Data	46 to 1500	Higher Layer Protocol and Frame Data
Frame CRC	4	32-bit Cyclical Redundancy Check
ESD	1	End of Stream Delimiter
Idle	Variable	Inter Frame Idles

Table 14. MAC Frame for 802.3

802.1q VLAN and 802.1p Priority Frame

The 3-bit of 802.1p priority is embedded into the 802.1q VLAN frame as described below:

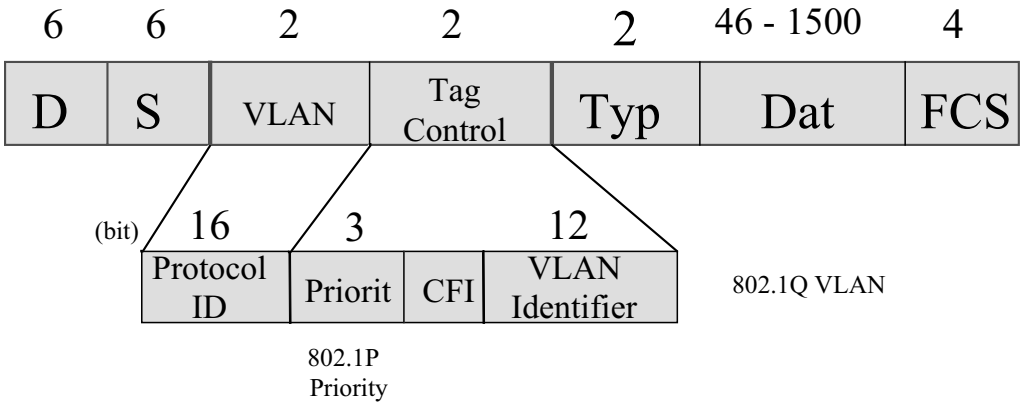


Figure 10. 802.1q and 802.1p Frame Format

Selection of Isolation Transformer(Note 1)

One simple 1:1 isolation transformer is needed at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements. The following table gives recommended transformer characteristics.

Characteristics Name	Value	Test Condition
Turns Ratio	1 CT : 1 CT	
Open-Circuit Inductance (min.)	350µH	100mV, 100KHz, 8mA
Leakage Inductance (max.)	0.4µH	1MHz (min.)
Inter-Winding Capacitance (max.)	12pF	
D.C. Resistance (max.)	0.9Ω	
Insertion Loss (max.)	1.0dB	0MHz to 65MHz
HIPOT (min.)	1500Vrms	

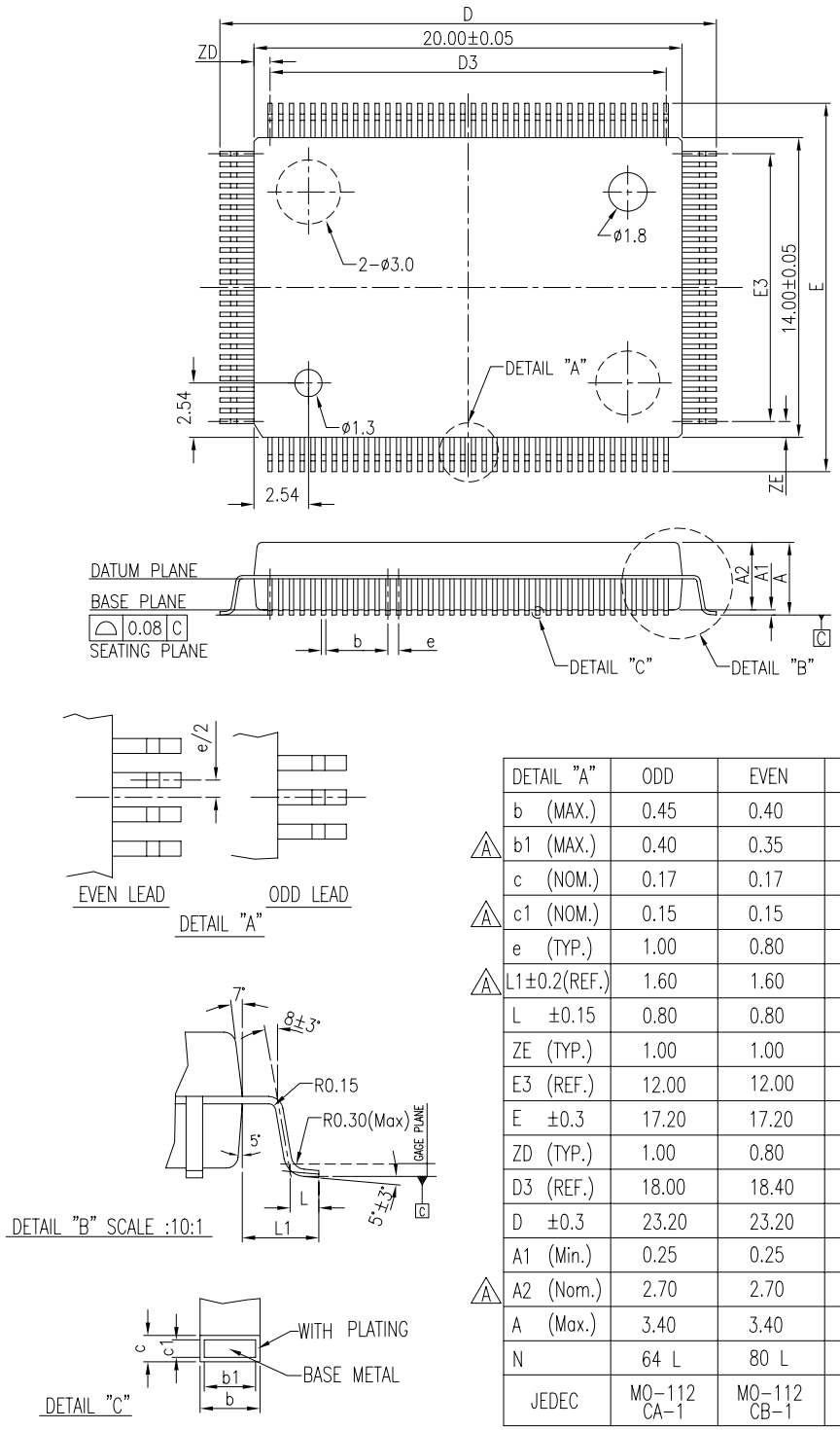
Note 1. The IEEE 802.3u standard for 100BaseTX assumes a transformer loss of 0.5dB. For the transmit line transformer, insertion loss of up to 1.3dB can be compensated by increasing the line drive current by means of reducing the ISET resistor value.

Selection of Reference Crystal

An oscillator or crystal with the following typical characteristics is recommended.

Characteristics Name	Value	Units
Frequency	25.00000	MHz
Frequency Tolerance (max.)	±100	ppm
Jitter (max.)	150	ps(pk-pk)

Package Information



	DETAIL "A"	ODD	EVEN	EVEN	EVEN
	b (MAX.)	0.45	0.40	0.35	0.25
A	b1 (MAX.)	0.40	0.35	0.30	0.20
	c (NOM.)	0.17	0.17	0.17	0.17
A	c1 (NOM.)	0.15	0.15	0.15	0.15
	e (TYP.)	1.00	0.80	0.65	0.50
A	L1±0.2(REF.)	1.60	1.60	1.60	1.60
	L ±0.15	0.80	0.80	0.80	0.80
	ZE (TYP.)	1.00	1.00	0.83	0.75
	E3 (REF.)	12.00	12.00	12.35	12.50
	E ±0.3	17.20	17.20	17.20	17.20
	ZD (TYP.)	1.00	0.80	0.58	0.75
	D3 (REF.)	18.00	18.40	18.85	18.50
	D ±0.3	23.20	23.20	23.20	23.20
	A1 (Min.)	0.25	0.25	0.25	0.25
A	A2 (Nom.)	2.70	2.70	----	----
	A (Max.)	3.40	3.40	3.40	3.40
	N	64 L	80 L	100 L	128L
	JEDEC	MO-112 CA-1	MO-112 CB-1	CC-1	----

128-Pin PQFP (PQ)

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