

This is a short form datasheet and is intended to provide an overview only. Additional details are available from IDT. Contact information may be found on the last page.

## HIGHLIGHTS

- DPLL1 and DPLL2 can be used on line cards to manage the generation of synchronous port clocks and IEEE 1588 synchronization signals based on multiple system backplane references
- DPLL3 can be used on line cards to select incoming line clocks for use on system backplanes; it can also be used for general purpose timing applications
- APLL1 and APLL2 generate clocks with jitter < 1 ps RMS (12 kHz to 20 MHz) for: 1000BASE-T and 1000BASE-X ports and to generate IEEE 1588 time stamp clocks and 1 pulse per second (PPS) signals
- Fractional-N input dividers support a wide range of reference frequencies
- The device can be configured from an external EEPROM after reset

## FEATURES

- Differential reference inputs (IN1 to IN4) accept clock frequencies between 2 kHz and 650 MHz
- Single ended inputs (IN5 to IN6) accept reference clock frequencies between 2 kHz and 162.5 MHz
- Loss of Signal (LOS) pins (LOS0 to LOS3) can be assigned to any clock reference input
- Reference monitors qualify/disqualify references depending on activity, frequency and LOS pins
- Automatic reference selection state machines select the active reference for each DPLL based on the reference monitors, priority tables, revertive and non-revertive settings and other programmable settings
- Fractional-N input dividers enable the DPLLs to lock to a wide range of reference clock frequencies including: 10/100/1000 Ethernet, 10G Ethernet, OTN, SONET/SDH, PDH, TDM, GSM and GNSS frequencies
- Any reference inputs (IN1 to IN6) can be designated as external sync pulse inputs (1 PPS, 2 kHz, 4 kHz or 8 kHz) associated with a selectable reference clock input
- FRSYNC\_8K\_1PPS and MFRSYNC\_2K\_1PPS output sync pulses that are aligned with the selected external input sync pulse input and frequency locked to the associated reference clock input
- DPLL1 and DPLL2 can be configured with bandwidths between 18 Hz and 567 Hz
- DPLL1 and DPLL2 lock to input references with frequencies between 2 kHz and 650 MHz
- DPLL3 locks to input references with frequencies between 8 kHz and 650 MHz
- DPLL1 and DPLL2 generate clocks with PDH, TDM, GSM, CPRI/OBSAI, 10/100/1000 Ethernet and GNSS frequencies; these clocks are directly available on OUT1 and OUT8
- DPLL3 generates N x 8 kHz clocks up to 100 MHz that are output on OUT9 and OUT10
- APLL1 and APLL2 can be connected to DPLL1 and DPLL2
- APLL1 and APLL2 generate 10/100/1000 Ethernet, 10G Ethernet, or SONET/SDH frequencies

- Any of eight common XO frequencies can be used for the System Clock: 10 MHz, 12.8 MHz, 13 MHz, 19.44 MHz, 20 MHz, 24.576 MHz, 25 MHz or 30.72 MHz
- The I2C slave, SPI or the UART interface can be used by a host processor to access the control and status registers
- The I2C master interface can automatically load a device configuration from an external EEPROM after reset
- Differential outputs OUT3 to OUT6 output clocks with frequencies between 1 PPS and 650 MHz
- Single ended outputs OUT1, OUT2, OUT7, and OUT8 output clocks with frequencies between 1 PPS and 125 MHz
- Single ended outputs OUT9 and OUT10 output clocks N\*8 kHz multiples up to 100 MHz
- DPLL1 and DPLL2 support independent programmable delays for each of IN1 to IN16; the delay for each input is programmable in steps of 0.61 ns with a range of  $\pm 78$  ns
- The input to output phase delay of DPLL1 and DPLL2 is programmable in steps of 0.0745 ps with a total range of  $\pm 20$   $\mu$ s
- The clock phase of each of the output dividers for OUT1 to OUT8 is individually programmable in steps of  $\sim 200$  ps with a total range of  $\pm 180^\circ$
- 1149.1 JTAG Boundary Scan
- 72-pin QFN green package

## APPLICATIONS

- Synchronous clock generation for 10/40G and lower rate, Ethernet, PON OLT and SONET/SDH line card
- Access routers, edge routers, core routers
- Carrier Ethernet switches
- Multiservice access platforms
- PON OLT
- LTE eNodeB

## DESCRIPTION

The 82P33724 Port Synchronizer for IEEE 1588 and Synchronous Ethernet provides tools to manage timing references, clock conversion and timing paths for IEEE 1588 and Synchronous Ethernet (SyncE). The device supports up to three independent timing paths for: IEEE 1588 clock generation; SyncE clock generation; and general purpose frequency translation. The device outputs low-jitter clocks that can directly synchronize Ethernet interfaces; as well as SONET/SDH and PDH interfaces and IEEE 1588 Time Stamp Units (TSUs).

The 82P33724 accepts four differential reference inputs and two single ended reference inputs that can operate at common Ethernet, SONET/SDH and PDH frequencies that range from 2 kHz to 650 MHz. The references are continually monitored for loss of signal and for frequency offset per user programmed thresholds. All of the references are available to all three Digital PLLs (DPLLs). The active reference for each DPLL is determined by forced selection or by automatic selection based on user programmed priorities, locking allowances, reference monitors, and LOS inputs.

The 82P33724 can accept a clock reference and an associated phase locked sync signal as a pair. DPLL1/DPLL2 can lock to the clock reference and align the frame sync and multi-frame sync outputs with the paired sync input. The device allows any of the differential or single ended reference inputs to be configured as sync inputs that can be associated with any of the other differential or single ended reference inputs. The input sync signals can have a frequency of 1 PPS, 2 kHz, 4kHz or 8 kHz. This feature enables DPLL1/DPLL2 to phase align its frame sync and multi-frame sync outputs with a sync input without the need use a low bandwidth setting to lock directly to the sync input.

The DPLLs support three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode the DPLLs synthesize clocks based on the system clock alone. In Locked mode the DPLLs filter reference clock jitter with the selected bandwidth. In Locked mode, the long-term output frequency accuracy is the same as the long term frequency accuracy of the selected input reference. In Holdover mode, the DPLL uses frequency data acquired while in Locked mode to generate accurate frequencies when input references are not available.

The 82P33724 requires a system clock for its reference monitors and other digital circuitry. The frequency accuracy of the system clock determines the frequency accuracy of the DPLLs in Free-Run mode. The frequency stability of the system clock determines the frequency stability of the DPLLs in Free-Run mode and in Holdover mode; and it affects the wander generation of the DPLLs in Locked mode.

DPLL1 and DPLL2 can be configured with a range of selectable filtering bandwidths from 18 Hz to 567 Hz. DPLL3 is a wideband (BW > 25Hz) frequency translator that can be used, for example, to convert a recovered SyncE clock to a 25MHz backplane clock.

Clocks generated by DPLL1 and DPLL2 can be passed through APLL1 or APLL2 which are LC based jitter attenuating Analog PLLs (APLLs). The output clocks generated by APLL1 and APLL2 are suitable for serial GbE and lower rate interfaces, and for IEEE 1588 time stamps clocks and 1 PPS signals.

All 82P33724 control and status registers are accessed through an I2C slave, SPI or the UART microprocessor interface. For configuring the DPLLs, APLL1 and APLL2, the I2C master interface can automatically load a configuration from an external EEPROM after reset.

## FUNCTIONAL BLOCK DIAGRAM

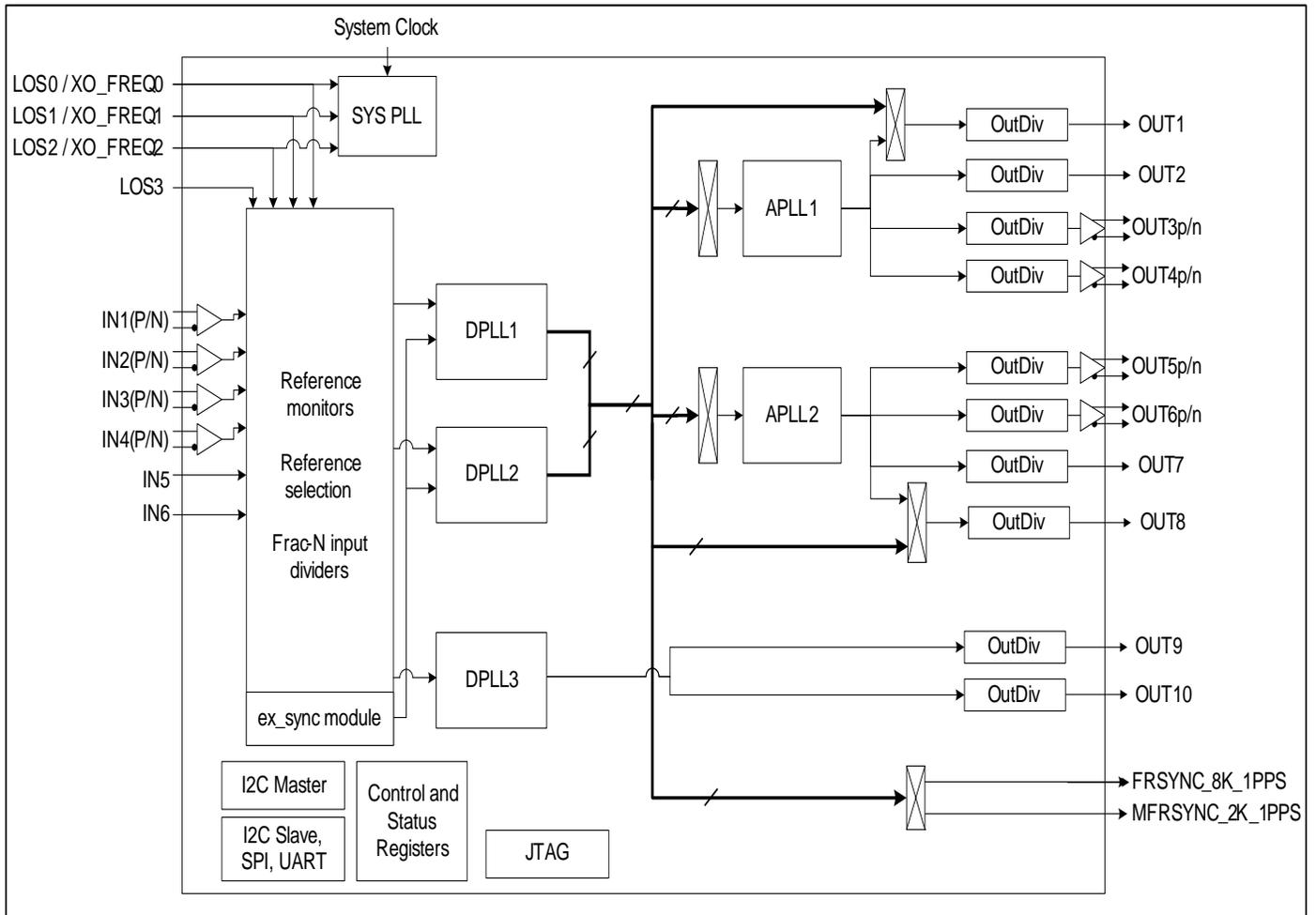
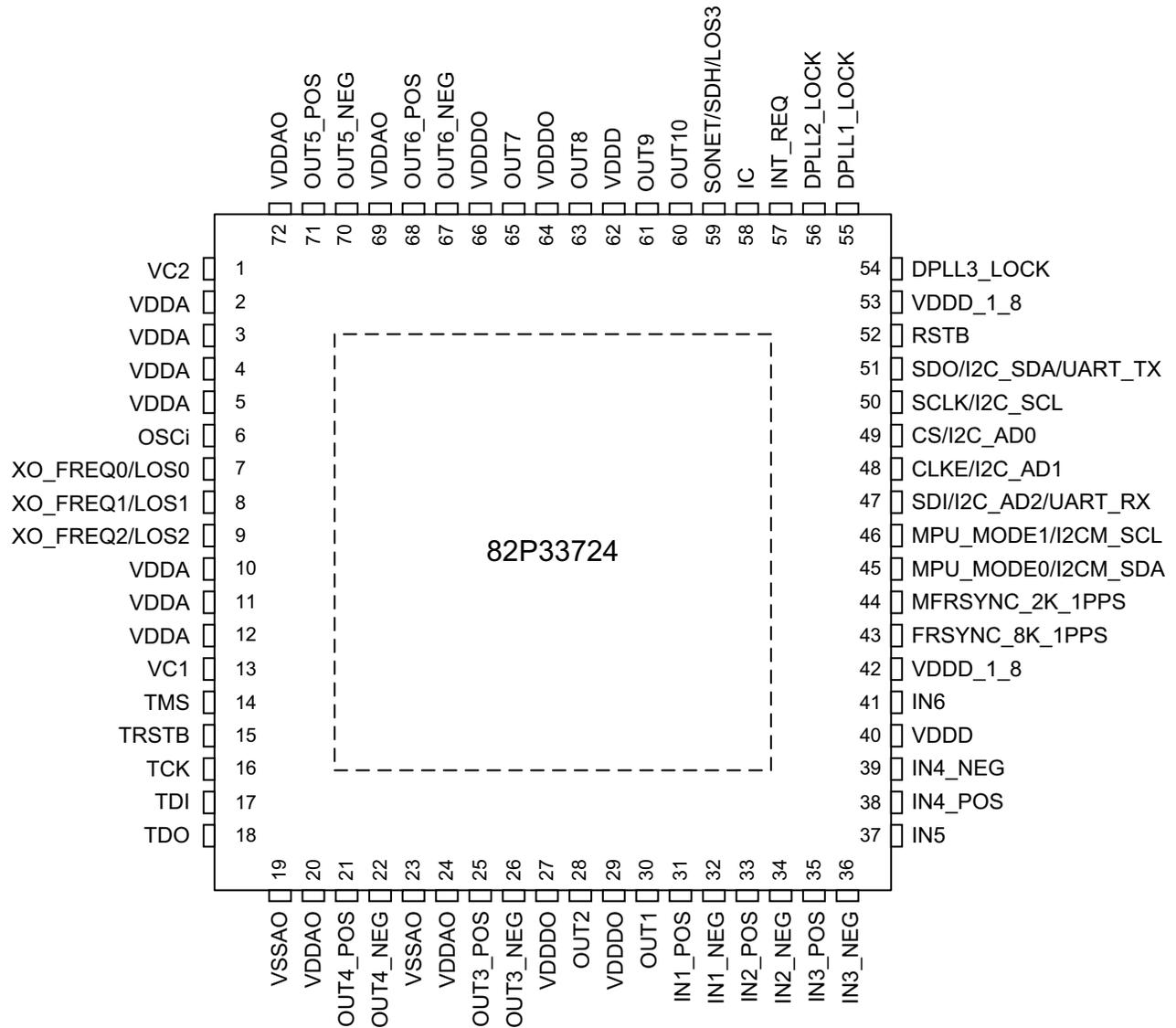


Figure 1. Functional Block Diagram

1 PIN ASSIGNMENT



**Figure 2. Pin Assignment (Top View)**

## 2 PIN DESCRIPTION

**Table 1: Pin Description**

Pin No.	Name	I/O	Type	Description
<b>Global Control Signal</b>				
6	OSCI	I	CMOS	<b>OSCI: Crystal Oscillator System Clock</b> A clock provided by a crystal oscillator is input on this pin. It is the system clock for the device. The oscillator frequency is selected via pins XO_FREQ0 - XO_FREQ2
59	SONET/SDH/ LOS3	I pull-down	CMOS	<b>SONET/SDH: SONET / SDH Frequency Selection</b> During reset, this pin determines the default value of the IN_SONET_SDH bit: High: The default value of the IN_SONET_SDH bit is '1' (SONET); Low: The default value of the IN_SONET_SDH bit is '0' (SDH). After reset, the value on this pin takes no effect. LOS3- This pin is used to disqualify input clocks.
52	RSTB	I pull-up	CMOS	<b>RSTB: Reset</b>
7 8 9	XO_FREQ0/ LOS0 XO_FREQ1/ LOS1 XO_FREQ2/ LOS2	I pull-down	CMOS	<b>XO_FREQ0 ~ XO_FREQ2:</b> These pins set the oscillator frequency. XO_FREQ[2:0] Oscillator Frequency (MHz) 000 10.000 001 12.800 010 13.000 011 19.440 100 20.000 101 24.576 110 25.000 111 30.720 <b>LOS0 ~ LOS2</b> - These pins are used to disqualify input clocks. After reset, this pin takes on the operation of LOS0-LOS2
<b>Input Clock and Frame Synchronization Input Signal</b>				
31 32	IN1_POS IN1_NEG	I	PECL/LVDS	<b>IN1_POS / IN1_NEG: Positive / Negative Input Clock 1</b> A reference clock is input on this pin. This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
33 34	IN2_POS IN2_NEG	I	PECL/LVDS	<b>IN2_POS / IN2_NEG: Positive / Negative Input Clock 2</b> A reference clock is input on this pin. This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
35 36	IN3_POS IN3_NEG	I	PECL/LVDS	<b>IN3_POS / IN3_NEG: Positive / Negative Input Clock 3</b> A reference clock is input on this pin. This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
38 39	IN4_POS IN4_NEG	I	PECL/LVDS	<b>IN4_POS / IN4_NEG: Positive / Negative Input Clock 4</b> A reference clock is input on this pin. This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
37	IN5	I pull-down	CMOS	<b>IN5: Input Clock 5</b> A reference clock is input on this pin. This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
41	IN6	I pull-down	CMOS	<b>IN6: Input Clock 6</b> A reference clock is input on this pin. This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
<b>Output Frame Synchronization Signal</b>				
43	FRSYNC _8K_1PPS	O	CMOS	<b>FRSYNC_8K_1PPS: 8 kHz Frame Sync Output</b> An 8 kHz signal or a 1PPS sync signal is output on this pin.
44	MFRSYNC _2K_1PPS	O	CMOS	<b>MFRSYNC_2K_1PPS: 2 kHz Multiframe Sync Output</b> A 2 kHz signal or a 1PPS sync signal is output on this pin.
<b>Output Clock</b>				
30 28	OUT1 OUT2	O	CMOS	<b>OUT1 ~ OUT2: Output Clock 1 ~ 2</b>

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
25 26	OUT3_POS OUT3_NEG	O	PECL/LVDS	<b>OUT3_POS / OUT3_NEG: Positive / Negative Output Clock 3</b> This output is set to LVDS by default. The LVDS output has internal 100 ohm termination.
21 22	OUT4_POS OUT4_NEG	O	PECL/LVDS	<b>OUT4_POS / OUT4_NEG: Positive / Negative Output Clock 4</b> This output is set to LVDS by default. The LVDS output has internal 100 ohm termination.
71 70	OUT5_POS OUT5_NEG	O	PECL/LVDS	<b>OUT5_POS / OUT5_NEG: Positive / Negative Output Clock 5</b> This output is set to LVDS by default. The LVDS output has internal 100 ohm termination.
68 67	OUT6_POS OUT6_NEG	O	PECL/LVDS	<b>OUT6_POS / OUT6_NEG: Positive / Negative Output Clock 6</b> This output is set to LVDS by default. The LVDS output has internal 100 ohm termination.
65 63	OUT7 OUT8	O	CMOS	<b>OUT7 ~ OUT8: Output Clock 7 ~ 8</b>
61 60	OUT9 OUT10	O	CMOS	<b>OUT9 ~ OUT10: Output Clock 9 ~ 10</b>
<b>Miscellaneous</b>				
13	VC1	O	Analog	<b>VC1: APLL1 VC Output</b> An external RC filter (a resistor in series with a capacitor to ground, and another capacitor in parallel) should be connected to this pin.
1	VC2	O	Analog	<b>VC2: APLL2 VC Output</b> An external RC filter (a resistor in series with a capacitor to ground, and another capacitor in parallel) should be connected to this pin.
<b>Lock Signal</b>				
54	DPLL3_LOCK	O	CMOS	DPLL3_LOCK This pin goes high when DPLL3 is locked
56	DPLL2_LOCK	O	CMOS	DPLL2_LOCK This pin goes high when DPLL2 is locked
55	DPLL1_LOCK	O	CMOS	DPLL1_LOCK This pin goes high when DPLL1 is locked
<b>Microprocessor Interface</b>				
57	INT_REQ	O Tri-state	CMOS	<b>INT_REQ: Interrupt Request</b> This pin is used as an interrupt request.
46 45	MPU_MODE1/ I2CM_SCL  MPU_MODE0/ I2CM_SDA	I/O pull-up	CMOS/ Open Drain	<b>MPU_MODE[1:0]: Microprocessor Interface Mode Selection</b> During reset, these pins determine the default value of the MPU_SEL_CNFG[1:0] bits as follows: 00: I2C mode 01: SPI mode 10: UART mode 11: I2C master (EEPROM) mode <b>I2CM_SCL: Serial Clock Line</b> In I2C master mode, the serial clock is output on this pin. <b>I2CM_SDA: Serial Data Input for I2C Master Mode</b> In I2C master mode, this pin is used as the for the serial data.
47	SDI/I2C_AD2/ UART_RX	I pull-down	CMOS	<b>SDI: Serial Data Input</b> In Serial mode, this pin is used as the serial data input. Address and data on this pin are serially clocked into the device on the rising edge of SCLK. <b>I2C_AD2: Device Address Bit 2</b> In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface. <b>UART_RX</b> In UART mode, this pin is used as the receive data (UART Receive)

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
48	CLKE/I2C_AD1	I pull-down	CMOS	<b>CLKE: SCLK Active Edge Selection</b> In Serial mode, this pin is an input, it selects the active edge of SCLK to update the SDO: High - The falling edge; Low - The rising edge.  <b>I2C_AD1: Device Address Bit 1</b> In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
49	CS/I2C_AD0	I pull-up	CMOS	<b>CS: Chip Selection</b> In Serial modes, this pin is an input. A transition from high to low must occur on this pin for each read or write operation and this pin should remain low until the operation is over.  <b>I2C_AD0: Device Address Bit 0</b> In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
50	SCLK/I2C_SCL	I pull-down	CMOS	<b>SCLK: Shift Clock</b> In Serial mode, a shift clock is input on this pin. Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the active edge of SCLK. The active edge is determined by the CLKE.  <b>I2C_SCL: Serial Clock Line</b> In I2C mode, the serial clock is input on this pin.
51	SDO/I2C_SDA/ UART_TX  I2C_SDA	I/O pull-up	CMOS/ Open Drain	<b>SDO: Serial Data Output</b> In Serial mode, this pin is used as the serial data output. Data on this pin is serially clocked out of the device on the active edge of SCLK.  <b>I2C_SDA: Serial Data Input/Output</b> In I2C mode, this pin is used as the input/output for the serial data.  <b>UART_TX:</b> In UART mode, this pin is used as the transmit data (UART Transmit)
<b>JTAG (per IEEE 1149.1)</b>				
14	TMS	I pull-up	CMOS	<b>TMS: JTAG Test Mode Select</b> The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.
15	TRSTB	I pull-up	CMOS	<b>TRSTB: JTAG Test Reset (Active Low)</b> A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.
16	TCK	I pull-down	CMOS	<b>TCK: JTAG Test Clock</b> The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.
17	TDI	I pull-up	CMOS	<b>TDI: JTAG Test Data Input</b> The test data are input on this pin. They are clocked into the device on the rising edge of TCK.
18	TDO	O tri-state	CMOS	<b>TDO: JTAG Test Data Output</b> The test data are output on this pin. They are clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning.
<b>Power &amp; Ground</b>				
2, 3, 4, 5, 10, 11, 12	VDDA	Power	-	VDDA: Analog Core Power - +3.3V DC nominal
20, 24, 69, 72	VDDAO	Power		VDDAO: Analog Output Power - +3.3V DC nominal
27, 29, 64, 66	VDDDO	Power		VDDDO: Digital Output Power - +3.3V DC nominal

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
40, 62	VDDD	Power		VDDD: Digital Core Power - +3.3V DC nominal
42, 53	VDDD_1_8	Power		VDDD_1_8: Digital Core Power - +1.8V DC nominal
19,23	VSSAO	Ground		VSSAO: Ground
73 (e_PAD)	VSS	Ground	-	VSS: Ground
<b>Other</b>				
58	IC	-	-	IC: Internal Connection Internal Use. This pin must be left open for normal operation.

## 2.1 RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

### 2.1.1 INPUTS

#### Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### Single-Ended Clock Inputs

For protection, unused single-ended clock inputs should be tied to ground.

#### Differential Clock Inputs

For applications not requiring the use of a differential input, both \*\_POS and \*\_NEG can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from \_POS to ground.

### 2.1.2 OUTPUTS

#### Status Pins

For applications not requiring the use of a status pin, we recommend bringing out to a test point for debugging purposes.

#### Single-Ended Clock Outputs

All unused single-ended clock outputs can be left floating, or can be brought out to a test point for debugging purposes.

#### Differential Clock Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

PACKAGE DIMENSIONS

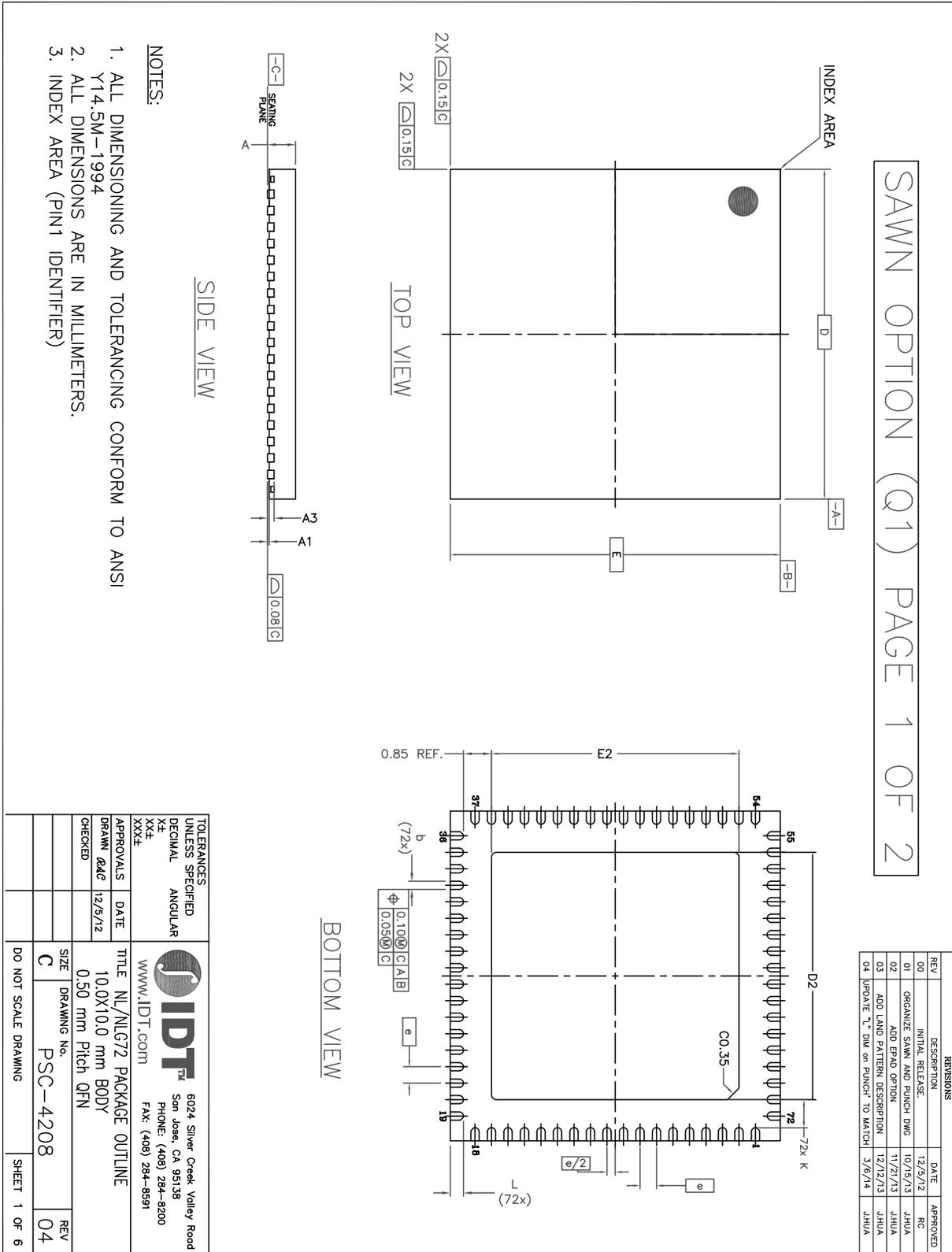


Figure 3. 72-Pin QFN Package Outline Page 1 (SAWN Option)

# SAWN OPTION (Q1) PAGE 2 OF 2

## EPAD OPTION:

SYMBOL	P2		
	MIN.	NOM.	MAX.
E2	7.40	7.50	7.60
D2	7.40	7.50	7.60

SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
D2	SEE EPAD OPTION		
E2	SEE EPAD OPTION		
K	0.20	—	—
A2	0.00	0.65	1.00
L	0.30	0.40	0.50
COMMON DIMENSIONS			
DIM SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3 REF	—	0.20 ref	—
b	0.18	0.25	0.30
Ⓜ		0.50 BSC	
D		10.00 BSC	
E		10.00 BSC	

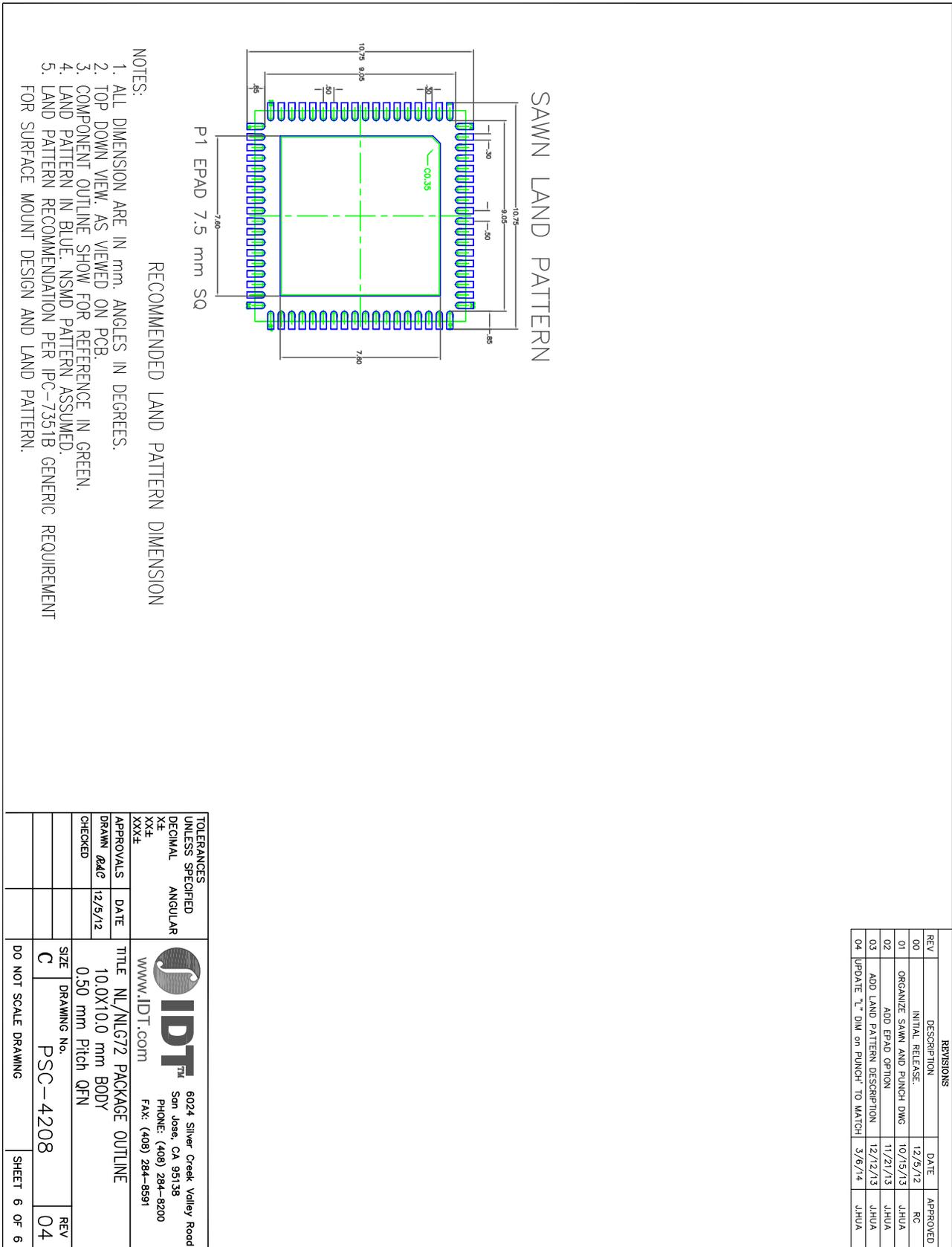
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	12/5/12	RC
01	ORGANIZE SAWN AND PUNCH DWG	10/15/13	JHUA
02	ADD EPAD OPTION	11/21/13	JHUA
03	ADD LAND PATTERN DESCRIPTION	12/12/13	JHUA
04	UPDATE "L" DIM ON PUNCH TO MATCH	3/6/14	JHUA

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XXX± ° XXXX±		APPROVALS DATE DRAWN <i>gdc</i> 12/9/12 CHECKED	
TITLE 10.0 X 10.0 mm BODY 0.50 mm Pitch QFN		SIZE C DRAWING No. PSC-4208	
DO NOT SCALE DRAWING		SHEET 2 OF 6	



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**Figure 4. 72-Pin QFN Package Outline Page 2 (SAWN Option)**



**Figure 5. 72-Pin QFN Package Recommended Land Pattern**

## ORDERING INFORMATION

Table 2: Ordering Information

Part/Order Number	Package	Temperature
82P33724NLG	72-Pin QFN	-40° to +85°C

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.



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