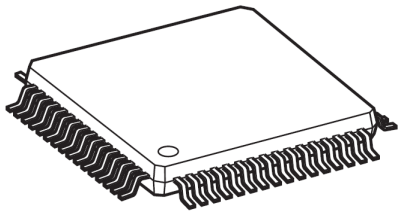
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC90104FG

Multi System Video Decoder IC

The TC90104FG is a single chip IC that converts analog video signals to digital video signals (ITU-R BT.601 / ITU-R BT.656 or 18bit digital RGB signal).

Additionally, the TC90104FG has a 3-channel A/D converter as an analog input interface, and has 3-line Y/C separation and multi-system color decoder functionality.



LQFP64-P-1010-0.50E

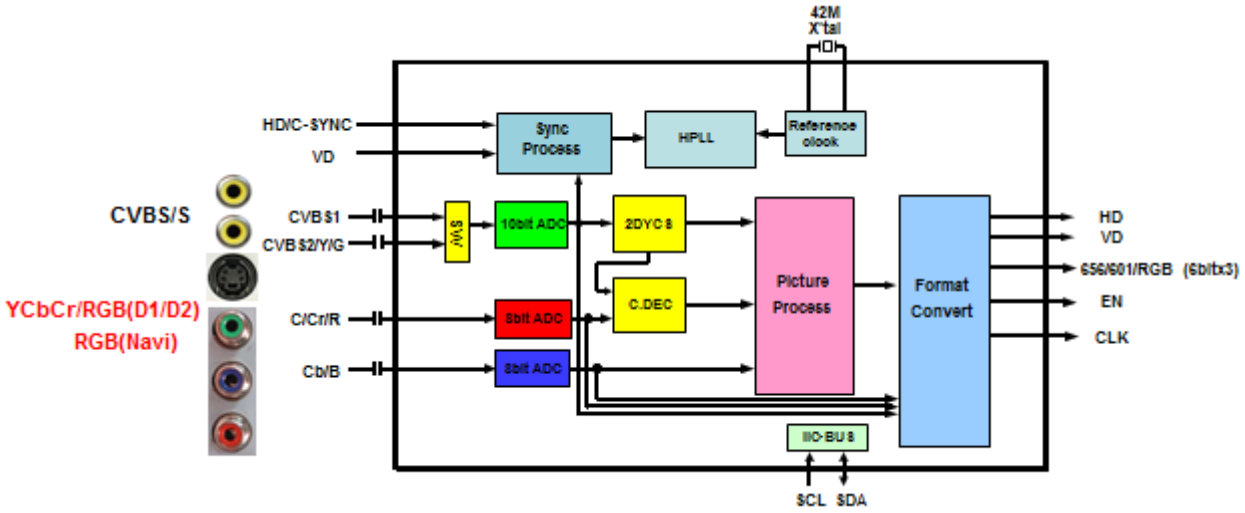
Weight: 0.4g (typ.)

1. Features

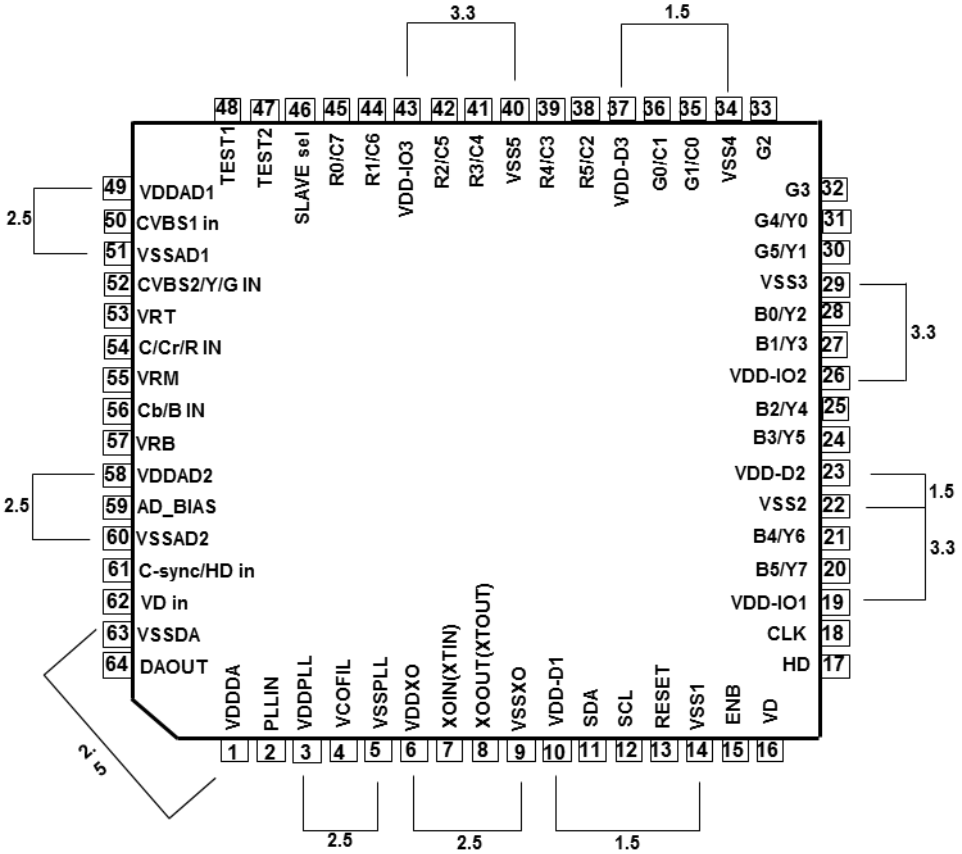
- Input: CVBS, Y/C(S-Video), YCbCr, RGB
- Multi-color decoder
- Adaptive multi-standard detection / sync processing
- Synchronous playback / Standard identification
- Y/C separation: 3-line YCS (NTSC/PAL)
  BPF processing. (SECAM)
- Picture process Y: V-Enhance, LTI, sharpness, noise cancel, contrast, brightness
  C: TOF, ACC, color gain, CTI, noise cancel
  RGB: color gain, color offset, gamma correction
- Analog RGB input: WQVGA to WVGA (dot by dot)
- ADC-clock phase adjustment (RGB input)
- Output: ITU-R BT.601 / ITU-R BT.656 in Video, RGB 6bit x 3 in RGB.
- I^2C-bus control
- Package: LQFP 64 pin (0.50 mm pitch)
- Power supply: 3.3 V, 2.5 V, 1.5 V

2. Block Diagram

To explain the function, there are omitted part for function block and application circuit.



3. Pin Layout



4. Pin Descriptions

Pin No.	Pin Name	Pin Function	Pin type	Standard withstand voltage [V]	Processing at unused time
1	VDDDA	2.5 V power supply for DAC	VDD	2.5	-
2	PLLIN	Input of PLL circuit for clock	IN	2.5	-
3	VDDPLL	2.5 V power supply for PLL circuit	VDD	2.5	-
4	VCOFIL	Filter terminal for PLL circuit	Bias	2.5	-
5	VSSPLL	GND for PLL circuit	VSS	0	-
6	VDDXO	Power supply for X'tal circuit	VDD	2.5	-
7	XOIN	Input for X'tal circuit	IN	2.5	-
8	XOOUT	Output for X'tal circuit	OUT	2.5	-
9	VSSXO	GND for X'tal circuit	GND	0	-
10	VDD-D1	1.5 V power supply for Logic circuit	VDD	1.5	-
11	SDA	Serial data input/output <I^2C-BUS>	I / O	5	-
12	SCL	Serial clock input <I^2C-BUS>	IN	5	-
13	RESET	System reset	IN	3.3	-
14	VSS1	GND for logic	GND	0	-
15	ENB	Enable signal output	OUT	3.3	Open
16	VD	Vertical timing signal output	OUT	3.3	Open
17	HD	Horizontal timing signal output	OUT	3.3	Open
18	CLK	Clock signal output	OUT	3.3	-
19	VDD-IO1	3.3 V power supply for I/O circuit	VDD	3.3	-
20	B5/Y7	B5 / Y7 signal output	OUT	3.3	-
21	B4/Y6	B4 / Y6 signal output	OUT	3.3	-
22	VSS2	GND for logic	GND	0	-
23	VDD-D2	1.5V power supply for logic circuit	VDD	1.5	-
24	B3/Y5	B3 / Y5 signal output	OUT	3.3	-
25	B2/Y4	B2 / Y4 signal output	OUT	3.3	-
26	VDD-IO2	3.3V power supply for I/O circuit	VDD	3.3	-
27	B1/Y3	B1 / Y3 signal output	OUT	3.3	-
28	B0/Y2	B0 / Y2 signal output	OUT	3.3	-
29	VSS3	GND for logic	GND	0	-
30	G5/Y1	G5 / Y1 signal output	OUT	3.3	-
31	G4/Y0	G4 / Y0 signal output	OUT	3.3	-
32	G3	G3 signal output	OUT	3.3	-

Pin No.	Pin Name	Pin Function	Pin type	Standard withstand voltage [V]	Processing at unused time
33	G2	G2 signal output	OUT	3.3	-
34	VSS4	GND for logic	GND	0	-
35	G1/C0	G1 / C0 signal output	OUT	3.3	-
36	G0/C1	G0 / C1 signal output	OUT	3.3	-
37	VDD-D3	1.5 V power supply for logic circuit	VDD	1.5	-
38	R5/C2	R5 / C2 signal output	OUT	3.3	-
39	R4/C3	R4 / C3 signal output	OUT	3.3	-
40	VSS5	GND for logic	GND	0	-
41	R3/C4	R3 / C4 signal output	OUT	3.3	-
42	R2/C5	R2 / C5 signal output	OUT	3.3	-
43	VDD-IO3	3.3 V power supply for I/O circuit	VDD	3.3	-
44	R1/C6	R1 / C6 signal output	OUT	3.3	-
45	R0/C7	R0 / C7 signal output	OUT	3.3	-
46	SLAVE sel	I^2C-BUS slave-address selector	IN	3.3	-
47	TEST2	Test terminal (Always connect to GND)	IN	3.3	GND
48	TEST1	Test terminal (Always connect to GND)	IN	3.3	GND
49	VDDAD1	2.5 V power supply for ADC circuit	VDD	2.5	-
50	CVBS1 in	Composite video signal input	IN	2.5	GND via 0.1 μF
51	VSSAD1	GND for ADC circuit	GND	0	-
52	CVBS2/Y/G IN	Composite video / Y / G signal input	IN	2.5	GND via 0.1 μF
53	VRT	Reference top voltage terminal for ADC	Bias	2.5	-
54	C/Cr/R IN	C / Cr /R signal input	IN	2.5	GND via 0.1 μF
55	VRM	Reference middle voltage terminal for ADC	Bias	2.5	-
56	Cb/B IN	Cb / B signal input	IN	2.5	GND via 0.1 μF
57	VRB	Reference bottom voltage terminal for ADC	Bias	2.5	-
58	VDDAD2	2.5 V power supply for ADC circuit	VDD	2.5	-
59	AD_BIAS	Bias voltage terminal for ADC	Bias	2.5	-
60	VSSAD2	GND for ADC circuit	GND	0	-
61	C-sync/HD in	Composite-sync signal / Horizontal timing signal input	IN	3.3	GND
62	VD in	Vertical timing signal input	IN	3.3	GND
63	VSSDA	GND for DAC circuit for clock	GND	0	-
64	DAOUT	Output of DAC circuit for clock	OUT	2.5	-

5. Function

5.1 Overview

- Analog input interface for CVBS (Composite video signal), Y/C separate signal, Component signal (D1/D2), analog RGB signal (D1/D2) and analog RGB signal (WQVGA / VGA / WVGA)
- Multi system 3-line comb filter (2DYCS)
- Multi system video decoder and sync processing
- Color system detection (selectable auto detection or manual setting)
- Picture processing function
- Adjustable the clock phase of ADC in analog RGB input mode
- Digital output interface for ITU-R BT.601/656 and 18bit RGB signal
  When input signal is analog RGB, output signal is digital RGB only.

5.2 Input signal

5.2.1 Input signal list

Input signal format			Frequency			Effective pixels		Total pixels	
			fH[kHz]	fV[Hz]	fs [MHz]	Horizontal	Vertical	Horizontal	Vertical
CVBS	NTSC		15.75/15.734	60/59.94	27	720	240	858	262.5
	PAL		15.625	50	27	720	288	864	312.5
Y/C	NTSC		15.75/15.734	60/59.94	27	720	240	858	262.5
	PAL		15.625	50	27	720	288	864	312.5
YCbCr	D1	480i	15.75/15.734	60	27	720	240	858	262.5
		576i	15.625	50	27	720	288	864	312.5
	D2	480p	31.5/31.469	60	27	720	480	858	525
		576p	31.25	50	27	720	576	864	625
RGB	D1	480i	15.75/15.734	60	27	720	240	858	262.5
		576i	15.625	50	27	720	288	864	312.5
	D2	480p	31.5/31.469	60	27	720	480	858	525
		576p	31.25	50	27	720	576	864	625
RGB	WQVGA (400x234)		15.734	60	fH×508	400	234	508	262
			15.625	50	fH×508	400	234	508	312
	WQVGA (480x234)		15.734	60	fH×610	480	234	610	262
			15.625	50	fH×610	480	234	610	312
	VGA (640x480)		31.5	60	fH×800	640	480	800	525
			31.25	50	fH×800	640	480	800	625
	WVGA (800x480)		31.5	60	fH×1056	800	480	1056	525
			31.25	50	fH×1056	800	480	1056	625

5.2.2 Input signal

The TC90104FG is equipped with 3-ch ADC for Composite video signal, YCbCr signal and RGB signal and Y/C signal input.

The input-dynamic-range for ADC is designed in AVDD x 0.4 [V] with the normal input dynamic range being 1 Vp-p (AVDD = 2.5 V). Be sure to use 0.7 Vp-p (1 Vp-p x 0.7) with 140IRE input when using NTSC as the recommended reference input amplitude.

We recommend that you use 0.7 Vp-p with 140IRE input for the input amplitude.

CVBS, Y/C, YCbCr, RGB (D1/D2) signal are processed at MCD block, and RGB (WQVGA, VGA, WVGA) signal are processed at RGB block.

5.2.3 Table of Input – Output signal

Input signal				Processing		Output signal					
Input format			f H [kHz]	Sampling clock [MHz]	Internal Format	Output clock [MHz]	RGB	601 656	HD	VD	ENB
CVBS	NTSC		15.75/15.734	27	4:2:2	13.5 / 27	-	○	○	○	-
	PAL		15.625	27	4:2:2	13.5 / 27	-	○	○	○	-
Y/C	NTSC		15.75/15.734	27	4:2:2	13.5 / 27	-	○	○	○	-
	PAL		15.625	27	4:2:2	13.5 / 27	-	○	○	○	-
YCbCr	D1	480i	15.75/15.734	27	4:2:2	13.5 / 27	-	○	○	○	-
		576i	15.625	27	4:2:2	13.5 / 27	-	○	○	○	-
	D2	480p	31.5/31.469	27	4:2:2	27	-	○	○	○	-
		576p	31.25	27	4:2:2	27	-	○	○	○	-
RGB	D1	480i	15.75/15.734	27	4:2:2	13.5 / 27	-	○	○	○	-
		576i	15.625	27	4:2:2	13.5 / 27	-	○	○	○	-
	D2	480p	31.5/31.469	27	4:2:2	27	-	○	○	○	-
		576p	31.25	27	4:2:2	27	-	○	○	○	-
RGB	WQVGA (400x234)		15.734	fH×508	4:4:4	fH×508	○	-	○	○	○
			15.625	fH×508	4:4:4	fH×508	○	-	○	○	○
	WQVGA (480x234)		15.734	fH×610	4:4:4	fH×610	○	-	○	○	○
			15.625	fH×610	4:4:4	fH×610	○	-	○	○	○
	VGA (640x480)		31.5	fH×800	4:4:4	fH×800	○	-	○	○	○
			31.25	fH×800	4:4:4	fH×800	○	-	○	○	○
	WVGA (800x480)		31.5	fH×1056	4:4:4	fH×1056	○	-	○	○	○
			31.25	fH×1056	4:4:4	fH×1056	○	-	○	○	○

5.2.4 Typical input level of analog input signal

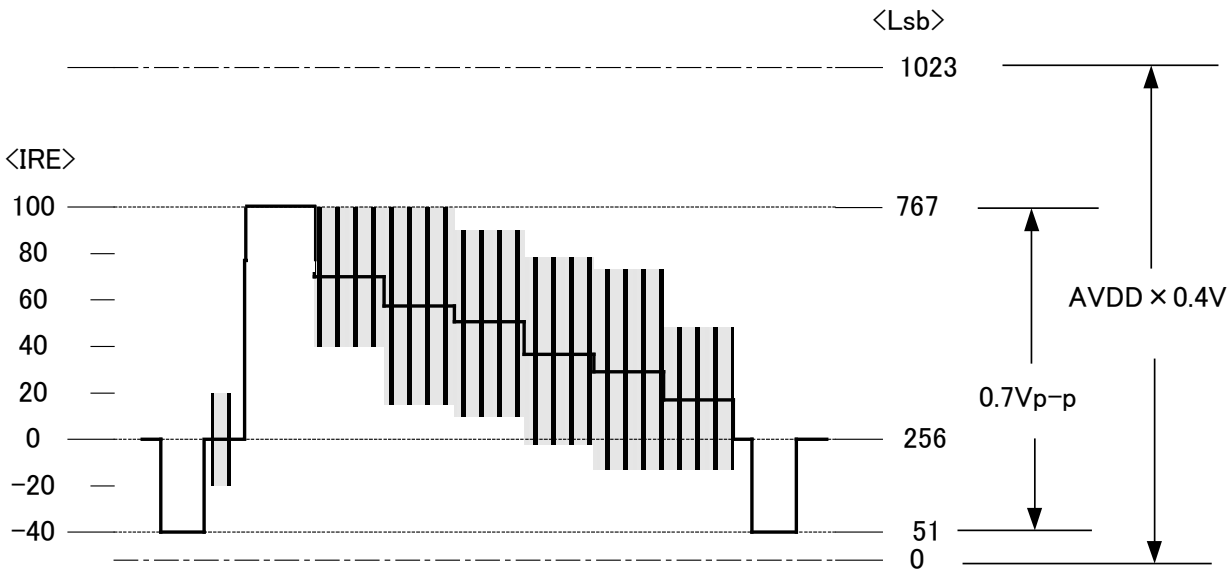


Fig.1 Reference input level to CVBS1(Composite Video) and CVBS2/Y/G(S-Video Y, Componet Y) when 100% White (i.e., composite video input)

CVBS, Y, Component-Y signal need to input 0.7 Vpp when 140IRE, and also C signal (S-signal) need to input 0.2 Vpp when 40IRE. (VDD = 2.5 V, 140IRE = 0.7 Vpp at NTSC)
When use Component-CbCr , CbCr-level is 0.7 Vpp for 100%.
An above waveform is color bar signal of 75%

Input terminal	Input level = Vp-p *1	Output : LSB *2	Notes
CVBS	0.7 Vp-p (500 mVp-p)	16-235 (for 8bit)	Output at ITU-R BT.656/601 format
Y	0.7 Vp-p (500 mVp-p)	16-235 (for 8bit)	Output at ITU-R BT.656/601 format
C	0.2 Vp-p (Burst signal)	31-225 (for 8bit)	Output at ITU-R BT.656/601 format
Cb	0.7 Vp-p	31-225 (for 8bit)	Output at ITU-R BT.656/601 format
Cr	0.7 Vp-p	31-225 (for 8bit)	Output at ITU-R BT.656/601 format

*1 About input level,
It has indicate the case of NTSC.
CVBS and Y input level will be 140IRE at the White of 100%.
Please adjust to 0.7 V this 100%.
Values in the ( ) is the level of from the pedestal to white 100%.

Input level of C(= chroma signal) has indicate the burst level at the time of NTSC.
Input level of CbCr has indicate the level of color-100% at the time of NTSC.

*2 About output level,
It has indicate the case of NTSC.
CVBS and Y output level is white100% output level at the time of NTSC.
Values in the ( ) is the output level of from the pedestal to white 100%.

Output level of C(chroma signal) indicate the CbCr level at the time of color-100%.
Output level of CbCr indicate the level of color-100% at the time of NTSC.

Notes: The above output level is influenced by the picture quality adjustment.
It does not indicate the maximum level.

Fig.2 Reference input level to C/Cr/R (S-Video C)

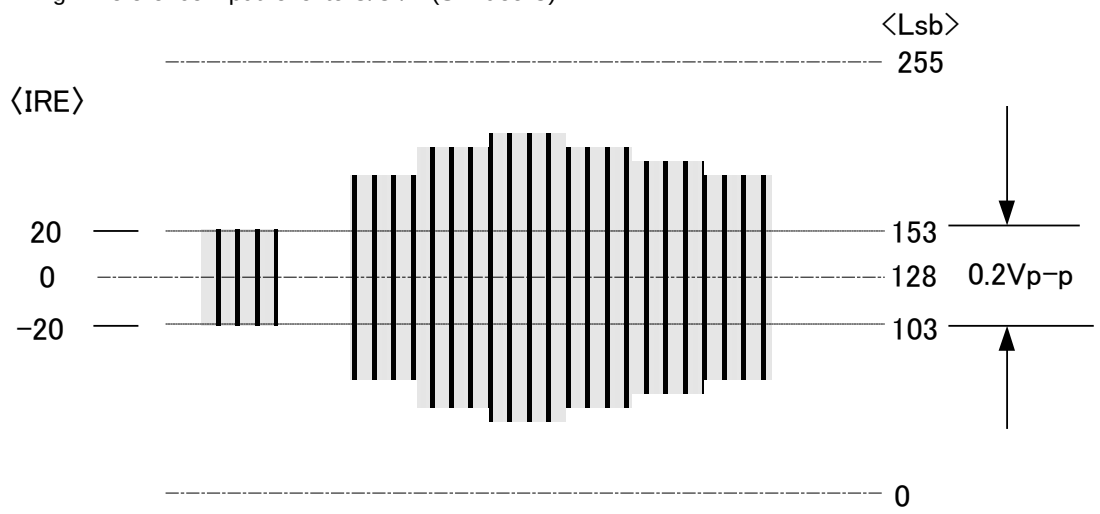


Fig.3 Typical input level to C/Cr/R (Component Cr) and Cb/B (Component Cb)

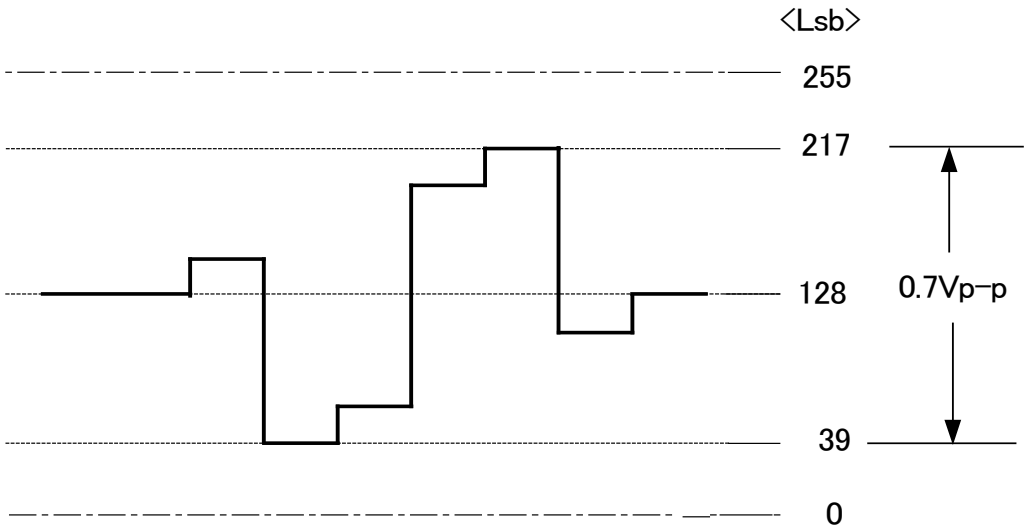


Fig.4 Typical input level to CVBS2/Y/G (RGB G), C/Cr/R (RGB R) and Cb/B (RGB B)

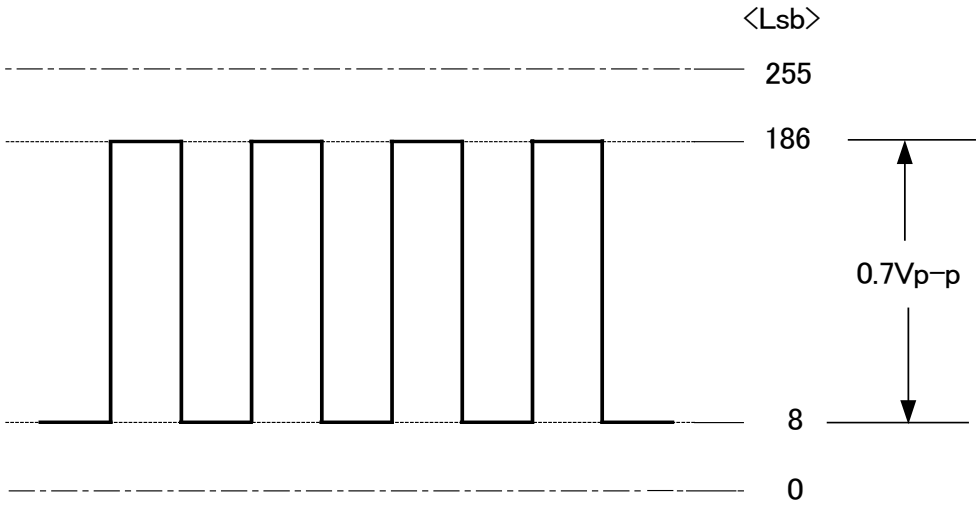
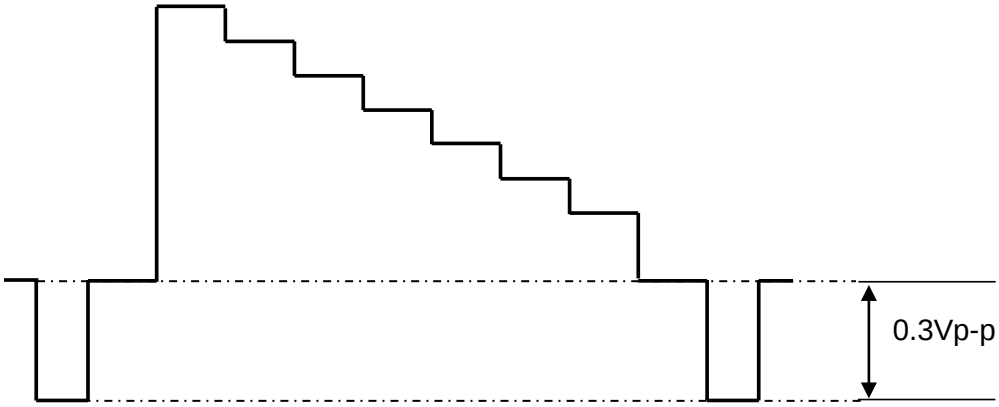


Fig.5 Typical input level to Composite sync



5.2.5 Operation mode (I/O select) setting

Signal process path (I/O) is selected by I^2C-BUS register (Sub00H [D7] RGB_MCD by common on all Bank).

RGB_MCD = 0: MCD block select (CVBS, Y/C, YCbCr, RGB(D2,D1))
1: RGB block select (RGB (QVGA, VGA, WVGA))

Output format decides by signal process route. ITU-R BT.601 or ITU-R BT.656 is output at route of MCD block, and RGB 18bit is output at route of RGB block.

The setting of MCD block depend on Bank0, and setting of RGB depend on Bank1 and Bank2.

Input mode	Setting of Sub address: 00H	Active Bank	Setting contents
Video	00(hex)	Bank 0	CVBS/YCbCr input to ITU-R BT.656/601 output
A-RGB	81(hex)	Bank1	RGB(dot by dot) input to RGB 18bit output
gamma of A-RGB	82(hex)	Bank2	RGB(dot by dot) input to RGB gamma setting

5.2.6 Output format

The output format (ITU-R BT.656/601) is selected by register FORMATO (Bank0, Sub address02h).
However, when D2 format is inputted, output format is fixed on 4:2:2 format.
Y: pedestal level = 16 LSB
C: center electric potential = 128 LSB

Signal process of Y output signal below pedestal is set by register CLP (Bank 0, Sub address 29h).
CLP = 1 : signal below pedestal is fixed on 16LSB
CLP = 0 : signal below pedestal is outputted through

Output signal	Bit	Data rate	Description
Y [0-7]	8	13.5 MHz/27 MHz (ITU-R BT.601/656)	Y / YCbCr (ITU-R BT.601/656)
C [0-7]	8	6.75 MHz	Cb / Cr (CLK: 13.5 MHz)
CLK	1	13.5 MHz/27 MHz	864fH/1728fH: 625 line system 858fH/1716fH: 525 line system Polarity: negative (initial setting)
HD	1	f H	Recovered horizontal sync signal
VD	1	f V	Recovered vertical sync signal

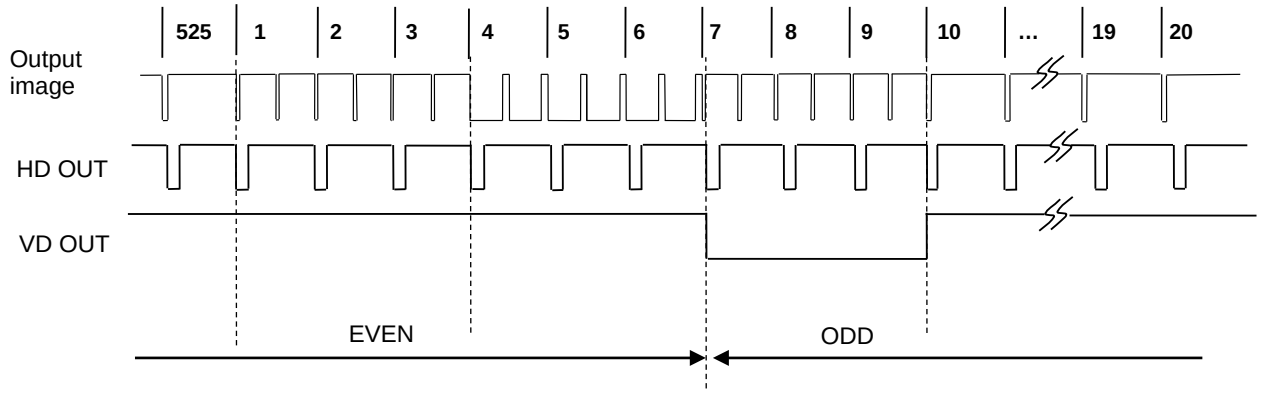
HD / VD pulse width in “Sync-through” mode

	525i system	625i system
HD pulse width	4.74 μs (128 cycle @ 27 MHz clock)	
VD pulse width	3 .0 H	2.5 H or 3.0 H

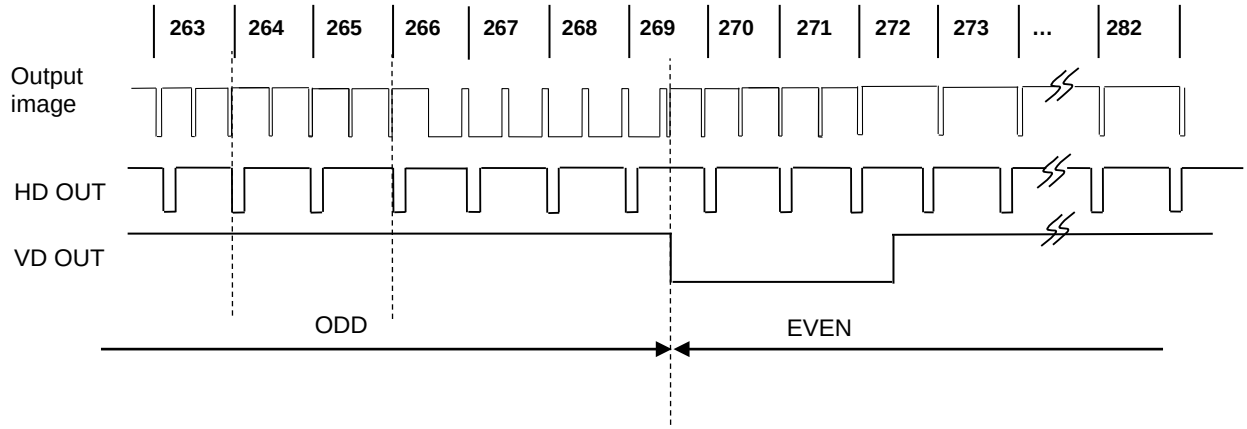
*Notes
The HD pulse width used in ITU-R BT.656-compliant mode is the same as the zone defined from EAV to SAV.
If a non-standard signal is input during ITU-R BT.656-compliant mode, then the values may not necessarily be the values shown in the above chart.
The VD pulse is synchronized using the HD standard. As a result, if the H cycle jitters, then the VD width will also jitter. Also, in Through mode, the phase with the HD has time lag of 0.5H in ODD/EVEN.

5.2.6.1. 525i/60Hz Input mode

(1'st Field)



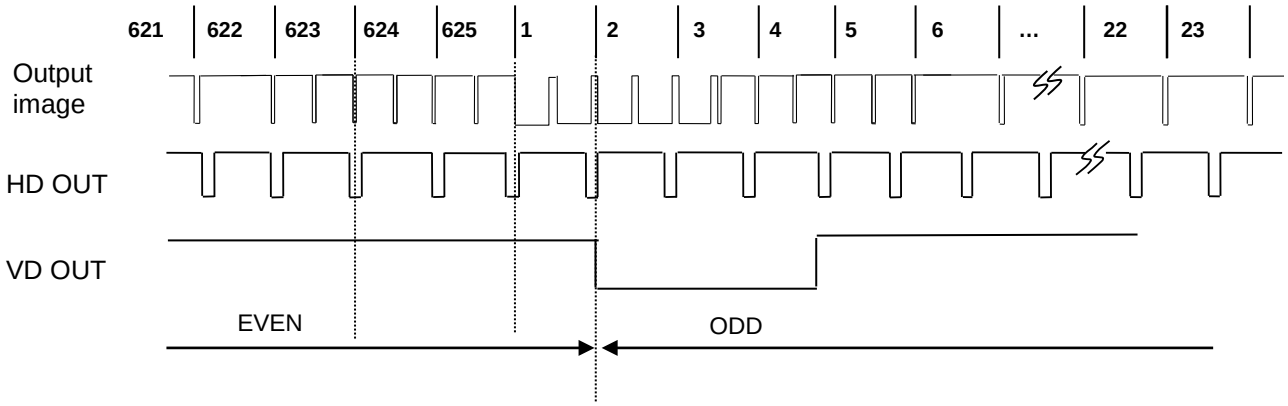
(2nd Field)



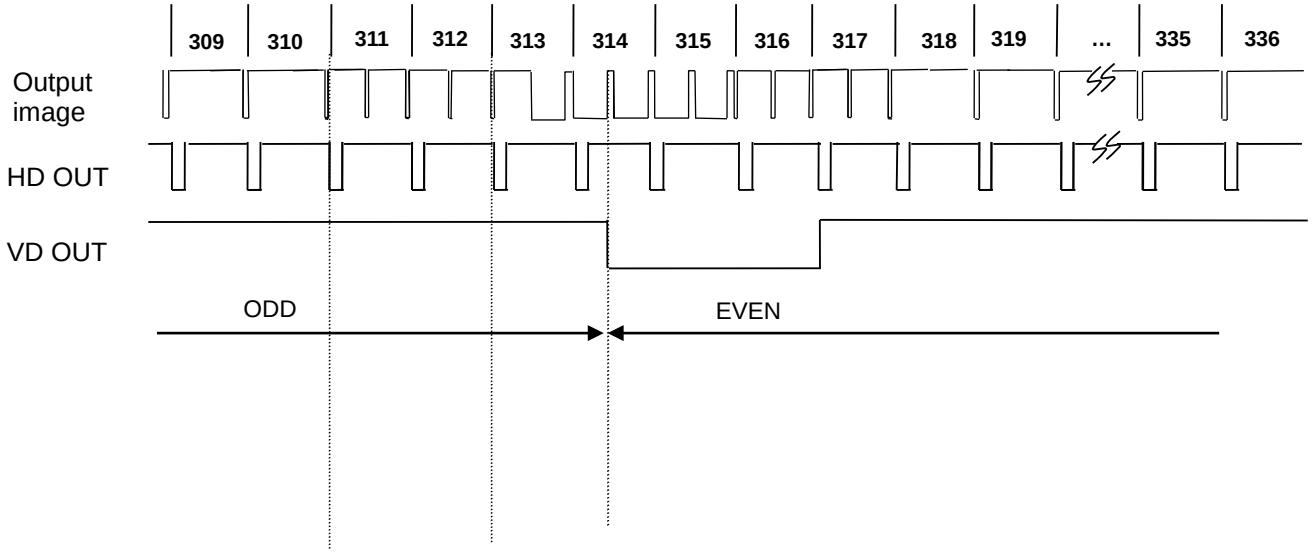
VD position is dependent on register setting.

5.2.6.2. 625i / 50Hz Input mode

(1st, 3rd field)



(2nd, 4th field)



VD position is dependent on register setting.

5.3 RGB block <Bank1>

5.3.1 Sync separation

There are two ways to provide sync signal;
One way is to input Sync-on-Green signal to “C-sync/HD in” (61pin) and operate sync-separation in IC.
Another way is to input HD pulse to “C-sync/HD in” (61pin) and input VD pulse to “VD in” (62 pin).

“C-sync/HD” (61pin) is an analog slicer input with a sync tip clamping. The slice level is programmable through the SYNCSLEV1[1:0] (Bank1, Sub address 1Eh)

5.3.2 Detection function for format discrimination

Following data can be detected for format discrimination by analog/digital sync input signal.
no-signal detect, input analog/digital detect, polarity, detect
V frequency, V-sync width, V-sync line, 1V line,
H frequency, H-sync width

5.3.3 Clock phase adjustment

Sampling clock of ADC can be selected from four phases for each R and G, B channel respectively.

5.3.4 Output format

Output format of video signal, at RGB block path, is 18bit digital RGB signal (R: 6 bit, G: 6 bit, B: 6 bit).
Also, HD/VD signal is outputted to HD (17 pin) / VD(16 pin), Enable signal is outputted to ENB (15 pin) and clock signal is outputted to CLK (18 pin).

6. Absolute Maximum rating

The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Exceeding the maximum rating may result in destruction, degradation or other damage to the IC and other components. When designing applications for this IC, be sure that none of the maximum rating values will ever be exceeded.

Characteristics	Symbol	Rating	Unit
Power voltage1 (1.5 V system)	VDD1	-0.3 to VSS+2.0	V
Power voltage2 (2.5 V system)	VDD2	-0.3 to VSS+3.5	V
Power voltage3 (3.3 V system)	VDD3	-0.3 to VSS+3.9	V
Input voltage (1.5 V system)	VIN1	-0.3 to VDD1+0.3	V
Input voltage (2.5 V system)	VIN2	-0.3 to VDD2+0.3	V
Input voltage (3.3 V system)	VIN3	-0.3 to VDD3+0.3	V
Input voltage (3.3 V system, 5 V withstand voltage)	VIN4 (Notes1)	-0.3 to VSS+5.5	V
Potential difference between power pins (between 1.5 V system power pins)	ΔVDG1 (Notes2)	0.3	V
Potential difference between power pins (between 2.5 V system power pins)	ΔVDG2 (Notes2)	0.3	V
Potential difference between power pins (between 3.3 V system power pins)	ΔVDG3 (Notes2)	0.3	V
Power dissipation	PD (Notes3)	2190	mW
Storage temperature	Tstg	-40 to 125	°C

Note1**:** The withstand voltage for pins (SDA, SCL) is 5 V.

Note2**:** For each of 1.5 V and 2.5 V and 3.3 V, system power supply terminal is made into the same voltage. The maximum potential difference should not exceed rating for all power supply terminals then. In addition, potential difference between all V_{SS} terminal must be under 0.01 V in this status.

Note3**:** If you intended to use a temperature higher than Ta = 25°C, reduce by 21.9 mW per one degree (°C) increase.

7. Operating condition

The TC90104FG is not guaranteed to function correctly if it is used outside its specified power voltage rage (1.5 V system power**:** 1.40 V to 1.60 V, 2.5 V system power**:** 2.3 V to 2.7 V, 3.3 V system power**:** 3.0 V to 3.6 V). Please use within the specified operating conditions.

If you temporarily leave and then return to the specified operating conditions, this IC's conditions will change, and so it is necessary to reset the IC's power to continue using it correctly within the specified operating conditions.

Characteristics	Corresponding terminal	Symbol	Min	Typ.	Max	Unit
Power voltage of digital block	10, 23, 37	VDD-D	1.4	1.5	1.6	V
Power voltage of I/O block	19, 26, 43	VDD-IO	3.0	3.3	3.6	V
Power voltage of XO block	6	VDDXO	2.3	2.5	2.7	V
Power voltage of PLL block	3	VDDPLL	2.3	2.5	2.7	V
Power voltage of analog block	1, 49, 58	VDDDA, VDDAD	2.3	2.5	2.7	V
Operating templature		Topr	-40	—	85	°C

8. Electrical characteristic

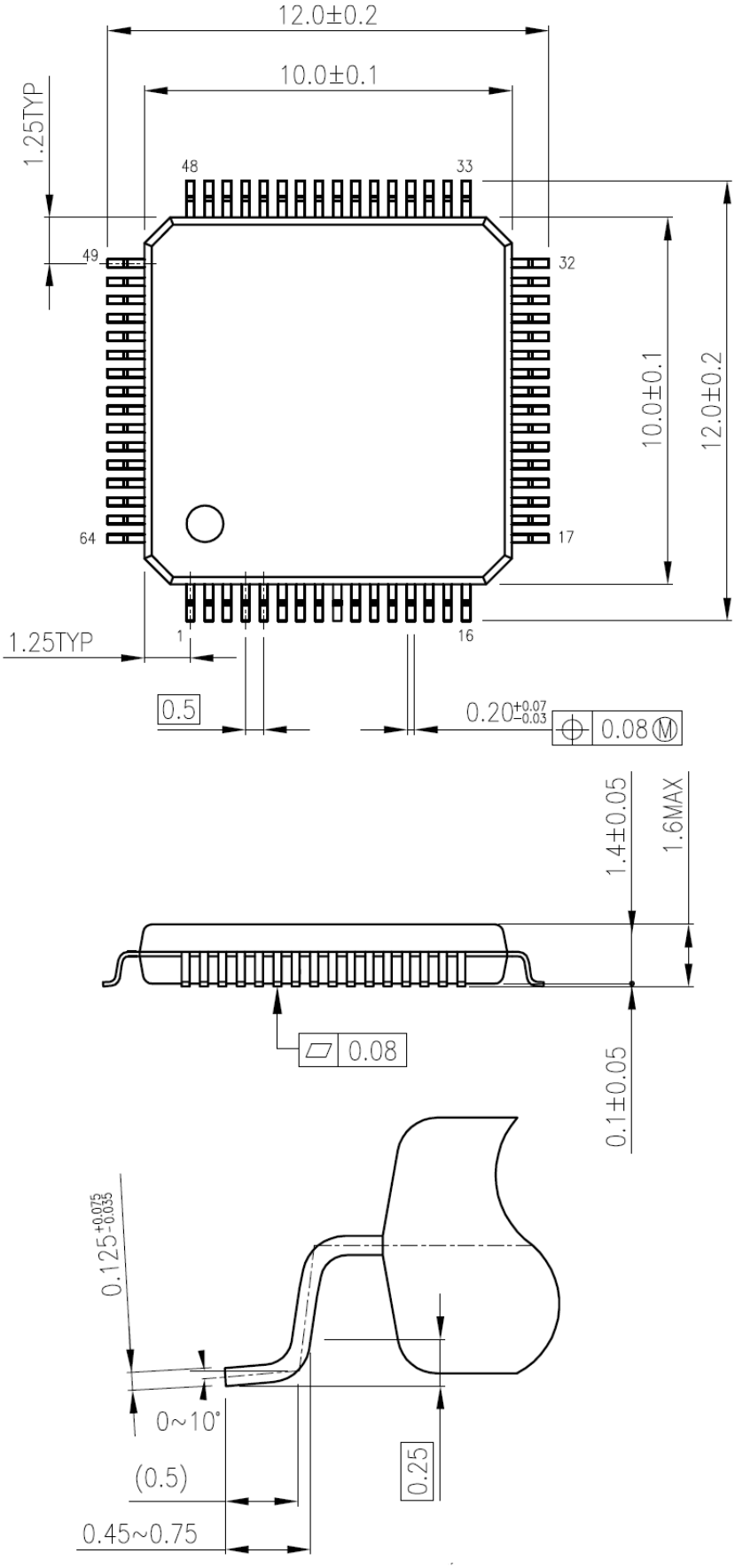
8.1 DC characteristic

(Ta = 25°C, 1.5 V system = 1.50 ± 0.1 V, 2.5 V system = 2.50 ± 0.2 V, 3.3 V system = 3.30 ± 0.3 V)

Characteristic	Terminal NO.	Symbol	Min	Typ.	Max	Unit	Note
Power supply current	10, 23, 37	IDD1 (1.5 V system)	–	46	70	mA	Depend on load at 3.3 V system.
	1, 3, 6, 49, 58	IDD2 (2.5 V system)	–	82	125	mA	
	19, 26, 43	IDD3 (3.3 V system)	–	10	–	mA	
Input voltage	13, 46, 47, 48, 61, 62	VIH	VDD3x0.8	–	VDD3	V	I/O input terminal of 3.3 V system
	11, 12						I/O input terminal of 5.0 V system
	13, 46, 47, 48, 61, 62	VIL	VSS	–	VDD3x0.2	V	I/O input terminal of 3.3 V system
	11,12						I/O input terminal of 5.0 V system
Input current	13, 46, 47, 48, 61, 62	IIH	-10	–	10	μA	I/O input terminal of 3.3 V system
	11, 12						I/O input terminal of 5.0 V system
	13, 46, 47, 48, 61, 62	IIL	-10	–	10	μA	I/O input terminal of 3.3 V system
	11, 12						I/O input terminal of 5.0 V system
Output voltage	15, 16, 17, 18, 20, 21, 24, 25, 27, 28, 30, 31, 32, 33, 35, 36, 38, 39, 41, 42, 44, 45	V_{OH}	VDD3-0.6	–	VDD3	V	I/O output terminal of 3.3 V system When load current: -4 mA
		V_{OL}	VSS	–	0.4	V	I/O output terminal of 3.3 V system When load current: +4 mA

9. Package

LOFP64-P-1010-0.50E **Unit: mm**



Weight: 0.4 g (Typ.)

10. Revision History

Date	Revision	Contents
2015/12/01	1.00	First edition

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