

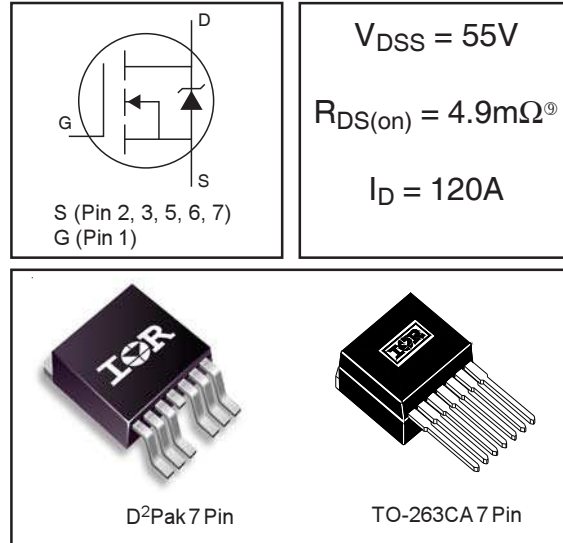
HEXFET® Power MOSFET

**Features**

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to  $T_{jmax}$
- Lead-Free

**Description**

This HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.



Base part number	Package Type	Standard Pack		Orderable Part Number	Note
		Form	Quantity		
IRF1405ZS-7PPbF-	D <sup>2</sup> Pak-7Pin	Tube	50	IRF1405ZS-7PPbF	EOL notice # 289
IRF1405ZS-7PPbF		Tape and Reel Left	800	IRF1405ZSTR7PP	
IRF1405ZL-7PPbF-	TO-263CA	Tube	50	IRF1405ZL-7PPbF-	EOL notice # 288

**Absolute Maximum Ratings**

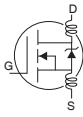
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	150	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (See Fig. 9)	100	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	120	
$I_{DM}$	Pulsed Drain Current ①	590	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	230	W
	Linear Derating Factor	1.5	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	250	mJ
$E_{AS} (tested)$	Single Pulse Avalanche Energy Tested Value ③	810	
$I_{AR}$	Avalanche Current ④	See Fig. 12a, 12b, 15, 16	A
$E_{AR}$	Repetitive Avalanche Energy ⑤		mJ
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	0.65	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑦	—	40	

HEXFET® is a registered trademark of International Rectifier.

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

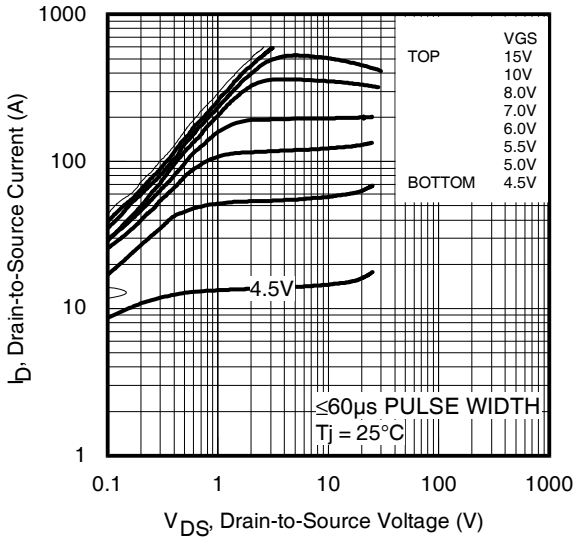
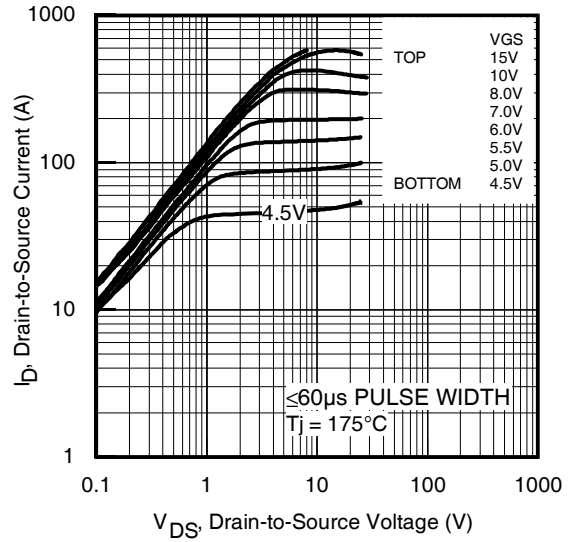
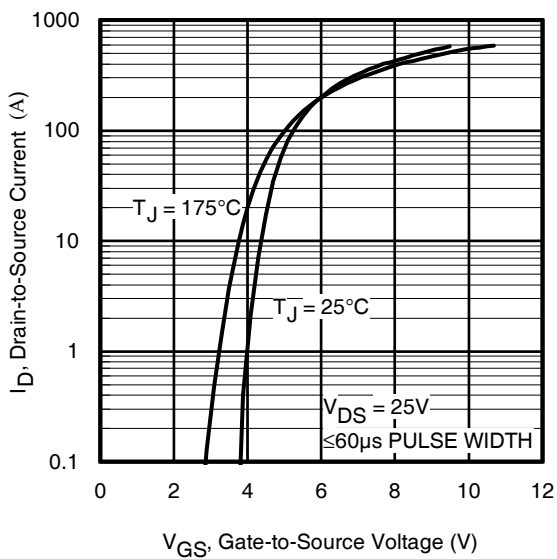
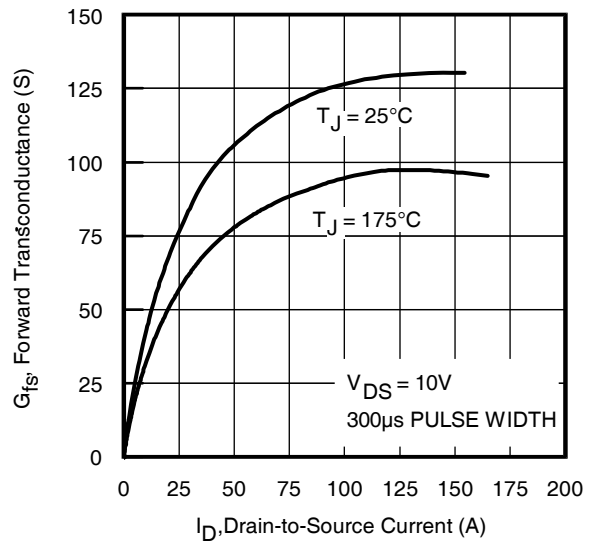
	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	55	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.054	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub> SMD	Static Drain-to-Source On-Resistance	—	3.7	4.9	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 88A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 150μA
g <sub>fs</sub>	Forward Transconductance	150	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 88A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 55V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 55V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	150	230	nC	I <sub>D</sub> = 88A
Q <sub>gs</sub>	Gate-to-Source Charge	—	37	—		V <sub>DS</sub> = 44V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	64	—		V <sub>GS</sub> = 10V ③
t <sub>d(on)</sub>	Turn-On Delay Time	—	16	—	ns	V <sub>DD</sub> = 28V
t <sub>r</sub>	Rise Time	—	140	—		I <sub>D</sub> = 88A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	170	—		R <sub>θ</sub> = 5.0Ω
t <sub>f</sub>	Fall Time	—	130	—		V <sub>GS</sub> = 10V ②
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	5360	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	1310	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	340	—		f = 1.0MHz, See Fig. 5
C <sub>oss</sub>	Output Capacitance	—	6080	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	920	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 44V, f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance	—	1700	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 44V

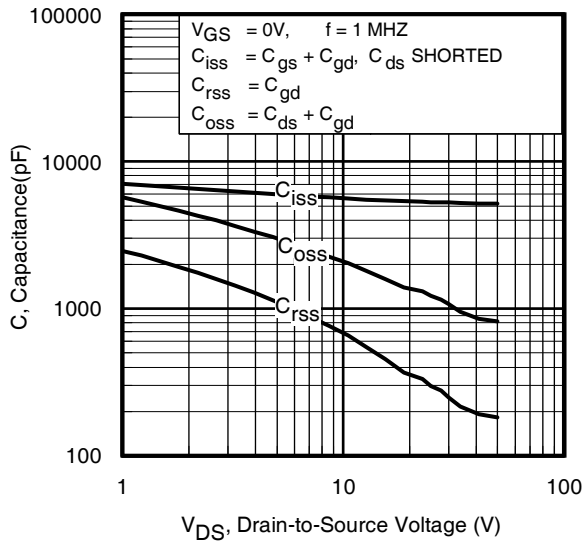
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	150	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	590		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 88A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	63	95	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 88A, V <sub>DD</sub> = 28V
Q <sub>rr</sub>	Reverse Recovery Charge	—	160	240	nC	di/dt = 100A/μs ③

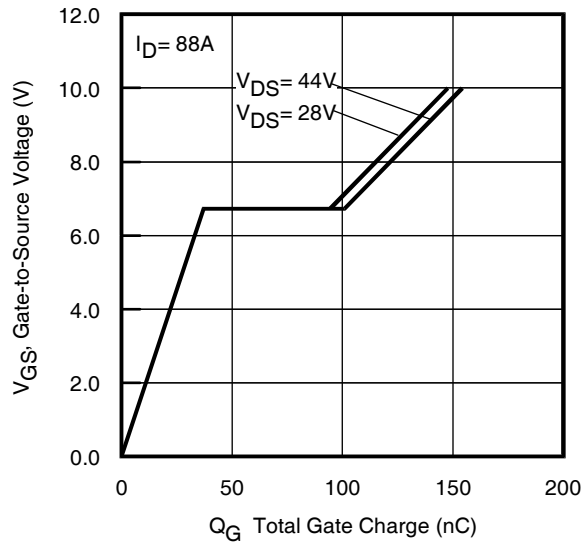
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L=0.064mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 88A, V<sub>GS</sub> = 10V.  
Part not recommended for use above this value.
- ③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
- ④ C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑤ Limited by T<sub>Jmax</sub>, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R<sub>θ</sub> is measured at T<sub>J</sub> of approximately 90°C.
- ⑨ Solder mounted on IMS substrate.

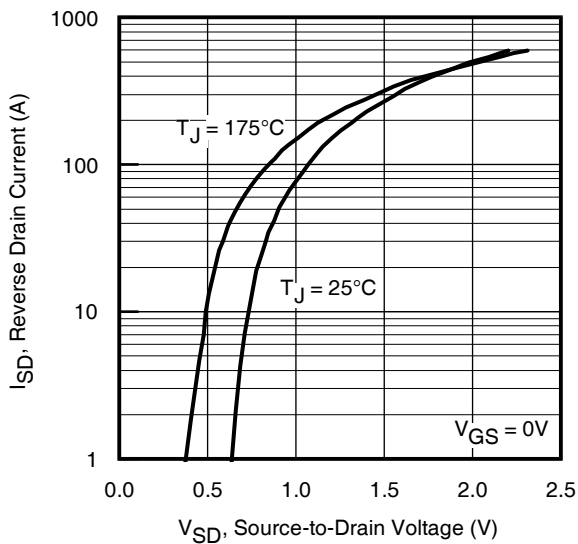

**Fig 1.** Typical Output Characteristics

**Fig 2.** Typical Output Characteristics

**Fig 3.** Typical Transfer Characteristics

**Fig 4.** Typical Forward Transconductance vs. Drain Current



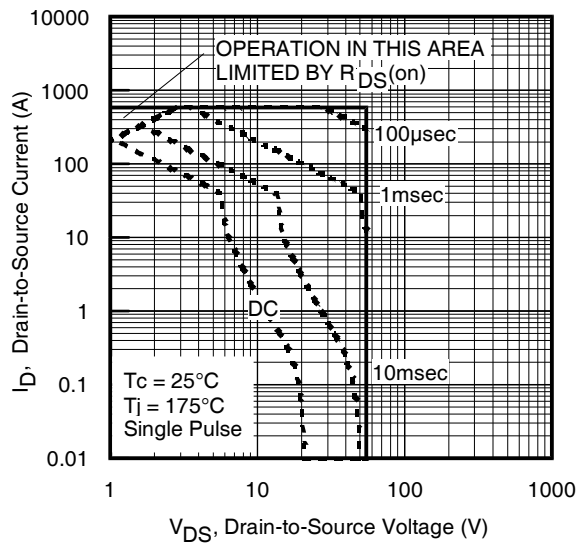
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



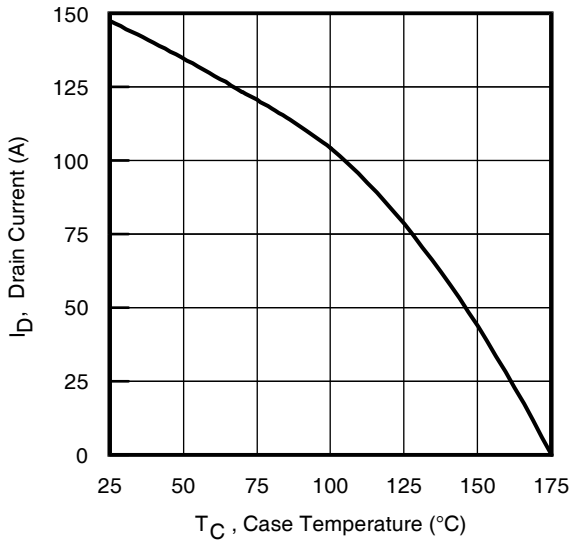
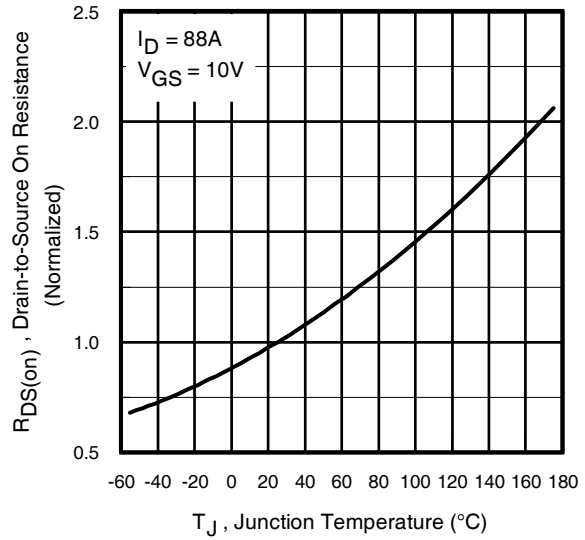
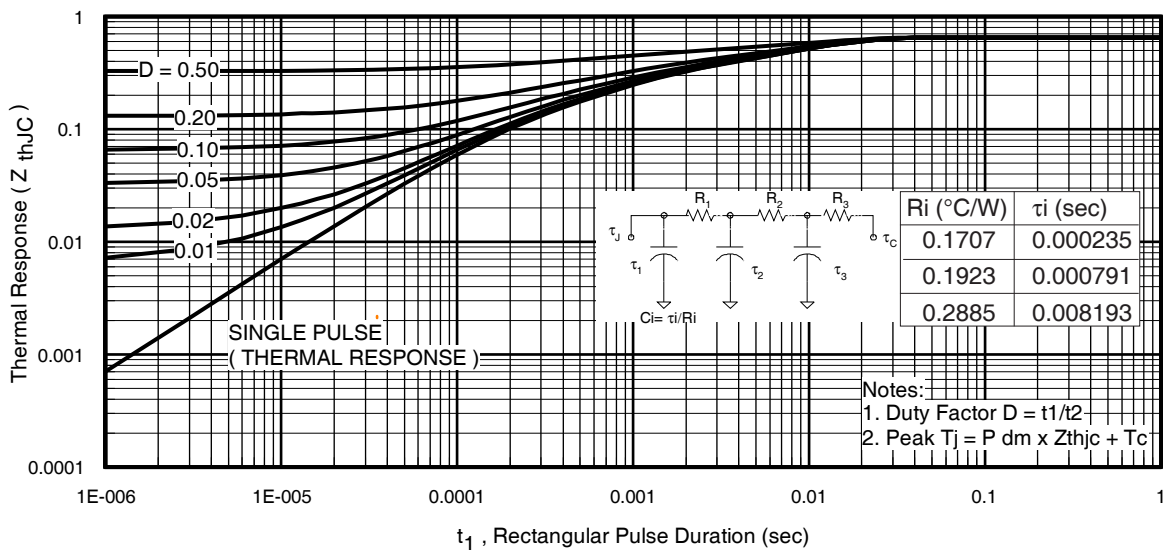
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

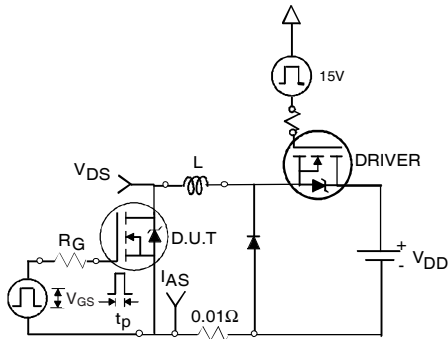
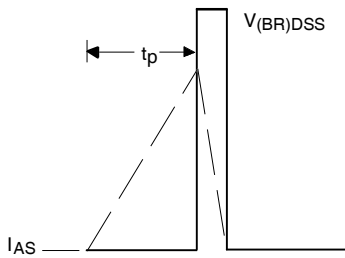
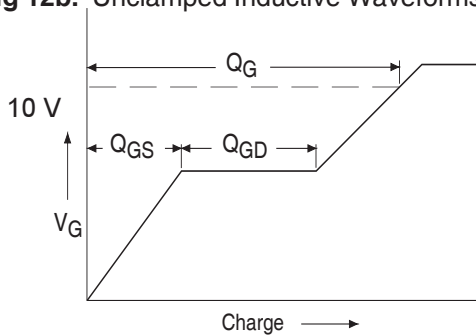
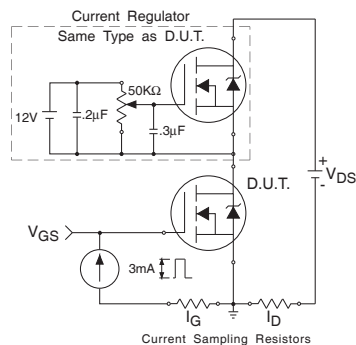
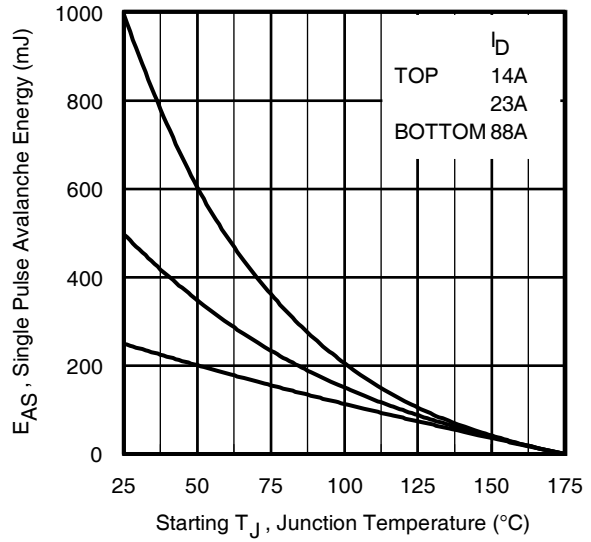
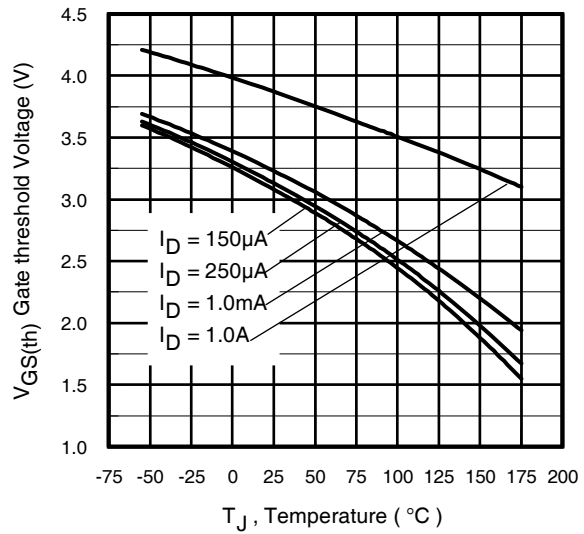


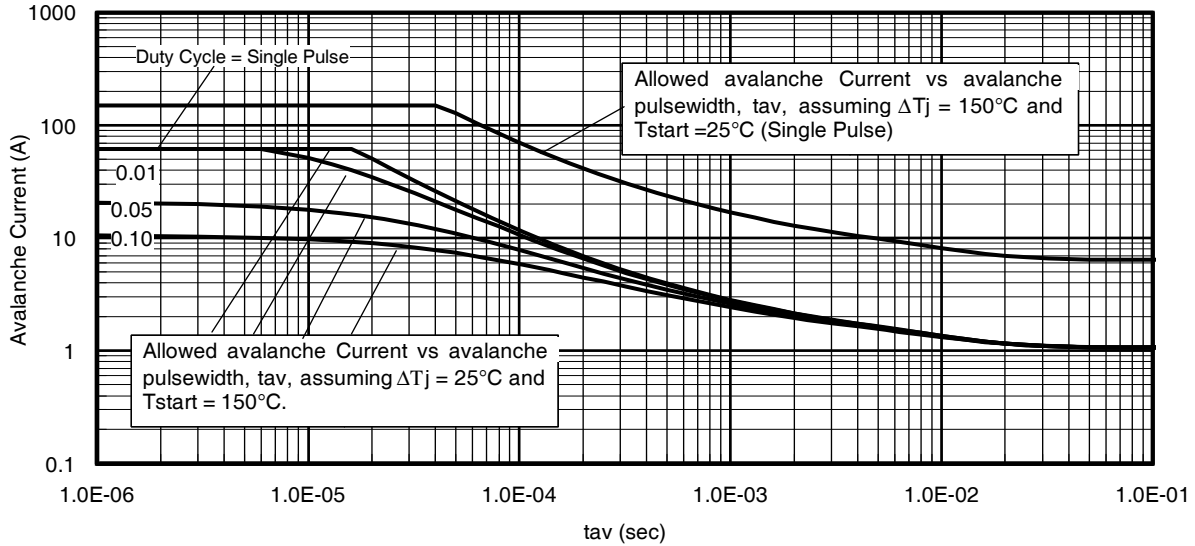
**Fig 7.** Typical Source-Drain Diode Forward Voltage



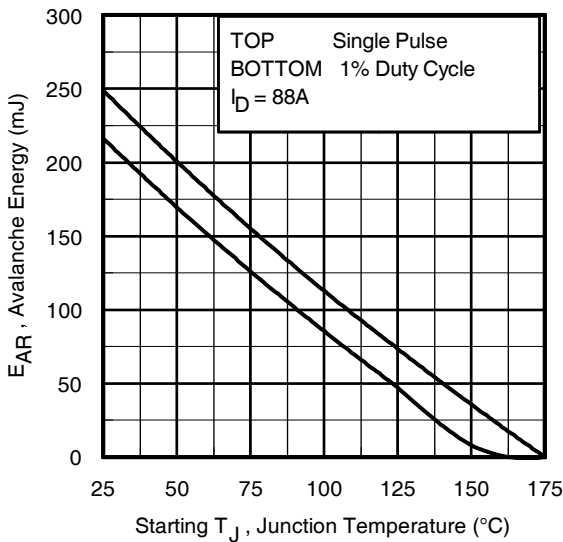
**Fig 8.** Maximum Safe Operating Area


**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Normalized On-Resistance vs. Temperature

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case


**Fig 12a.** Unclamped Inductive Test Circuit

**Fig 12b.** Unclamped Inductive Waveforms

**Fig 13a.** Basic Gate Charge Waveform

**Fig 13b.** Gate Charge Test Circuit

**Fig 12c.** Maximum Avalanche Energy vs. Drain Current

**Fig 14.** Threshold Voltage vs. Temperature



**Fig 15.** Typical Avalanche Current vs. Pulsewidth



**Fig 16.** Maximum Avalanche Energy vs. Temperature

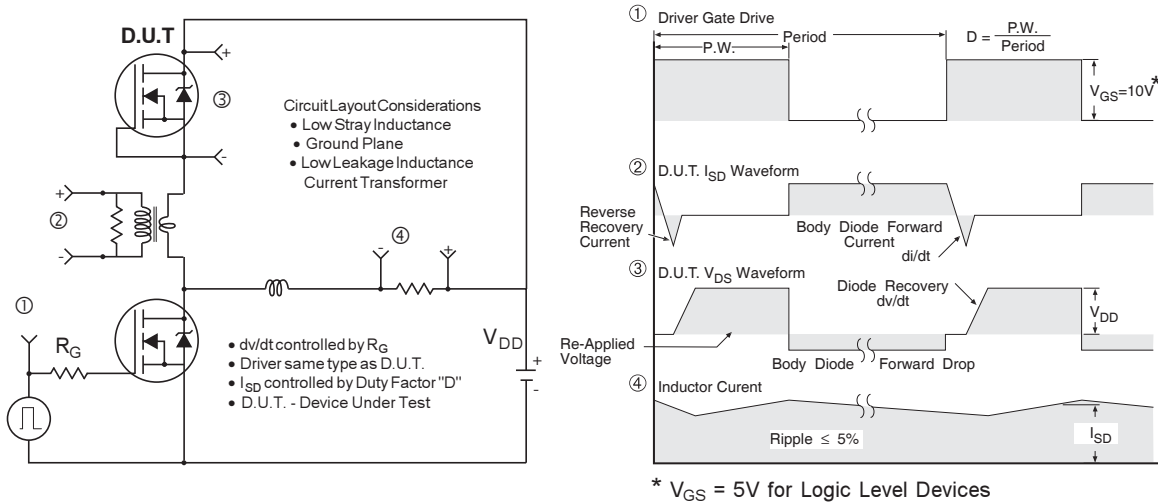
**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

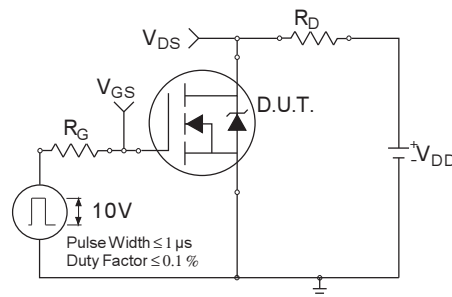
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

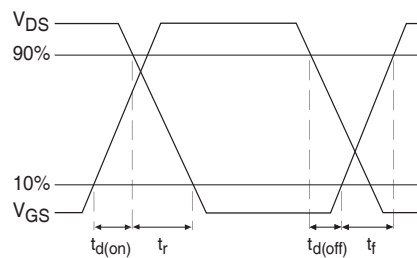
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



**Fig 18a. Switching Time Test Circuit**

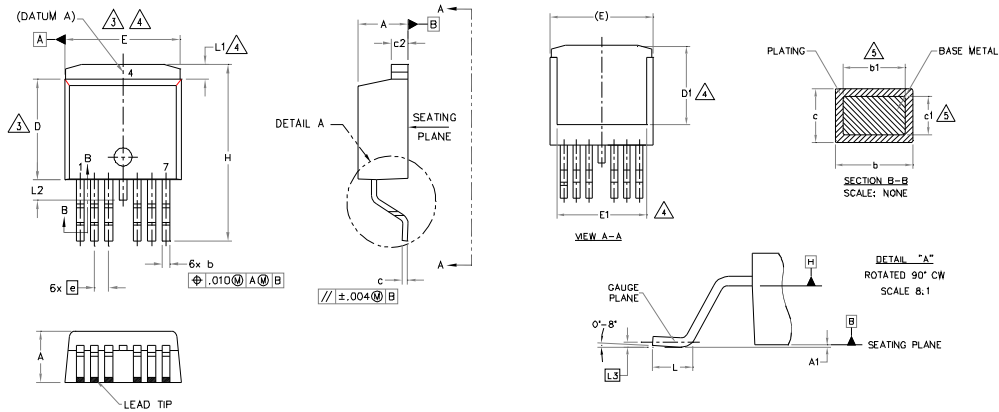


**Fig 18b. Switching Time Waveforms**



## D<sup>2</sup>Pak - 7 Pin Package Outline

Dimensions are shown in millimeters (inches)

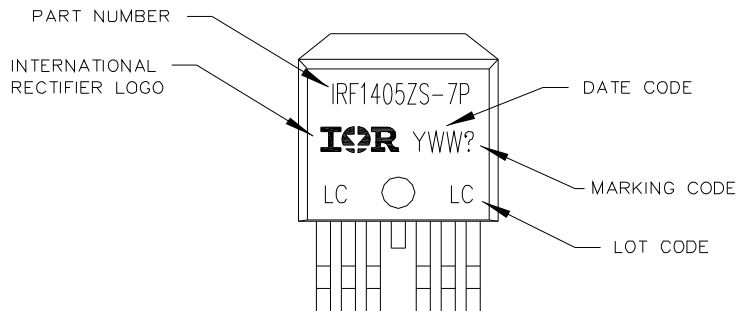


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	—	0.254	—	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	7.42	.270	.292	
E	9.65	10.54	.380	.415	
E1	6.22	8.48	.245	.334	4
e	1.27 BSC		.050 BSC		
H	14.61	15.88	.575	.625	4
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

- NOTES:
- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
  - DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  - $\Delta 3$  DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
  - $\Delta 4$  THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  - $\Delta 5$  DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  - DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
  - CONTROLLING DIMENSION: INCH.
  - OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB. EXCEPT FOR DIMS. E, E1 & D1.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

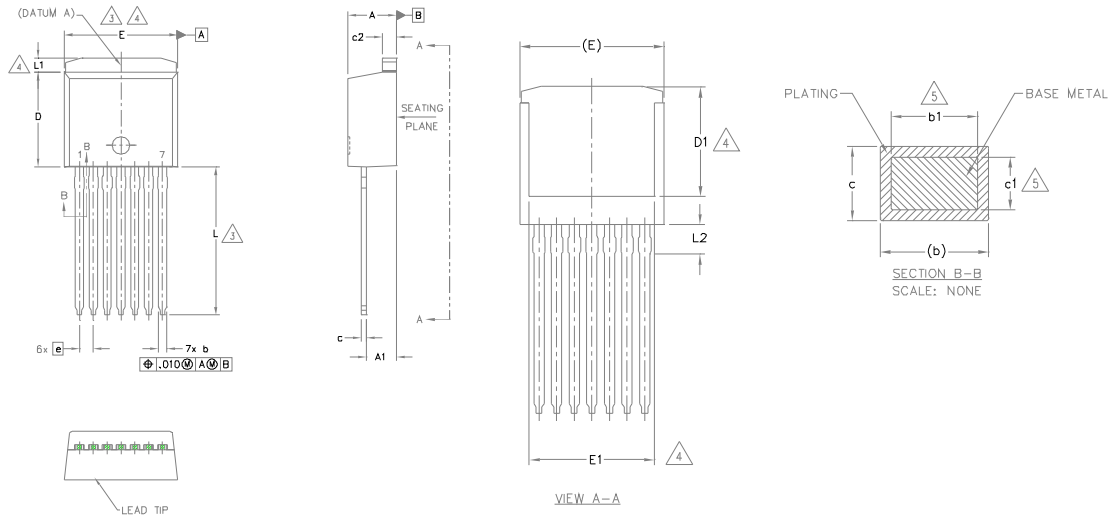
## D<sup>2</sup>Pak - 7 Pin Part Marking Information



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

## TO-263CA 7 Pin Long Leads Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
- 7.- OUTLINE CONFORM TO JEDEC TO-263 CA EXCEPT FOR DIMS. E, E1 & D1.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.91	.020	.036	
b1	0.51	0.81	.020	.032	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.51	9.65	.335	.380	3
D1	6.86	7.42	.270	.292	4
E	9.65	10.54	.380	.415	3,4
E1	6.22	8.48	.245	.334	4
e	1.27	BSC	.050	BSC	
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	-	6.35	-	.250	

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- SOURCE
- 3.- SOURCE
- 4.- DRAIN
- 5.- SOURCE
- 6.- SOURCE
- 7.- SOURCE

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

## D<sup>2</sup>Pak - 7 Pin Tape and Reel

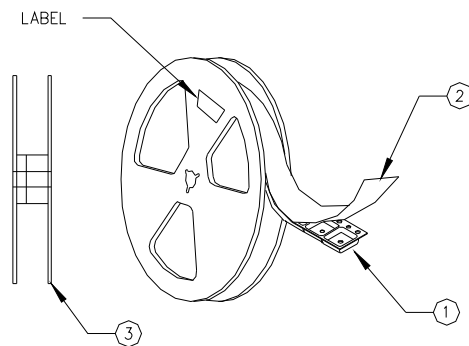
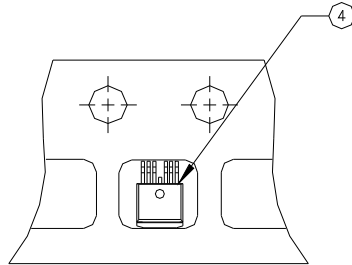
### NOTES, TAPE & REEL, LABELLING:

#### 1. TAPE AND REEL.

- 1.1 REEL SIZE 13 INCH DIAMETER.
- 1.2 EACH REEL CONTAINING 800 DEVICES.
- 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
- 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
- 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
- 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.

#### 2. LABELLING (REEL AND SHIPPING BAG).

- 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXSTRL-7P
- 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXSTRL-7P
- 2.3 I.R. PART NUMBER: IRFXXXSTRL-7P
- 2.4 QUANTITY:
- 2.5 VENDOR CODE: IR
- 2.6 LOT CODE:
- 2.7 DATE CODE:



**Note:** For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

**Qualification information<sup>†</sup>**

Qualification level	Industrial <sup>††</sup>	
	(per JEDEC JESD47F <sup>†††</sup> guidelines)	
Moisture Sensitivity Level	D <sup>2</sup> Pak-7PIN	MSL1 (per JEDEC J-STD-020D <sup>††</sup> )
	TO-263CA 7Pin	
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site:

<http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
10/29/2014	<ul style="list-style-type: none"> <li>• Updated data sheet with IR corporate template.</li> <li>• Updated D2-Pak 7-Pin ordering information to reflect the End-Of-life of the Tube packaging option (EOL notice #289)</li> <li>• Removed TO-263CA package (EOL notice # 288).</li> <li>• Removed <math>R_{\theta JA} = 62 \text{ }^{\circ}\text{C/W}</math> &amp; <math>R_{\theta CS} = 0.5 \text{ }^{\circ}\text{C/W}</math> from thermal resistance table on page 1( does not apply to D2-Pak 7- Pin).</li> <li>• Updated part marking on page 9 .</li> </ul>

International  
 Rectifier

**IR WORLD HEADQUARTERS:** 101 N. Sepulveda Blvd., El Segundo, California 90245, USA

To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>