CoolRunner XPLA3 CPLD Automotive IQ Product Family Introduction and Ordering

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Advance Product Specification

Features

- Guaranteed to meet full electrical specifications over T_A = –40°C to +125°C
- Technology: 0.35 µm EEPROM process
- Full Boundary Scan Test (IEEE 1149.1) for flexible in-system device and system testing
- Fast programming times in production saves time and money
  - Increases system reliability through reduced device handling
- High-speed pin-to-pin delays of 10 ns (100 MHz)
- Slew rate control per output to reduce EMI
- 100% routable which enables all device resources to be utilized

Family Overview

The CoolRunner™ XPLA3 (extended Programmable Logic Array) Automotive IQ product family of CPLDs is targeted for low power systems that include portable, handheld, automotive, and power sensitive applications. Each member of the XPLA3 family includes Fast Zero Power™ (FZP) design technology that combines low power and high speed. With this design technique, the XPLA3 family delivers power that is less than 100 µA at standby without the need for "turbo bits" or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any other CPLD. CoolRunner devices are the only TotalCMOS PLDs, as they use both a CMOS process technology and the patented full CMOS FZP design technique.

The CoolRunner XPLA3 family employs a full PLA structure for logic allocation within a functon block. The PLA provides maximum flexibility and logic density, with superior pin locking capability, while maintaining deterministic timing.

XPLA3 CPLDs are supported by WebPACK™ and WebFITTER™ from Xilinx and industry standard CAE tools (Cadence/OrCAD, Exemplar Logic, Mentor, Synopsys, ViewLogic, and Synplicity), using text (ABEL, VHDL, Verilog) and schematic capture design entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms.

The XPLA3 family features also include industry-standard, IEEE 1149.1, JTAG interface through which boundary-scan testing and In-System Programming (ISP) and reprogramming of the device can occur. The XPLA3 CPLD is electrically reprogrammable using industry standard device programmers.

Table 1: **CoolRunner XPLA3 Device Family**

	XCR3032XL	XCR3064XL	XCR3128XL	XCR3256XL	XCR3384XL	XCR3512XL
Macrocells	32	64	128	256	384	512
Usable Gates	750	1,500	3,000	6,000	9,000	12,000
Registers	32	64	128	256	384	512
F_{SYSTEM} (MHz)	95	95	95	88	87	77

Table 2: **CoolRunner XPLA3 Packages and User I/O Pins**

	XCR3032XL	XCR3064XL	XCR3128XL	XCR3256XL	XCR3384XL	XCR3512XL
44-pin VQFP	36	36	-	-	-	-
100-pin VQFP	-	68	84	-	-	-
144-pin TQFP	-	-	108	120	-	-
208-pin PQFP	-	-	-	164	172	180

Absolute Maximum Ratings(1)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage(2) relative to GND	–0.5	4.0	V
V_I	Input voltage(3) relative to GND	–0.5	5.5(4)	V
I_{OUT}	Output current, per pin	–100	100	mA
T_J	Maximum junction temperature	–40	150	°C
T_{STR}	Storage temperature	–65	150	°C

Notes:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage must rise monotonically.
3. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to 7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
4. External I/O voltage may not exceed V_{CC} by 4.0V.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient temperature	–40	+125	°C
V_{CC}	Supply voltage	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	5.5	V
V_O	Output voltage	0	V_{CC}	V
T_R	Input rise time	-	20	ns
T_F	Input fall time	-	20	ns

Quality and Reliability Characteristics

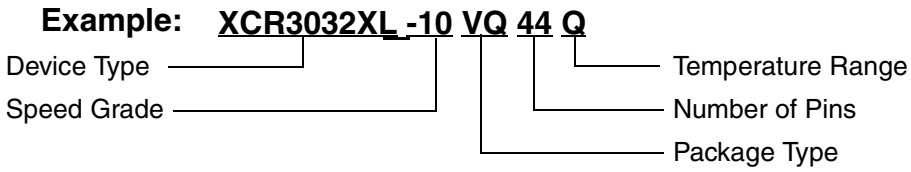
Symbol	Parameter	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/erase cycles (Endurance) @ T_A = 70°C	10,000	-	Cycles

Component Availability

Pins		44	100	144	208
Type		Plastic VQFP	Plastic VQFP	Plastic TQFP	Plastic PQFP
Code		VQ44	VQ100	TQ144	PQ208
XCR3032XL	-10	Q	-	-	-
XCR3064XL	-10	Q	Q	-	-
XCR3128XL	-10	-	Q	Q	-
XCR3256XL	-12	-	-	Q	Q
XCR3384XL	-12	-	-	-	Q
XCR3512XL	-12	-	-	-	Q

Notes:
1. Q = Automotive IQ (T_A = –40°C to +125°C).

Ordering Information



Device Ordering Options

Device
XCR3032XL
XCR3064XL
XCR3128XL
XCR3256XL
XCR3384XL
XCR3512XL

Speed	
-10	10 ns pin-to-pin delay
-12	12 ns pin-to-pin delay

Package	
VQ44	44-pin Quad Flat Pack (VQFP)
VQ100	100-pin Quad Flat Pack (VQFP)
TQ144	144-pin Plastic Quad Flat Pack (TQFP)
PQ208	208-pin Plastic Quad Flat Pack (PQFP)

Temperature	
Q = Automotive IQ	T_A = –40°C to +125°C

For more details about the CoolRunner XPLA3 Automotive devices, refer to the individual specifications:

DS119, *XCR3032XL Data sheet*

DS119-1, *XCR3064XL Data sheet*

DS119-2, *XCR3128XL Data sheet*

DS119-3, *XCR3256XL Data sheet*

DS119-4, *XCR3384XL Data sheet*

DS119-5, *XCR3512XL Data sheet*

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/17/02	1.0	Initial Xilinx release.
02/10/03	1.1	Updated F_{STSTEM} for XCR3384XL from 83 to 87 MHz.
05/07/03	1.2	Added 120 I/O to XCR3256XL in Table 2.
10/18/04	1.3	Added "Not to be used in new designs" watermark; moved to "Mature Products"