

# FDP51N25 / FDPF51N25

## N-Channel UniFET™ MOSFET

500 V, 51 A, 60 mΩ

### Features

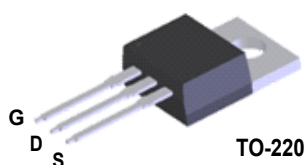
- $R_{DS(on)} = 60 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 25.5 \text{ A}$
- Low Gate Charge (Typ. 55 nC)
- Low Crss (Typ. 63 pF)

### Applications

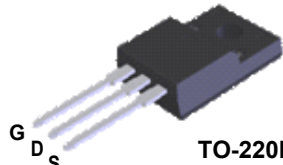
- PDP TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

### Description

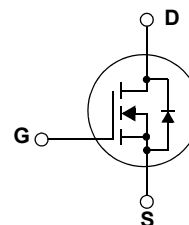
UniFET™ MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



TO-220



TO-220F



### Absolute Maximum Ratings

Symbol	Parameter		FDP51N25	FDPF51N25	Unit
$V_{DSS}$	Drain-Source Voltage		250		V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	51	51*	A
		- Continuous ( $T_C = 100^\circ\text{C}$ )	30	30*	A
$I_{DM}$	Drain Current	- Pulsed (Note 1)	204	204*	A
$V_{GSS}$	Gate-Source voltage		$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)		1111		mJ
$I_{AR}$	Avalanche Current (Note 1)		51		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)		32		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5		V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	320	38	W
		- Derate above $25^\circ\text{C}$	3.7	0.3	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150		$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300		$^\circ\text{C}$

\*Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	FDP51N25	FDPF51N25	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.39	3.3	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.5	--	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP51N25	FDP51N25	TO-220	-	-	50
FDPF51N25	FDPF51N25	TO-220F	-	-	50

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

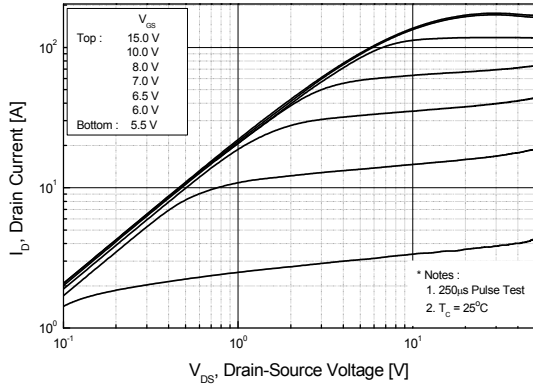
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA, T <sub>J</sub> = 25°C	250	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	--	0.25	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 250V, V <sub>GS</sub> = 0V V <sub>DS</sub> = 200V, T <sub>C</sub> = 125°C	--	--	1 10	μA μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 25.5A	--	0.048	0.060	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40V, I <sub>D</sub> = 25.5A	--	43	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz	--	2620	3410	pF
C <sub>oss</sub>	Output Capacitance		--	530	690	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	63	90	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 125V, I <sub>D</sub> = 51A R <sub>G</sub> = 25Ω	--	62	135	ns
t <sub>r</sub>	Turn-On Rise Time		--	465	940	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	98	205	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	--	130	270
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 200V, I <sub>D</sub> = 51A V <sub>GS</sub> = 10V	--	55	70	nC
Q <sub>gs</sub>	Gate-Source Charge		--	16	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		(Note 4)	--	27	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	51	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	204	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 51A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>S</sub> = 51A di <sub>f</sub> /dt = 100A/μs	--	178	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	4.0	--	μC

### Notes:

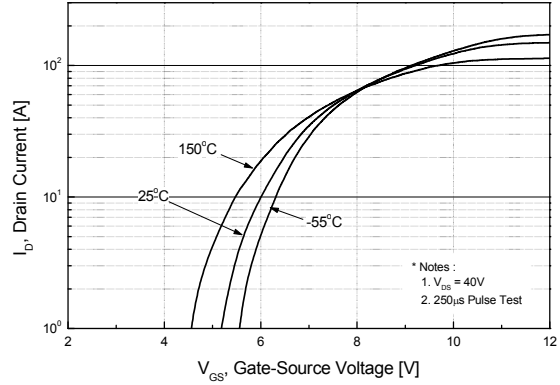
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 0.68mH, I<sub>AS</sub> = 51A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 51A, di<sub>f</sub>/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C
4. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

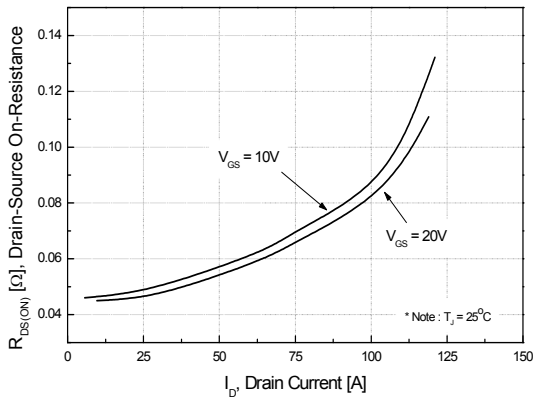
**Figure 1. On-Region Characteristics**



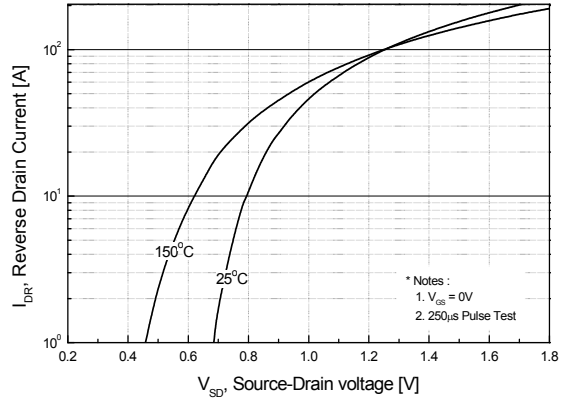
**Figure 2. Transfer Characteristics**



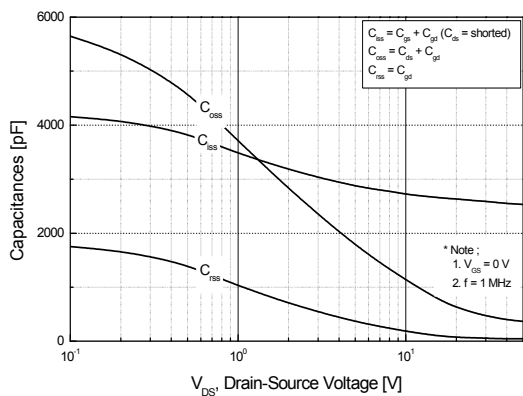
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



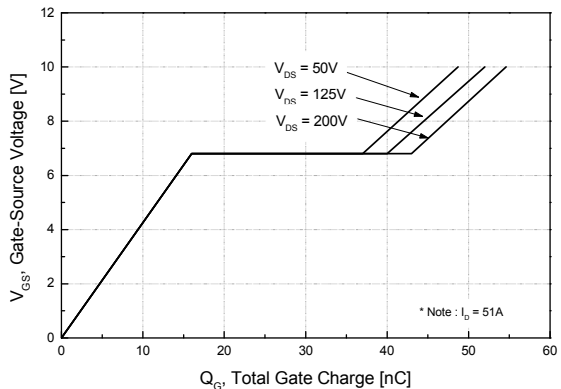
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

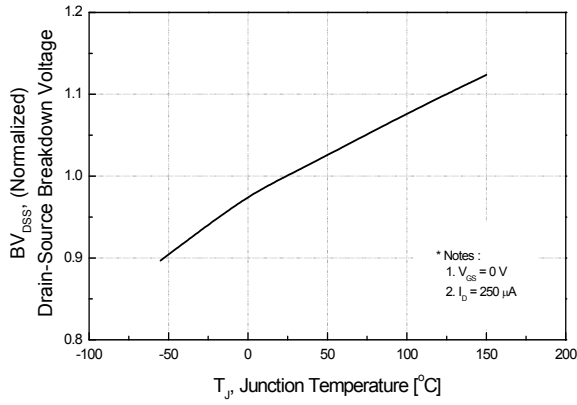


**Figure 6. Gate Charge Characteristics**

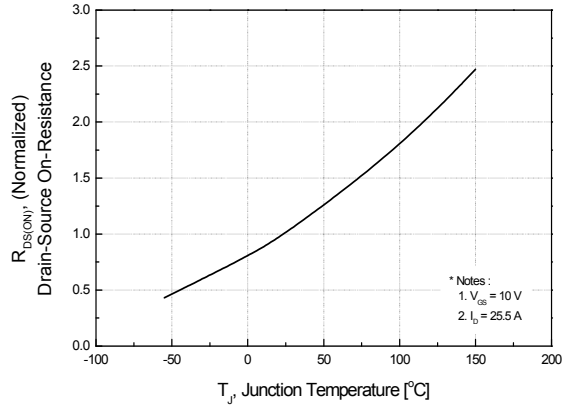


**Typical Performance Characteristics** (Continued)

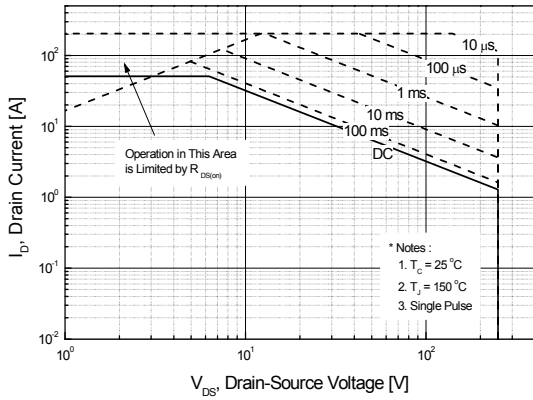
**Figure 7. Breakdown Voltage Variation vs. Temperature**



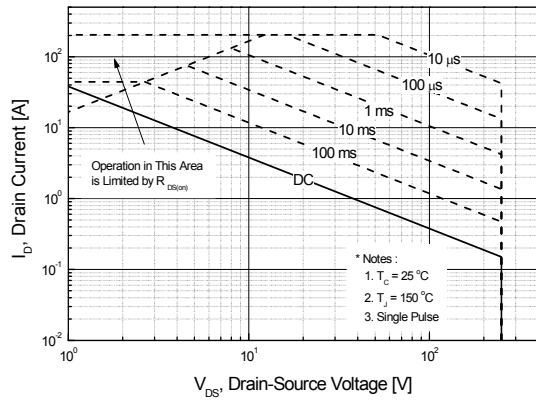
**Figure 8. On-Resistance Variation vs. Temperature**



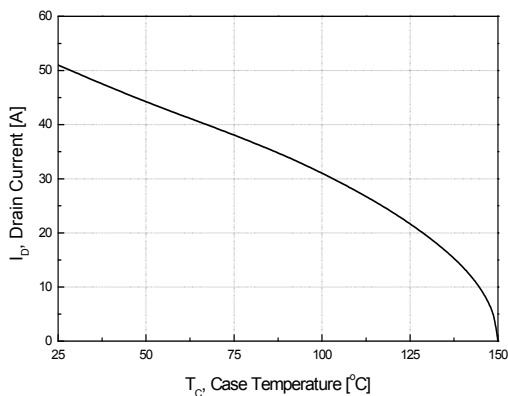
**Figure 9-1. Maximum Safe Operating Area for FDP51N25**



**Figure 9-2. Maximum Safe Operating Area for FDPF51N25**



**Figure 10. Maximum Drain Current vs. Case Temperature**



Typical Performance Characteristics (Continued)

Figure 11-1. Transient Thermal Response Curve for FDP51N25

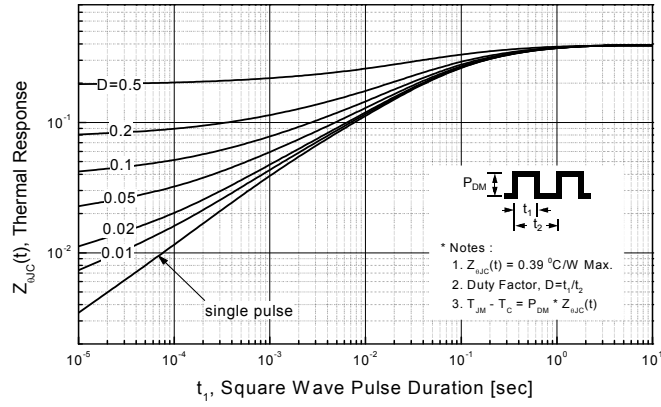
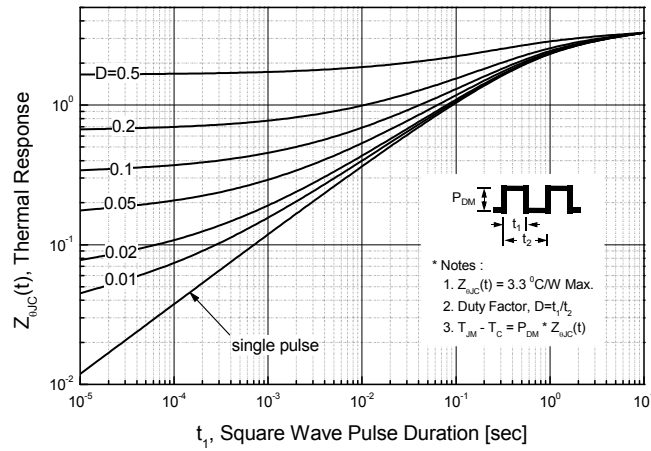
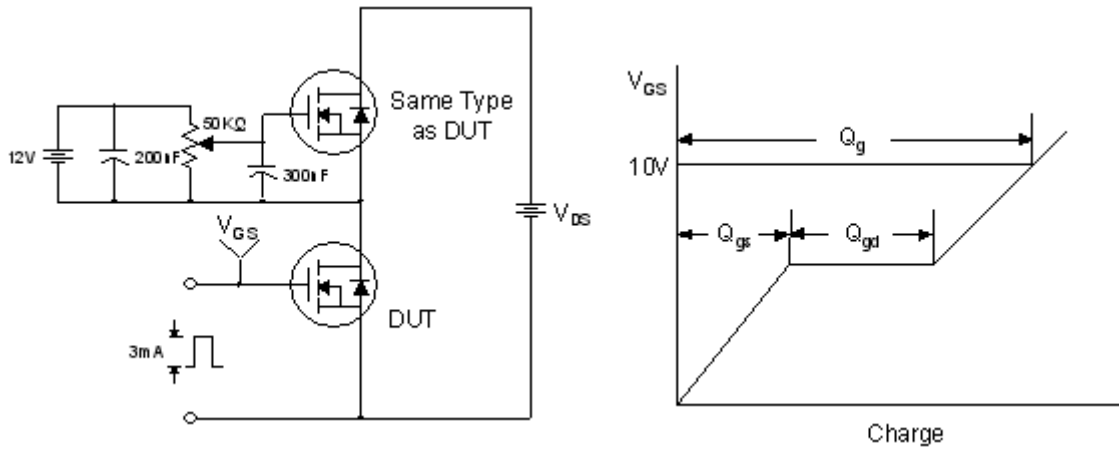


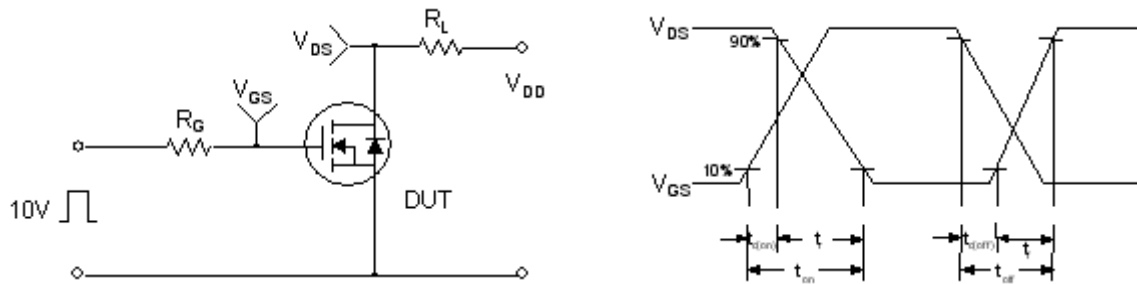
Figure 11-2. Transient Thermal Response Curve for FDPF51N25



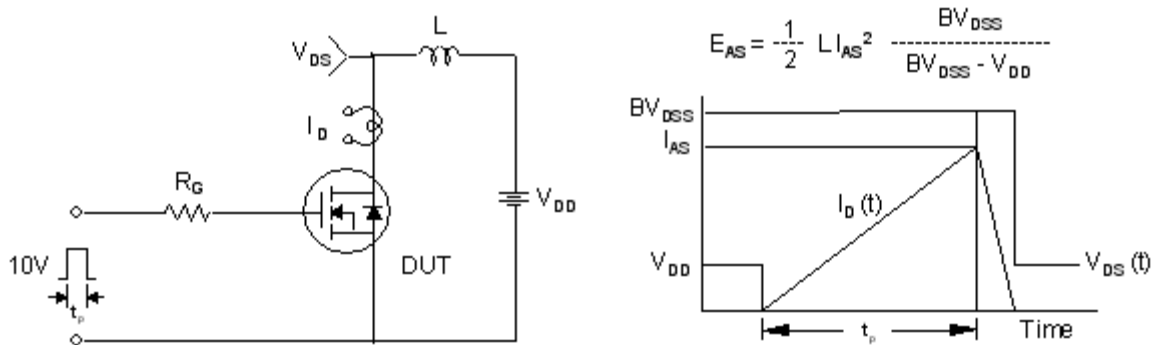
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

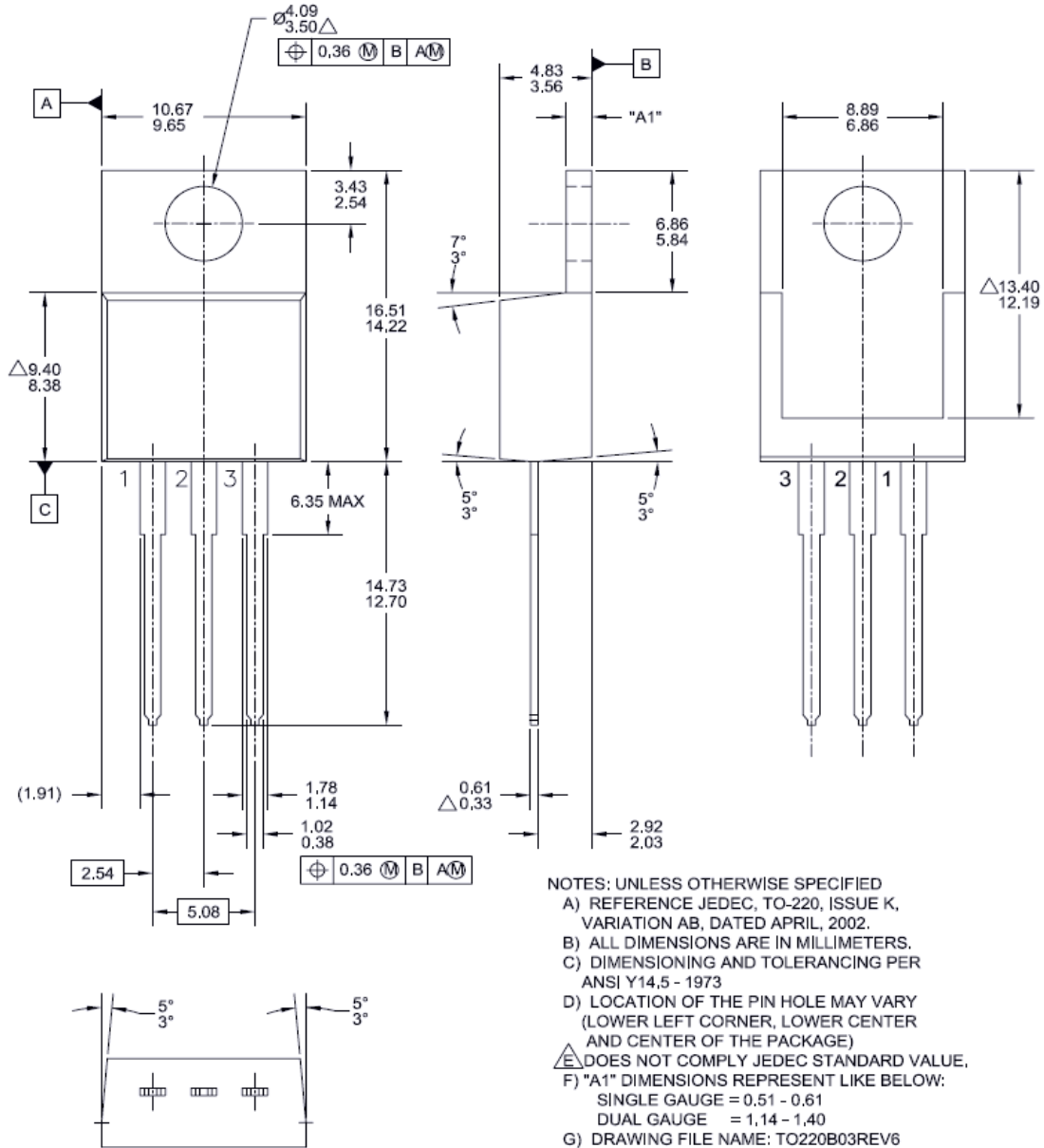


Peak Diode Recovery dv/dt Test Circuit & Waveforms



**Mechanical Dimensions**

**TO-220B03**

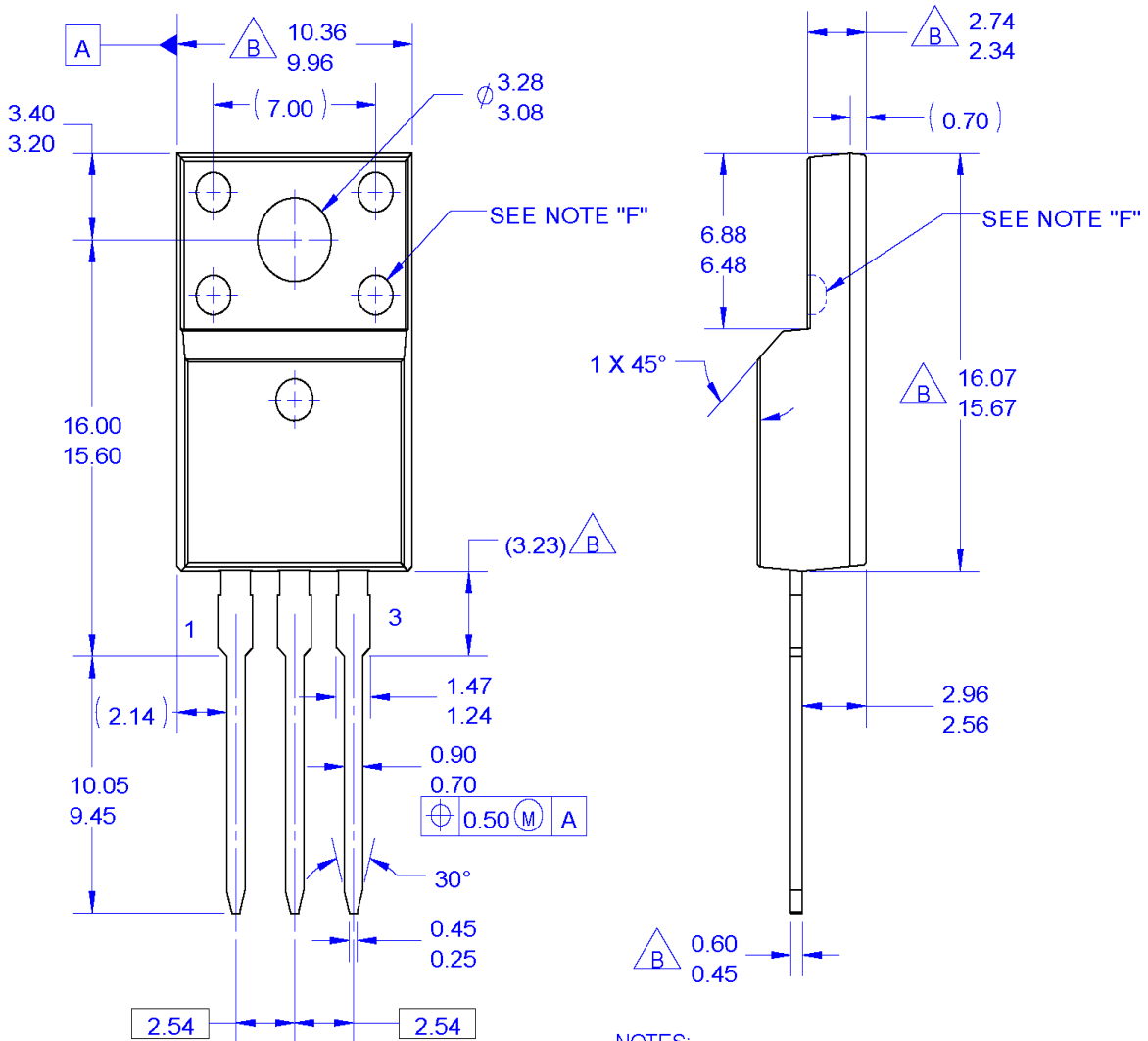


Dimensions in Millimeters



**Mechanical Dimensions** (Continued)

**TO-220M03**



**NOTES:**

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.  
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3

Dimensions in Millimeters



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| BitSiC™                  | Global Power Resource™                          | TinyBuck™        |
| Build it Now™            | Green Bridge™                                   | TinyCalc™        |
| CorePLUS™                | Green FPS™                                      | TinyLogic®       |
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|                          | QS™   |                  |
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|                          | SuperSOT™-6                                     |                  |
|                          | SuperSOT™-8                                     |                  |
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I64