100234D
November 1, 2000

Bt8953A/ RS8953B

product bulletin

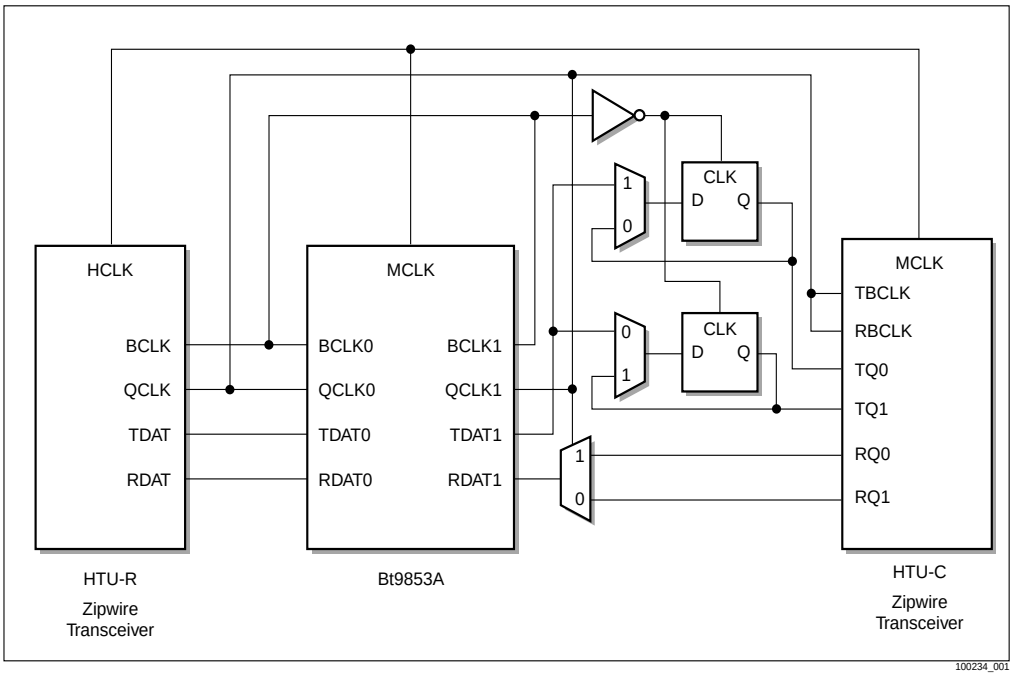
Product Affected: **Bt8953A, RS8953B**

BCLK Phase Constraints In Repeater Mode; Non-Conformance

While in repeater mode (REPEAT_EN = 1 for CH1 & CH2), a BCLK1 to BCLK2 phase difference of 180 degrees, +/- 5 nSec, will result in corrupted data transfer. All other phase relationships are acceptable.

In a repeater-mode application, to prevent a phase difference of 180 degrees between BCLK1 and BCLK2, the same clock is feed to both BCLK1 and BCLK2. To use the same clock for both HDSL transceivers, one HDSL transceiver needs to be slaved to the other HDSL transceiver. This is accomplished by setting the HDSL transceiver, which is configured as HTU-C, to “parallel slave mode”. Then the parallel signals, from the HDSL transceiver, need to be externally converted to “serial, sign first mode” to interface to the Bt8953A/RS8953B.

To configure the Zipwire transceiver to “parallel slave mode”, address 0x06 of the Zipwire transceiver needs to be modified. Also to align the sign and magnitude data correctly, the tbclk_pol and rbclk_pol needs to set properly. The tbclk_pol and rdbclk_pol are controlled by address 0x06 of the Zipwire transceiver. TQ[1,0] should be sampled on the falling edge of TBCLK. RQ[1,0] should be sampled on the falling edge of RBCLK.


HCLK
BCLK
QCLK
TDAT
RDAT
HTU-R
Zipwire
Transceiver
MCLK
BCLK0
QCLK0
TDAT0
RDAT0
BCLK1
QCLK1
TDAT1
RDAT1
Bt9853A
1
0
CLK
D
Q
0
1
CLK
D
Q
1
0
MCLK
TBCLK
RBCLK
TQ0
TQ1
RQ0
RQ1
HTU-C
Zipwire
Transceiver
100234_001