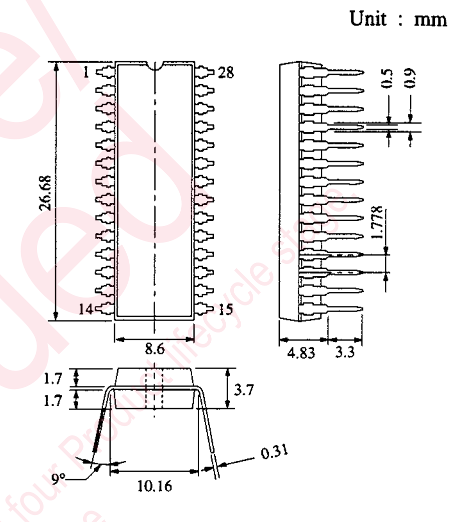
AN5818NK

U.S. TV Multiplex Sound System Demodulation

■ Description

The AN5818K is an integrated circuit consisting of a Multiplex Sound Decoder and dbx Noise Reduction for use in Sound Processing of TV signal.

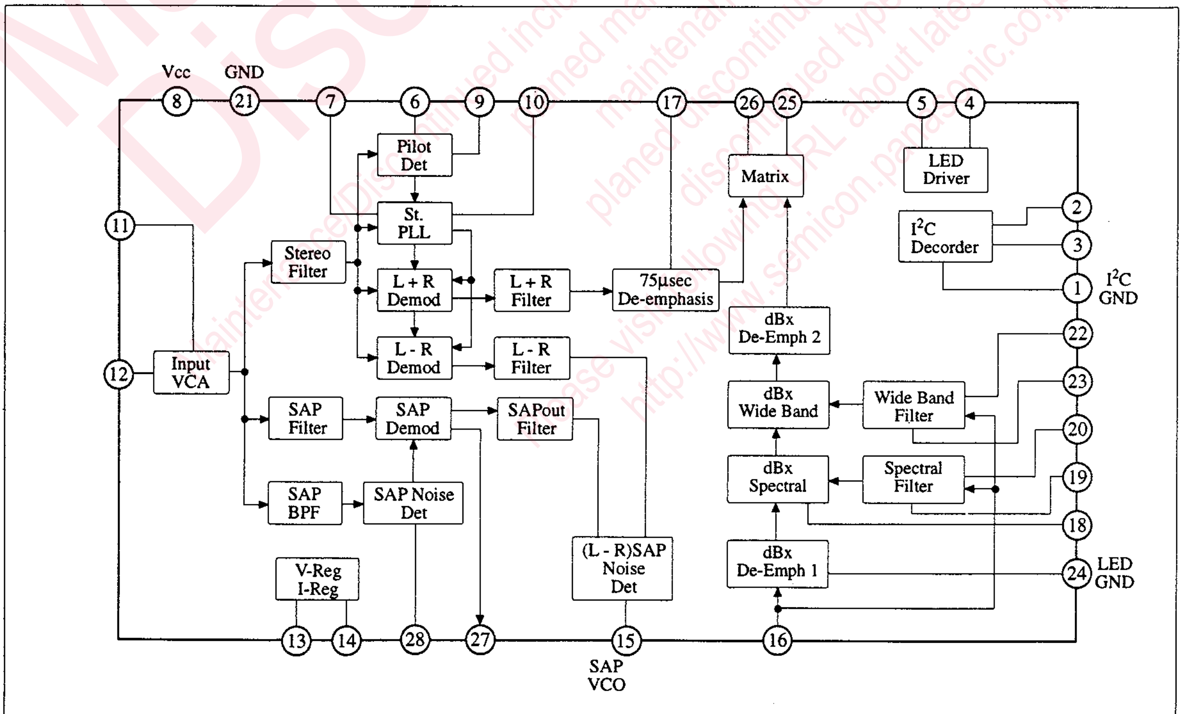


28-Lead Shrunk DIL Plastic Package

■ Features

- Audio multiplex TV demodulation and dbx Noise Reduction circuits are configured on One Chip
- Operating supply voltage correspondent to TV, VTR (8.5V ~ 9.5V)
- Built-in SAP multifunction recognition circuit
- Pilot cancel circuit using new-quasi/SINE waveform generation circuit
- Built-in LED driver for Stereo and SAP
- I²C bus control for the following : Input Amp. gain, VCO adjustment, Filter adjustment, Low-pass separation and High-pass separation.

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	Vcc	11.0	V
Supply Current	Icc	75	mA
Power Dissipation (Ta=75°C)	P_D	1143	mW
Operating Ambient Temperature	Topr	-20 ~ +75	°C
Storage Temperature	Tstg	-55 ~ +150	°C

■ Recommended Operating Range (Ta=25°C)

Item	Symbol	Range
Operating Supply Voltage Range	Vcc	8.5V ~ 9.5V

■ Electrical Characteristics (Ta=25°C)

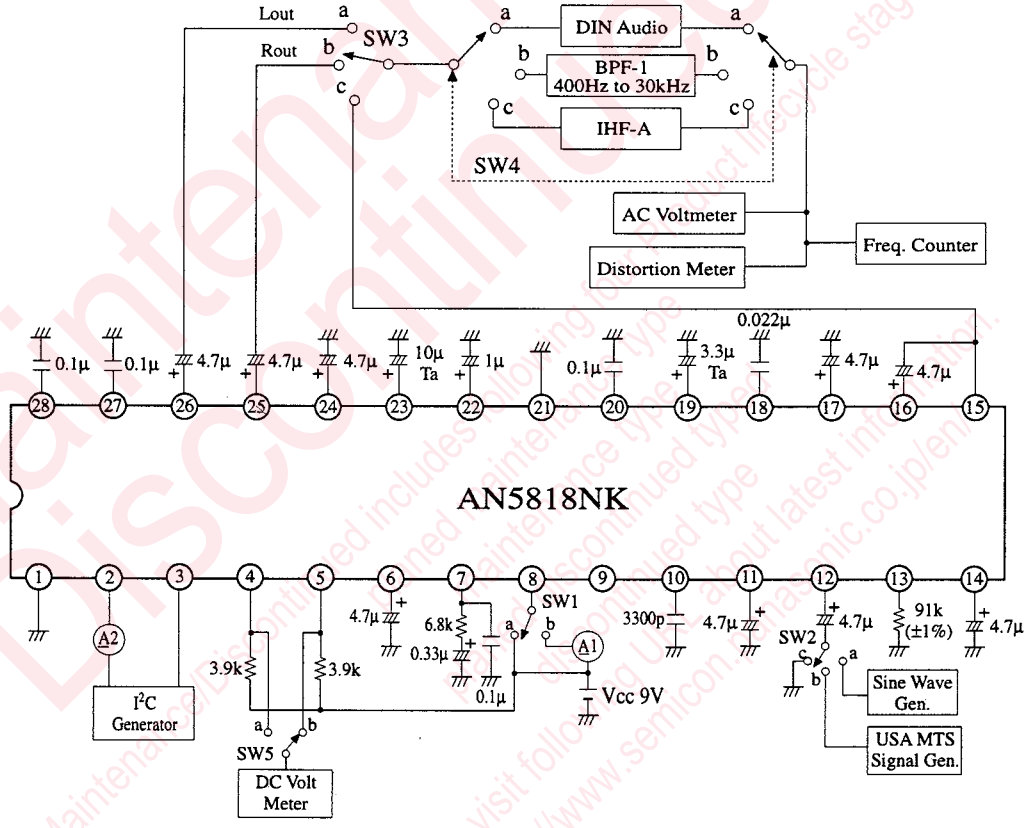
Item	Symbol	Test cct	Condition	min.	typ.	max.	Unit
Total circuit current	I_{CC}	1	No signal	35	55	75	mA
Mono output level	$V_{O(MONO)}$	1	f=1kHz (Mono) 100% mod	480	530	580	mVrms
Mono frequency characteristic-1	$V_{1(MONO)}$	1	f=300Hz (Mono) 30% mod	-0.5	0	+0.5	dB
Mono frequency characteristic-2	$V_{2(MONO)}$	1	f=8kHz (Mono) 30% mod	-1.5	-0.4	+0.4	dB
Mono distortion rate	$THD_{(MONO)}$	1	f=1kHz (Mono) 100% mod			0.7	%
Mono noise level	$V_{n(MONO)}$	1	Input short BPF (A curve)			-60	dBV
(L), (R) output voltage difference	$V_{LR(MONO)}$	1	f=1kHz (Mono) 100% mod	-0.5	0	+0.5	dB
Stereo output level	$V_{O(st)}$	1	f=1kHz, [L(R)-only] 100% mod	420	520	620	mVrms
Stereo freq. characteristic-1	$V_{1(st)}$	1	f=300Hz, [L(R)-only] 30% mod	-0.7	0	+0.7	dB
Stereo freq. characteristic-2	$V_{2(st)}$	1	f=3kHz, [L(R)-only] 30% mod	-1	0	+1	dB
Stereo freq. characteristic-3	$V_{3(st)}$	1	f=8kHz, [L(R)-only] 30% mod	-2.5	-1.3	0	dB
Stereo distortion rate	$THD_{(st)}$	1	f=1kHz, [L(R)-only] 100% mod			1.0	%
Stereo noise level	Vn(st)	1	f=15.73kHz (f_H), υ=0.084Vpp, BPF			-60	dBV
Stereo discrimination level	$V_{TH(st)}$	1	f=15.73kHz(fH)	8	16	24	mVrms
Stereo discrimination hysteresis	$V_{HY(st)}$	1	f=15.73kHz(fH)	-4		-0.5	dB
SAP output level	$V_{O(SAP)}$	1	f=1kHz, (SAP) 100% mod	390	560	790	mVrms
SAP frequency characteristic-1	$V_{1(SAP)}$	1	f=300Hz, (SAP) 30% mod	-1.0	0	1.0	dB
SAP frequency characteristic-2	$V_{2(SAP)}$	1	f=3kHz, (SAP) 30% mod	-3.5	-1.8	0	dB
SAP distortion rate	$THD_{(SAP)}$	1	f=1kHz, (SAP) 100%			1.5	%
SAP noise level	Vn(SAP)	1	f=78.7kHz (fH), υ=0.42Vpp, BPF			-65	dBV
SAP discrimination level	$V_{TH(SAP)}$	1	f=78.7kHz(5fH)	20		48	mVrms
SAP discrimination hysteresis	$V_{HY(SAP)}$	1	f=78.7kHz(5fH)	-4.0		-0.5	dB
SAP→Stereo crosstalk	CT_1	1	(SAP) 1kHz, 100% mod (Stereo) pilot-signal			-50	dB
Stereo→SAP crosstalk	CT_2	1	(Stereo) 1kHz, 100% mod (SAP) carrier-signal			-50	dB

Note : Vcc=9V, Stereo PLL VCO Adjustment : 15.734kHz ±50Hz
Input Level (100% mod.) : L+R = 0.424Vpp (pre-emphasis OFF), L-R = 0.848Vpp (dbx-NR OFF),
Pilot = 0.084Vpp, SAP = 0.254Vpp (dbx-NR OFF)

■ Electrical Characteristics (Ta=25°C)(Continue)

Item	Symbol	Test cct	Condition	min.	typ.	max.	Unit
I²C interface							
Suction current during ACK	I_{ACK}	1	Max. suction current value of pin 2 during ACK	2.0	10	20	mA
SCL, SDA signal input High Level	V_{IHI}	1		3.5		5.0	V
SCL, SDA signal input Low Level	V_{ILO}	1		0		0.9	V
Max. frequency allowable to input	f_{imax}	1				100	kbit/s

Test Circuit 1



Note : (Ta) Tantalum capacitor

■ Description of test circuit and test method

No	Item	Symbol	SW					Input Conditions	Measurement
			1	2	3	4	5		
1	Total circuit current	I_{CC}	b	c	a	a	b	No signal	Value of DC Ampere Meter 1
2	Mono output level	$V_{O(MONO)}$	a	b	a/b	a	b	f=1kHz (Mono) 100% mod	Value of AC Volt Meter
3	Mono frequency characteristic-1	$V_{1(MONO)}$	a	b	a/b	a	b	f=300Hz (Mono) 30% mod	Level ratio V300Hz/V1kHz
4	Mono frequency characteristic-2	$V_{2(MONO)}$	a	b	a/b	a	b	f=8kHz (Mono) 30% mod	Level ratio V8kHz/V1kHz
5	Mono distortion rate	$THD_{(MONO)}$	a	b	a/b	b	b	f=1kHz (Mono) 100% mod	Value of Distortion Meter
6	Mono noise level	$V_{n(MONO)}$	a	c	a/b	c	b	No signal	Value of AC Volt Meter
7	(L), (R) output voltage difference	$V_{LR(MONO)}$	a	b	a/b	a	b	f=1kHz (Mono) 100% mod	Level ratio V(R)/V(L)
8	Stereo output level	$V_{O(st)}$	a	b	a/b	a	b	f=1kHz (L(R)-only) 100% mod	Value of AC Volt Meter
9	Stereo frequency characteristic-1	$V_{1(st)}$	a	b	a/b	a	b	f=300Hz (1kHz) (L(R)-only) 30% mod	Level ratio V300Hz/V1kHz
10	Stereo frequency characteristic-2	$V_{2(st)}$	a	b	a/b	a	b	f=3kHz (L(R)-only) 30% mod	Level ratio V3kHz/V1kHz
11	Stereo frequency characteristic-3	$V_{3(st)}$	a	b	a/b	a	b	f=8kHz (L(R)-only) 30% mod	Level ratio V8kHz/V1kHz
12	Stereo distortion rate	$THD_{(st)}$	a	b	a/b	b	b	f=1kHz (L(R)-only) 100% mod	Value of Distortion Meter
13	Stereo noise level	Vn(st)	a	b	a/b	c	b	Stereo pilot signal	Value of AC Volt Meter
14	Stereo discimination level	$V_{TH(st)}$	a	a	a	c	b	Increase the level from f=15.734kHz,5mVrms	Input level at which DC voltmeter value < 0.5V
15	Stereo discrimination hysteresis	$V_{HY(st)}$	a	a	a	c	b	Decrease the above input signal level	Input level at which DC voltmeter value > 2.0V
16	SAP output level	$V_{O(SAP)}$	a	b	a/b	a	a	f=1kHz (SAP) 100% mod	Value of AC Volt Meter
17	SAP frequency characteristic-1	$V_{1(SAP)}$	a	b	a/b	a	a	f=300Hz (1kHz) SAP 30% mod	Level ratio V300Hz/V1kHz
18	SAP frequency characteristic-2	$V_{2(SAP)}$	a	b	a/b	a	a	f=3kHz (1kHz) SAP 30% mod	Level ratio V3kHz/V1kHz
19	SAP distortion rate	$THD_{(SAP)}$	a	b	a/b	b	a	f=1kHz SAP 100% mod	Value of Distortion Meter
20	SAP noise level	$V_{n(SAP)}$	a	b	a/b	c	a	SAP carrier (0% mod)	Value of AC Volt Meter
21	SAP discrimination level	$V_{TH(SAP)}$	a	a	a	a	b	Increase the level from f=78.7kHz, 10mVrms	Input level at which DC voltmeter value < 0.5V
22	SAP discrimination hysteresis	$V_{HY(SAP)}$	a	a	a	a	b	Decrease the above input signal level	Input level at which DC voltmeter value > 2.0V
23	SAP→Stereo crosstalk	CT_1	a	b	a/b	a	b	f=1kHz, (SAP) 100% mod + pilot signal	Ratio of the levels when the 05H register is 00H and 40H
24	Stereo→SAP crosstalk	CT_2	a	b	a/b	a	b	f=1kHz, L(R)-only 100% mod + SAP carrier (0% mod)	Ratio of the levels when the 05H register is 00H and 40H

■ I²C Bus

Adjustment method by using I²C

[Slave address] B4

[List of sub address]

Sub address	DAC name	No. of bit
00H	Input level adjustment	6 bit
01H	Stereo PLLVCO adjustment	6 bit
02H	Filter adjustment	6 bit
03H	Low-pass separation adjustment	6 bit
04H	High-pass separation adjustment	6 bit
05H	Miscellaneous switches	7 bit

[Adjustment method]

1. Stereo PLLVCO adjustment (Sub address : 01H)
   Set the 05H register to the ADJ1 mode.
   Adjust the 01H register so as the frequency of the R output signal to become 15.534kHz ± 50Hz.

2. Filter adjustment (Sub address : 02H)
   Apply a sinewave of 15.73kHz, 100mVrms to the input pin.
   Adjust the 02H register so as the L output level to become minimum.

3. Input level adjustment (Sub address : 00H)
   Set the 05H register to 08H. Apply a sinewave of 300Hz, 150mVrms to the input pin. Adjust the 00H register so as the R output level to become 212mVrms ± 2mVrms.

4. Separation adjustment (Sub address : 03H and 04H)
   Set the 05H register to 00H. Apply the stereo L-only signal (300Hz, 300% mod) and adjust the 03H register so as the R output become minimum. Apply the stereo L-only signal (3kHz, 30% mod) and adjust the 04H register so as the R output to become minimum. Again set to 300Hz, adjust the 03H register.

5. Miscellaneous switches (Sub address : 05H)

Mode	Data								Lout Pin 26	Rout Pin 25	Note
	MSB							LSB			
	D7	D6	D5	D4	D3	D2	D1	D0			
ADJ1	0	0	0	0	0	0	0	1	L+R Filter output	VCO output f_H	Note 1
ADJ2	0	0	0	0	1	0	0	0	Mute	Input VCA output	Note 2
Mono	0	0	0	1	0	0	0	0	L + R	L + R	Note 3
LED	0	0	0	1	0	1	0	0			Note 4

Note1) ADJ1 mode
Note2) ADJ2 mode
Note3) Forced Mono
Note4) LED/OFF at Forced Mono

[05H Register Data]

D0 SW 1 for initial adjustment (0 : OFF, 1 : ON)
D1 Unused
D2 Switching the LED ON/OFF at forced Mono (0 : ON, 1 : OFF)
D3 SW2 for initial adjustment (0 : OFF, 1 : ON)
D4 Forced Mono switch (0 : OFF, 1 : ON)
D5 Switching L/R output at SAP (0 : L=R=SAP, 1 : L=L+R, R=SAP)
D6 Switching Stereo / SAP (0 : SAP, 1 : Stereo)
D7 Unused

■ I²C Bus

Mode table

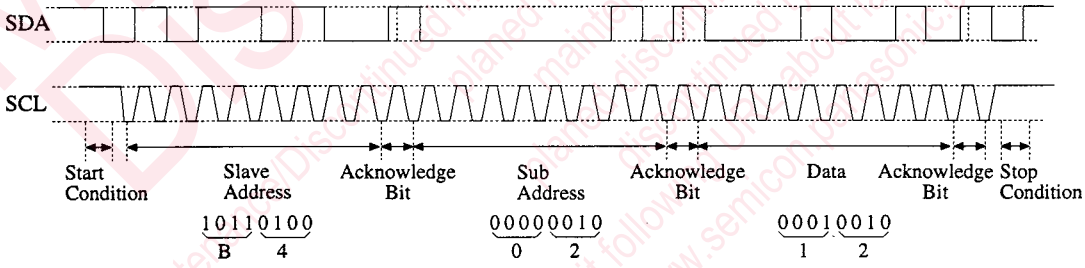
Input Signal	05H register	L_{out} Pin 26	R_{out} Pin 25
Stereo	00	L	R
	20	L	R
	40	L	R
	60	L	R
SAP	00	SAP	SAP
	20	L + R	SAP
	40	L + R	L + R
	60	L + R	L + R
Stereo + SAP	00	SAP	SAP
	20	L + R	SAP
	40	L	R
	60	L	R

[Signal detection]

Stereo or SAP received signal is detected by setting L or H at the LED pins. (L : ~1.1V, H : 3.9V~)

Received Signal	SAP LED Pin 4	Stereo LED Pin 5
Mono	H	H
Stereo	H	L
SAP	L	H
Stereo + SAP	L	L

<I²C Bus>



Example of transmission Message

For transmission messages, both SCL and SDA are transferred in the form of synchronized serial transimission. SCL is a clock of a specific frequency, and SDA indicates address data for controlling the receiving side and is transferred in parallel, being synchronized with SCL. Data is transferred in principle in 3 octets (bytes), and each one octet (one octet = 8 bits) includes one acknowledge bit. Frame structure is described below.

(a) Start Condition — The receiver becomes possible to receive data when SDA changes from Hi to Lo while SCL is Hi.
(b) Stop Condition — The receiver halts receiving when SDA changes from Lo to Hi while SCL is Hi.
(c) Slave Address — This is an address which is determined for each device. If other device address is sent, receiving will be halted.
(d) Sub Address — This is an address which is determine for each function.
(e) Data — This is control data.
(f) Acknowledge bit — This is a bit by which the master acknowledges that data was successfully received in each octet. Master sends the Hi signal and the receiver sends back the Lo signal as shown in Figure 3 with dotted line, causing the master to acknowledge the reception by the receiver. If the Lo signal is not returned, communication will be halted.

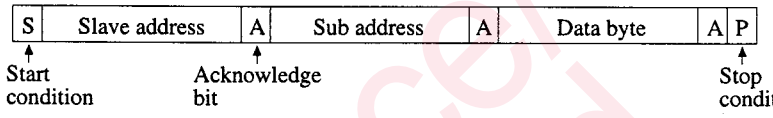
Except Start and Stop conditions, SDA does not change while SCL is Hi.

■ I²C Bus (Continue)

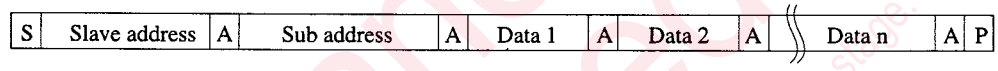
(1) This contains 5 DAC controls and 6 SWs, and promotes to eliminate set mechanical adjustments.

(2) This is provided with Auto-increment function.
- Sub address 0* : Auto-increment mode
(Sending data sequentially, sub address sequentially changes to input data.)
- Sub address 8* : Data update mode
(Sending data sequentially, data is inputted with the same sub address.)

(3) I²C BUS PROTOCOL
- Slave address :10110100 (B4H)
- Format (normal)



- Auto-increment mode / Data update mode



(4) Since the DAC initial status is not guaranteed, the standard data input is certainly necessary when power is turned ON.

- Sub address byte and Data byte format

Sub address	Upper MSB Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	← Input Level →					
01	0	0	← Stereo PLL VCO →					
02	0	0	← Filter Frequency Characteristic →					
03	0	0	← Low-pass separation →					
04	0	0	← High-pass separation →					
05	0	Stereo/SAP 0 → SAP	SAP/(L+R) 0 →L=R=SAP	Forced Mono 1 → ON	ADJ2 1 → ON	Forced Mono LED 0 → ON	0	ADJ1 1 → ON

1) 00H : Input Amp. gain
When Data = 00, 0.5dB
When Data = 3F, 5.5dB

2) 01H : VCO free-running frequency of stereo PLL
When Data = 00, -13%
When Data = 3F, +13%

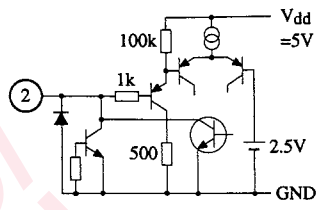
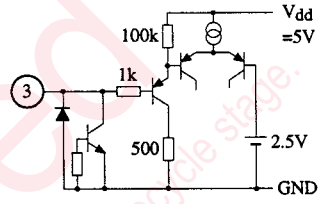
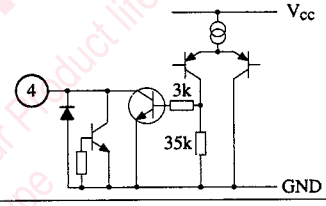
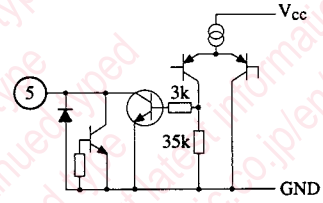
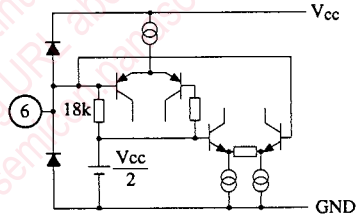
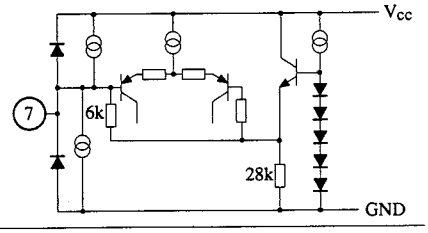
3) 02H : Filter frequency characteristics (wo)
When Data = 00, +25%
When Data = 3F, -25%

4) 03H : Low-pass separation
Adjusts separartion at low-pass (300Jz)

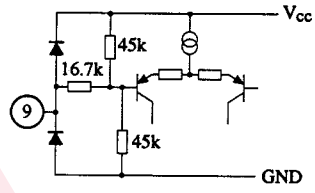
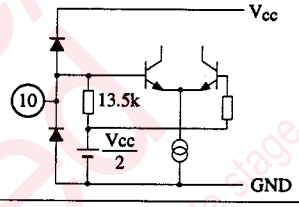
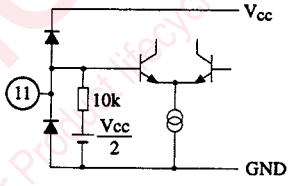
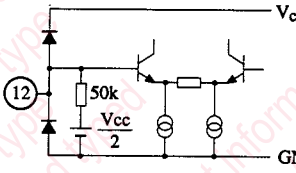
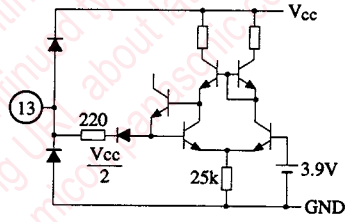
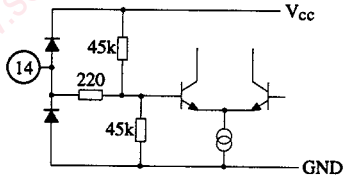
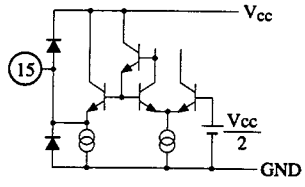
5) 04H : High-pass separation
Adjusts speparation at high-pass (3kHz)

<Electrostatic breakdown>
Pin 9, 23, 27 and 28 is at 200pF 170V level.

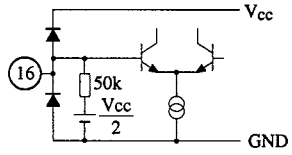
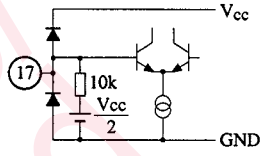
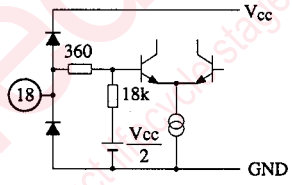
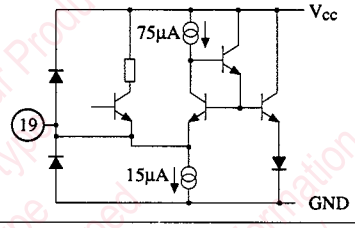
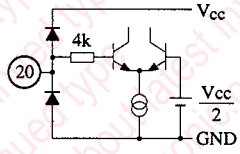
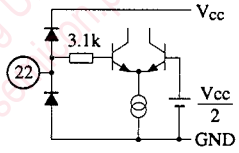
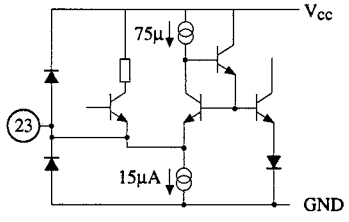
■ Pin Descriptions

Pin No.	Pin Name	Pin Description	Pin Voltage	Equivalent Circuit
1	I^2C GND	I^2C Bus, DAC GND pin.	0V	
2	SDA	I^2C Bus DATA input pin.		
3	SCL	I^2C Bus CLOCK input pin.		
4	SAP LED	SAP LED connection pin.		
5	Stereo LED	Stereo LED connection pin.		
6	Pilot Signal Detection	Stereo pilot signal detection pin.	$\frac{Vcc}{2}$	
7	Stereo PLL Filter	Stereo PLL low-pass filter connection pin.	2.8	
8	Vcc	Vcc pin	Vcc	

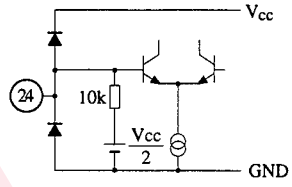
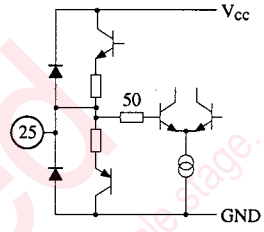
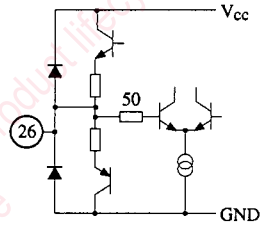
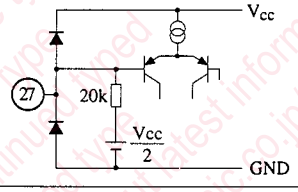
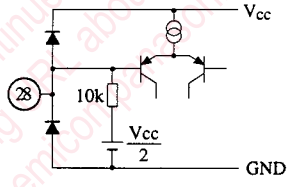
■ Pin Descriptions (Continue)

Pin No.	Pin Name	Pin Description	Pin Voltage	Equivalent Circuit
9	Pilot Signal Detection Hysteresis Adjustment	Pilot signal detection hysteresis setting pin.	$\frac{Vcc}{2}$	
10	Quasi Sinewave Filter	Low-pass filter connection pin of quasi sinewave circuit.	$\frac{Vcc}{2}$	
11	Stereo Filter Offset Absorption	Offset absorption pin of stereo filter output.	$\frac{Vcc}{2}$	
12	Composite Input	Composite signal input pin.	$\frac{Vcc}{2}$	
13	dbx Timing Current	Timing current setting pin of dbx rms value detection.	1.3V	
14	Reference	Reference power supply stabilization pin.	$\frac{Vcc}{2}$	
15	SAP / (L - R) Demodulation Output	SAP / (L - R) demodulation signal output pin.	$\frac{Vcc}{2}$ - 0.7	

■ Pin Descriptions (Continue)

Pin No.	Pin Name	Pin Description	Pin Voltage	Equivalent Circuit
16	dbx Input	(L - R) / SAP signal dbx NR input pin.	$\frac{Vcc}{2}$	
17	(L + R) Demodulation Output Offset Absorption	Offset absorption pin of (L + R) demodulation signal.	$\frac{Vcc}{2}$	
18	Spectral Level Adjustment	Recovery time setting pin of variable emphasis rms value detection.	$\frac{Vcc}{2}$	
19	Spectral Timing	Composite signal input pin.	0.2V	
20	Spectral Level Sensor Input	Input pin of variable emphasis rms value detection circuit.	$\frac{Vcc}{2}$	
21	GND	GND	0	
22	Wideband Level Sensor Input	Input pin of wideband expander rms value detection circuit.	$\frac{Vcc}{2}$	
23	Wideband Timing	Recovery time setting pin of wideband expandar rms value detection.	0.2V	

■ Pin Descriptions (Continue)

Pin No.	Pin Name	Pin Description	Pin Voltage	Equivalent Circuit
24	dbx Offset Absorption	Offset absorption pin of dbx NR output.	$\frac{Vcc}{2}$	
25	R Output	R Line Out Output pin.	$\frac{Vcc}{2}$	
26	L Output	L Line Out Output pin.	$\frac{Vcc}{2}$	
27	SAP Carrier Detection	Carrier level detection pin of SAP signal.	$\frac{Vcc}{2}$	
28	SAP Noise Level Setting	Noise detection pin of protection circuit against SAP operation error. (SAP demodulation is muted at noise detection.)	$\frac{Vcc}{2}$	

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