Features

- **8-bit Resolution**
- **1 Gsps (Min.) Sampling Rate**
- **ADC Gain Adjust**
- **2 GHz Full Power Input Bandwidth**
- **Fs = 1 Gsps, Fin = 20 MHz:**
  - **SINAD = 45 dB (7.4 Effective Bits) SFDR = 58 dBc**
- **Fs = 1 Gsps, Fin = 500 MHz:**
  - **SINAD = 44 dB (7.2 Effective Bits) SFDR = 56 dBc**
- **Fs = 1 Gsps, Fin = 1000 MHz (-3 dB Fs):**
  - **SINAD = 42 dB (7.0 Effective Bits) SFDR = 52 dBc**
- **2 Tone IMD: -53 dBc (489 MHz and 490 MHz) at 1 Gsps**
- **DNL = 0.3 LSB INL = 0.7 LSB**
- **Low Bit Error Rate (10^{-13}) at 1 Gsps**
- **Very Low Input Capacitance: 0.4 pF (Die Form)**
- **500 mVpp Differential or Single-ended Analog Inputs**
- **Differential or Single-ended 50 Ω ECL Compatible Clock Inputs**
- **ECL or LVDS/HSTL Output Compatibility**
- **Data Ready Output with Asynchronous Reset**
- **Gray or Binary Selectable Output Data; NRZ Output Mode**
- **Power Consumption: 3.4 W at T_J = 90° C**
- **Dual Power Supply: ±5 V**
- **Radiation Tolerance Oriented Design (150 Krad (Si) Measured)**

Description

The JTS8388B is a monolithic 8-bit analog-to-digital converter, designed for digitizing wide bandwidth analog signals at very high sampling rates of up to 1 Gsps.

The JTS8388B uses an innovative architecture, including an on-chip Sample and Hold (S/H), and is manufactured with an advanced high-speed bipolar process.

The on-chip S/H features a 2 GHz full power input bandwidth, providing excellent dynamic performance in undersampling applications (High IF digitizing).

Applications

- Digital Sampling Oscilloscopes
- Satellite Receiver
- Electronic Countermeasures/Electronic Warfare
- Direct RF Down-conversion

Screening

- Standard Die Flow
- Mil-PRF-38535, QML Level Q for Package Version
- Space Screening According to ESA/SCC 9000

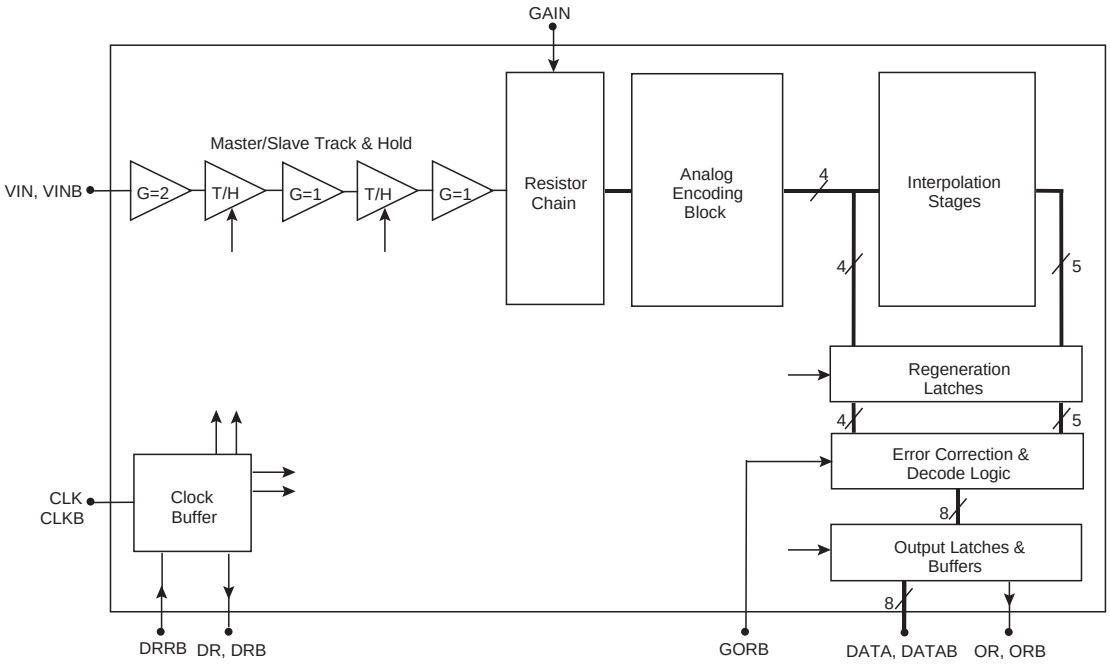
1 Gsps 8-bit A/D Converter

JTS8388B

2104A–BDC–09/03

Simplified Block Diagram

Figure 1. Simplified Block Diagram



Functional Description

The JTS8388B is an 8-bit 1 Gsps ADC based on an advanced high-speed bipolar technology featuring a cutoff frequency of 25 GHz.

The JTS8388B includes a front-end master/slave Track and Hold stage (Sample and Hold), followed by an analog encoding stage and interpolation circuitry.

Successive banks of latches regenerate the analog residues into logical data before entering an error correction circuitry and a resynchronisation stage followed by 75 Ω differential output buffers.

The JTS8388B works in a fully differential mode from analog inputs up to digital outputs.

The JTS8388B features a full power input bandwidth of 2 GHz.

The control pad GORB is provided to select either the gray or binary data output format.

The gain control pad is provided in order to adjust the ADC gain.

The JTS8388B uses only vertical isolated NPN transistors together with oxide-isolated polysilicon resistors, providing enhanced radiation tolerance (more than 100 kRad total dose expected radiation).

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6	V
Digital negative supply voltage	DV_{EE}		GND to -5.7	V
Digital positive supply voltage	V_{PLUSD}		GND - 0.3 to 2.8	V
Negative supply voltage	V_{EE}		GND to -6	V
Maximum difference between negative supply voltages	DV_{EE} to V_{EE}		0.3	V
Analog input voltages	V_{IN} or V_{INB}		-1 to 1	V
Maximum difference between V_{IN} and V_{INB}	V_{IN} - V_{INB}		-2 to 2	V
Digital input voltage	V_D	GORB	-0.3 to V_{CC} 0.3	V
Digital output current	I_O	Conditions: -3V < V_{OUT} < 0.5 V	20	mA
Digital input voltage	V_D	DRRB	V_{EE} -0.3 to 0.9	V
Digital output voltage	V_O		V_{PLUSD} -3 to V_{PLUSD} -0.5	V
Clock input voltage	V_{CLK} or V_{CLKB}		-3 to 1.5	V
Maximum difference between V_{CLK} and V_{CLKB}	V_{CLK} - V_{CLKB}		-2 to 2	V
Maximum junction temperature	T_J		135	°C
Storage temperature	T_{stg}		-65 to 150	°C
Lead temperature (soldering 10 s)	T_{leads}		300	°C

Note: Absolute maximum ratings are limiting values, to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect device reliability. The use of a thermal heat sink is mandatory (MCM fixture).

Recommended Conditions of Use

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Positive supply voltage	V_{CC}		4.75	5	5.25	V
Positive digital supply voltage	V_{PLUSD}	ECL output compatibility		0		V
	V_{PLUSD}	LVDS output compatibility	1.4	2.4	2.6	V
Negative supply voltages	$V_{EE,}$ D_{VEE}		-5.25	-5.0	-4.75	V

Recommended Conditions of Use (Continued)

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Differential analog input voltage (full-scale)	V_{IN}, V_{INB} V_{IN} - V_{INB}	50 Ω differential or single-ended	±113 450	±125 500	±137 550	mV mVpp
Clock input power level	PCLK PCLKB	50 Ω single-ended clock input	3	4	10	dBm
Operating temperature range	T_J	Civil: “C” grade Industrial: “V” grade Military: “M” grade	0 to 90 -40 to 105 -55 to 125			°C

Electrical Operating Characteristics

V_{EE} = D_{VEE} = -5 V; V_{CC} = 5 V; V_{IN} - V_{INB} = 500 mVpp full-scale differential input
Digital outputs 75 or 50 Ω differentially terminated; T_J (typical) = 70°C. Full temperature range: -55°C < T_J < 125°C

Parameter	Symbol	Temp	Test Level	Min.	Typ.	Max.	Unit
Resolution					8		bits
Analog Inputs							
Full-scale input voltage range (differential mode) (0 V common mode voltage)	V_{IN} V_{INB}	 Full	 IV	-125 -125		125 125	mV mV
Full-scale input voltage range (single-ended input option)	V_{IN} V_{INB}	 Full	 IV	-250	0	250	mV mV
Analog input capacitance (die)	C_{IN}		IV		0.4		pF
Input bias current	I_{IN}		IV		10		µA
Input resistance	R_{IN}		IV		1		MΩ
Full power input bandwidth	FPBW		IV		1.8		GHz
Small signal input bandwidth (10% full-scale)	SSBW		IV		2		GHz
Clock Inputs							
Logic compatibility for clock inputs (1)				ECL or specified clock input power level in dBm			
ECL clock inputs voltages (V_{CLK} or V_{CLKB}) Logic 0 voltage Logic 1 voltage Logic 0 current Logic 1 current	 V_{IL} V_{IH} I_{IL} I_{IH}	 Full Full Full Full		 -1.1 	 5 5	 -1.5 	 V V µA µA
Clock input power level into 50 Ω termination				dBm into 50 Ω			
Clock input power level				3	4	10	dBm
Clock input capacitance (die)	C_{CLK}				0.4		pF

Electrical Operating Characteristics (Continued)

V_{EE} = D_{VEE} = -5 V; V_{CC} = 5 V; V_{IN} - V_{INB} = 500 mVpp full-scale differential input
Digital outputs 75 or 50 Ω differentially terminated; T_J (typical) = 70°C. Full temperature range: -55°C < T_J < 125°C

Parameter		Symbol	Temp	Test Level	Min.	Typ.	Max.	Unit
Digital Outputs								
Logic compatibility for digital outputs (depending on the value of V_{PLUSD}) (2)						ECL or LVDS		
Differential output voltage swings								
75 Ω open transmission lines (ECL Levels)					1.5	1.620		V
75 Ω differentially terminated					0.7	0.825		V
50 Ω differentially terminated			Full	IV	0.54	0.660		V
Output levels (assuming V_{PLUSD} = 0 V) 75 Ω open transmission lines (3)								
logic 0 voltage		V_{OL}				-1.62		V
logic 1 voltage		V_{OH}	25°C	IV	-0.88	-0.8	-1.54	V
Output levels (assuming V_{PLUSD} = 0 V) 75 Ω differentially terminated (3)								
Logic 0 voltage		V_{OL}				-1.41		V
Logic 1 voltage		V_{OH}	25°C	IV	-1.07	-1	-1.34	V
Output levels (assuming V_{PLUSD} = 0 V) 50 Ω differentially terminated (3)								
Logic 0 voltage		V_{OL}				-1.45		V
Logic 1 voltage		V_{OH}	25°C	II	-1.2	-1.15	-1.32	V
Power Requirements								
Positive supply voltage	analog	V_{CC}				5		V
	digital (ECL)	V_{PLUSD}			4.75	0	2.6	V
	digital (LVDS)			II, IV	1.4	2.4	5.25	V
Positive supply current	analog	ICC				385	445	mA
	digital	I_{PLUSD}		II, IV		115	145	mA
Negative supply voltage		V_{EE}	Full	IV	-5.25	-5	-4.75	V
Negative supply current	analog	AIEE				165	200	mA
	digital	DIEE		II, IV		135	180	mA
Nominal power dissipation						3.4	4.1	W
		PD	Full	II, IV		4.1	4.3	W
Power supply rejection ratio (4)		PSRR		IV		±0.5		mV/V

Electrical Operating Characteristics (Continued)

V_{EE} = D_{VEE} = -5 V; V_{CC} = 5 V; V_{IN} - V_{INB} = 500 mVpp full-scale differential input
Digital outputs 75 or 50 Ω differentially terminated; T_J (typical) = 70°C. Full temperature range: -55°C < T_J < 125°C

Parameter	Symbol	Temp	Test Level	Min.	Typ.	Max.	Unit
DC Accuracy							
Differential non-linearity (4)(5)	DNL	Full	I, IV		0.35 0.5	0.6 0.7	LSB LSB
Integral non-linearity (4)(5)	INL	Full	I, IV		0.7 0.9	1 1.2	LSB LSB
No missing codes (5)		Full	Guaranteed over specified temperature range				
Gain error		Full	I IV	-10 -11	-2 -2	10 11	% Fs % Fs
Gain error drift		Full	IV	100	125	150	ppm/°C
Input offset voltage		Full	I IV	-26 -30	-5 -5	26 30	mV mV
Transient Performance							
Bit error rate (4)(6) Fs = 1 Gsps Fin = 143 MHz	BER	Full	IV		10^{-13}		Error/ sample
ADC settling time (4) V_{In} - V_{inB} = 400 mVpp	TS		IV		0.5		ns
Overvoltage recovery time (4)	ORT		IV		0.5		ns

Electrical Operating Characteristics (Continued)

V_{EE} = D_{VEE} = -5 V; V_{CC} = 5 V; V_{IN} - V_{INB} = 500 mVpp full-scale differential input
Digital outputs 75 or 50 Ω differentially terminated; T_J (typical) = 70°C. Full temperature range: -55°C < T_J < 125°C

Parameter	Symbol	Temp	Test Level	Min.	Typ.	Max.	Unit
AC Performance							
Single-ended or differential input mode, 50% clock duty cycle (CLK, CLKB), binary output data format, T_J = 70°C, unless otherwise specified.							
Signal to noise and distortion ratio (4)							
Fs = 1 Gsps Fin = 20 MHz				43	45		dB
Fs = 1 Gsps Fin = 500 MHz				42	44		dB
Fs = 1 Gsps Fin = 1000 MHz (-1 dBFs)	SINAD	Full	IV	40	42		dB
Effective number of bits (4)							
Fs = 1 Gsps Fin = 20 MHz				7.0	7.2		Bits
Fs = 1 Gsps Fin = 500 MHz				6.6	6.8		Bits
Fs = 1 Gsps Fin = 1000 MHz (-1 dBFs)	ENOB	Full	IV	6.2	6.4		Bits
Signal to noise ratio (4)							
Fs = 1 Gsps Fin = 20 MHz				42	45		dB
Fs = 1 Gsps Fin = 500 MHz				41	44		dB
Fs = 1 Gsps Fin = 1000 MHz (-1 dBFs)	SNR	Full	IV	41	44		dB
Total harmonic distortion (4)							
Fs = 1 Gsps Fin = 20 MHz					-54	-50	dBc
Fs = 1 Gsps Fin = 500 MHz					-50	-46	dBc
Fs = 1 Gsps Fin = 1000 MHz (-1 dBFs)	THD	Full	IV		-46	-42	dBc
Spurious free dynamic range (4)							
Fs = 1 Gsps Fin = 20 MHz					-57	-52	dBc
Fs = 1 Gsps Fin = 500 MHz					-52	-47	dBc
Fs = 1 Gsps Fin = 1000 MHz (-1 dBFs)					-47	-42	dBc
Fs = 1 Gsps Fin = 1000 MHz (-3 dBFs)	SFDR	Full	IV		-50	-45	dBc
Two tone intermodulation distortion (4)							
F_{IN1} = 489 MHz at Fs = 1 Gsps							
F_{IN2} = 490 MHz at Fs = 1 Gsps	IMD	Full	IV		-53	-47	dBc

Electrical Operating Characteristics (Continued)

V_{EE} = D_{VEE} = -5 V; V_{CC} = 5 V; V_{IN} - V_{INB} = 500 mVpp full-scale differential input
Digital outputs 75 or 50 Ω differentially terminated; T_J (typical) = 70°C. Full temperature range: -55°C < T_J < 125°C

Parameter	Symbol	Temp	Test Level	Min.	Typ.	Max.	Unit
Switching Performance and Characteristics - See Figures 2 and 3 on page 9							
Maximum clock frequency (binary output coding)	Fs			1		1.4	Gsps
Maximum clock frequency (Gray output coding)	Fs			1		1.9	Gsps
Minimum clock frequency	Fs		IV		10		Msps
Minimum clock pulse width (high)	TC1		IV	0.285	0.500	50	ns
Minimum clock pulse width (low)	TC2		IV	0.350	0.500	50	ns
Aperture delay (4)	TA		IV	100	250	400	ps
Aperture uncertainty (4)(7)	Jitter		IV		0.4	0.6	ps (rms)
Data output delay (3)(4)(9)(10)	TOD	Full	IV	1150	1360	1660	ps
Output rise/fall time for data (20% - 80%) (9)	TR/TF	Full	IV	250	350	550	ps
Output rise/fall time for data ready (20% - 80%) (9)	TR/TF	Full	IV	250	350	550	ps
Data ready output delay (4)(8)(9)(10)	TDR	Full	IV	1110	1320	1620	ps
Data ready reset relay	TRDR				720	1000	ps
(11)	TOD-TDR			40	40	40	ps
See timing diagram at 1 Gsps	TD1	Full	IV	460	460	460	ps
Data pipeline delay	TPD		IV		4		Clock cycles

Notes:
1. The clock inputs may be indifferently entered in differential or single-ended mode, using ECL levels or 4 dBm typical power level into the 50 Ω termination resistor of the in-phase clock input. (4 dBm into 50 Ω clock input correspond to 10 dBm power level for the clock generator).
2. Differential output buffers are internally loaded by 75 W resistors. Buffer bias current = 11 mA
3. Specified loading conditions for digital outputs:
   • 50 or 75 W controlled impedance traces properly 50/75 W terminated, or unterminated 75 W controlled impedance traces.
   • Controlled impedance traces far-end loaded by 1 standard ECLinPS register from Motorola® (e.g.: 10E452) (typical input parasitic capacitance of 1.5 pF including package and ESD protections).
4. See “Definitions of Terms” on page 28.
5. Histogram testing based on sampling of a 10 MHz sinewave at 50 Msps
6. Output error amplitude < ±4 LSB around worst code
7. Maximum jitter value obtained for single-ended clock input
8. At 1 Gsps, 50/50 clock duty cycle, TC2 = 500 ps (TC1). TDR - TOD = -100 ps (typ) does not depend on the sampling rate.
9. Termination load parasitic capacitance derating values:
   • 50 or 75 W controlled impedance traces properly 50 /75 W terminated: 60 ps / pF or 75 ps per additional ECLinPS load.
   • Unterminated (source terminated) 75W controlled impedance lines: 100 ps / pF or 150 ps per additional ECLinPS termination load.
10. Apply proper 50/75 W impedance traces propagation time derating values: 6 ps / mm (155 ps/inch) for TSEV8388B Evaluation Board.
11. Values for TOD and TDR track each other over temperature (1 percent variation for TOD - TDR per 100 degrees Celsius temperature variation). Therefore, TOD - TDR variation over temperature is negligible. Moreover, the internal (on-chip) and package skews between each Data TOD and TDR effect can be considered negligible. Consequently, minimum values for TOD and TDR are never more than 100 ps apart. The same is true for the TOD and TDR maximum values. See “Applying the JTS8388B” on page 30.

Figure 2. JTS8388B Timing Diagram (1 Gsps Clock Rate) Data Ready Reset, Clock Held at LOW Level

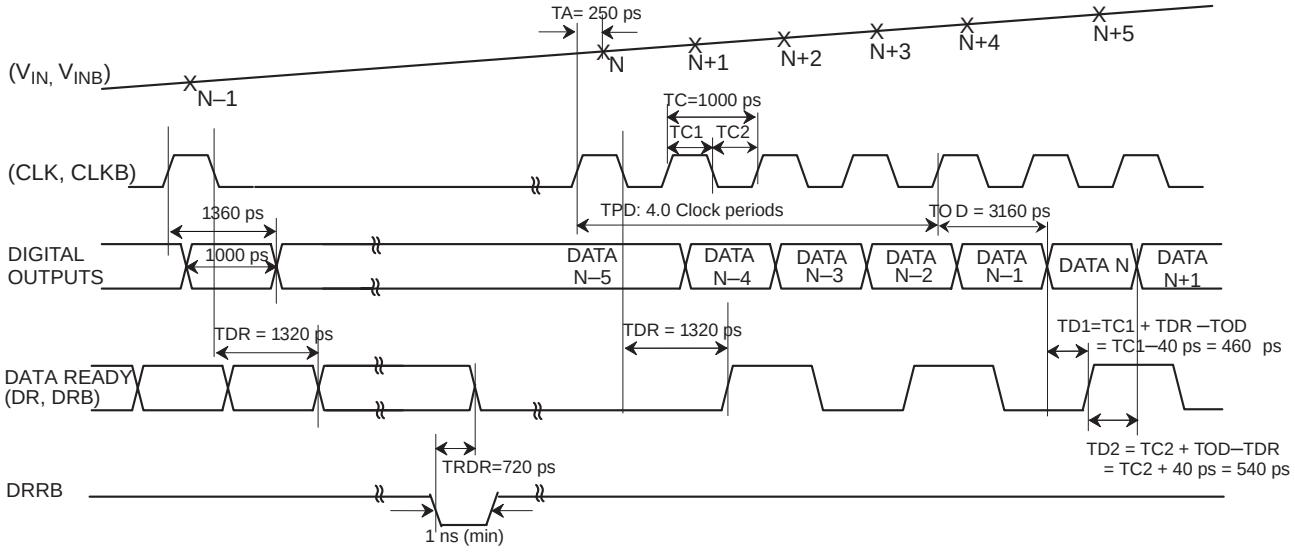


Figure 3. JTS8388B Timing Diagram (1 Gsps Clock Rate) Data Ready Reset, Clock held at HIGH Level

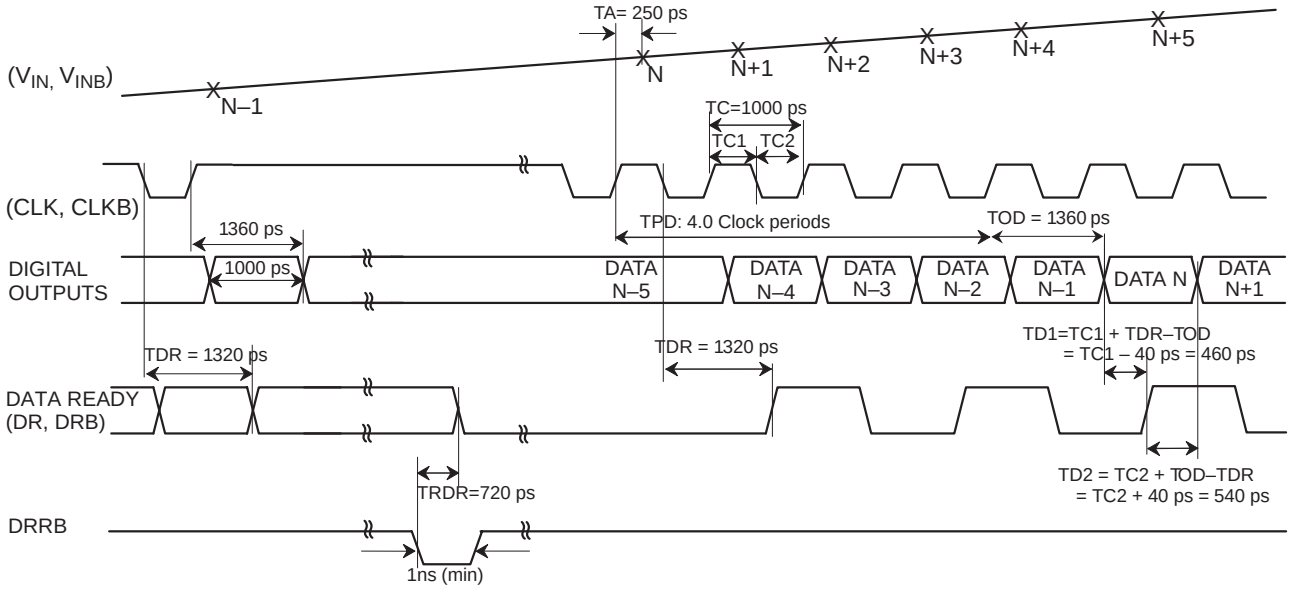


Table 1. Explanation of Test Levels

Level	Description
D	100% wafer tested at 25° C(2)
I	100% production tested at 25° C(2) (for packaged device)
II	100% production tested at 25° C(2), and sample tested at specified temperatures
III	Sample tested only at specified temperatures
IV	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature)
V	Parameter is a typical value only
VI	100% production tested over specified temperature range

Notes: 1. Only min. and max. values are guaranteed (typical values issue from characterization results)
2. Unless otherwise specified, all tests are pulsed tests: therefore $T_J = T_C = T_A$

Table 2. Wafer Screening

Parameter	Temperature	JTS8388B chip		Unit
		Min.	Max.	
DC accuracy at 50 Mpsps/10 MHz	25° C(1)			
DNL			0.6	LSB
INL			1	LSB
No missing codes		Guaranteed		
AC performance TBD	25° C(1)			
SNR		45		dB
ENOB		7.1		bit

Note: 1. Unless otherwise specified, all tests are pulsed tests: therefore $T_J = T_C = T_A$

Functions Description

Name	Function
V_{CC}	Positive power supply
V_{EE}	Analog negative power supply
V_{PLUSD}	Digital positive power supply
GND	Ground
VIN, VINB	Differential analog inputs
CLK, CLKB	Differential clock inputs
<D0:D7> <D0B:D7B>	Differential output data port
DR; DRB	Differential data ready outputs
OR; ORB	Out-of-range outputs
GAIN	ADC gain adjust
GORB	Gray or binary digital output select
DIOD/DRRB	Die junction temp. measurement/ asynchronous data ready reset

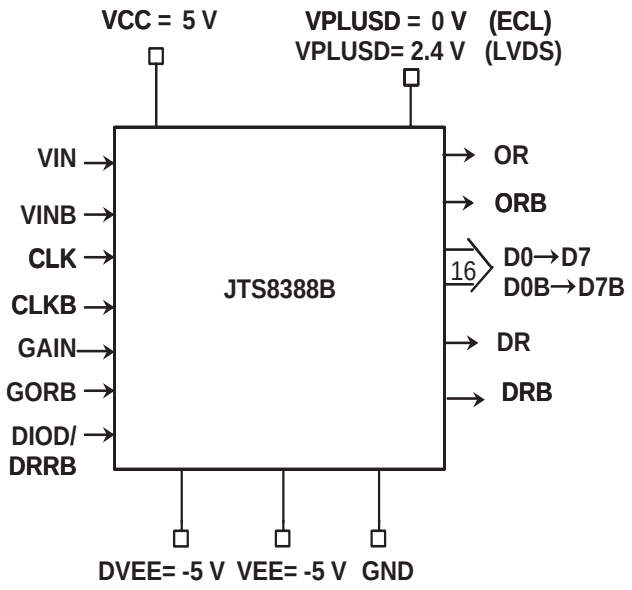


Table 3. Digital Coding

NRZ (Non Return to Zero) mode, ideal coding: does not include gain, offset, and linearity voltage errors.

Differential Analog Input	Voltage Level	Digital Output		Out of Range
		Binary GORB = V_{CC} or floating	Gray GORB = GND	
> 251 mV	> Positive full-scale + 1/2 LSB	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	1
251 mV	Positive full-scale + 1/2 LSB	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	0
249 mV	Positive full-scale - 1/2 LSB	1 1 1 1 1 1 1 0	1 0 0 0 0 0 0 1	0
126 mV	Positive 1/2 scale + 1/2 LSB	1 1 0 0 0 0 0 0	1 0 1 0 0 0 0 0	0
124 mV	Positive1/2 scale - 1/2 LSB	1 0 1 1 1 1 1 1	1 1 1 0 0 0 0 0	0
1 mV	Bipolar zero + 1/2 LSB	1 0 0 0 0 0 0 0	1 1 0 0 0 0 0 0	0
-1 mV	Bipolar zero - 1/2 LSB	0 1 1 1 1 1 1 1	0 1 0 0 0 0 0 0	0
-124 mV	Negative 1/2 scale + 1/2 LSB	0 1 0 0 0 0 0 0	0 1 1 0 0 0 0 0	0
-126 mV	Negative 1/2 scale - 1/2 LSB	0 0 1 1 1 1 1 1	0 0 1 0 0 0 0 0	0
-249 mV	Negative full-scale + 1/2 LSB	0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 1	0
-251 mV	Negative full-scale - 1/2 LSB	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	0
< -251 mV	< Negative full-scale - 1/2 LSB	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1

Chip Description

Table 4. JTS8388B Chip Functions Description

Symbol	Pad Number	Function
GND	20, 24, 26, 28, 33, 35, 37	Analog ground Pads n°20, 24, 26, 28, 37 are double Pads n° 26, 33, 35 are single 14 bonding wires are available for analog ground access
V_{PLUSD}	1, 11	Digital positive supply (0 V for ECL compatibility, 2.4 V for LVDS compatibility). 2 double pads
V_{CC}	19, 21, 23, 30, 39, 40	5 V analog supply
V_{EE}	22, 29, 31	-5 V analog supply
D_{VEE}	6	-5 V digital supply
VIN	34	In-phase (+) analog input signal of the differential Sample & Hold preamplifier
VINB	36	Inverted phase (-) analog input signal
CLK	25	In-phase (+) ECL clock input
CLKB	27	Inverted phase (-) ECL clock input
D0, D1, D2, D3, D4, D5, D6, D7	16, 14, 12, 9, 4, 2, 45, 43	In-phase (+) digital outputs D0 is the LSB. D7 is the MSB
D0B, D1B, D2B, D3B, D4B, D5B, D6B, D7B	17, 15, 13, 10, 5, 3, 46, 44	Inverted phase (-) digital outputs. D0B is the inverted LSB. D7B is the inverted MSB
OR	41	In-phase (+) out-of-range output Out-of-range goes high on the leading edge of code 0 or code 256
ORB	42	Inverted phase (-) out-of-range output
DR	7	In-phase (+) output of Data Ready signal
DRB	8	Inverted phase (-) output of Data Ready signal
GORB	18	Gray or binary select output format control pad • Binary output format if GORB is floating or tied at V_{CC} • Gray output format if GORB is connected to ground (0 V)
GAIN	38	ADC gain adjust pad
DIOD/DRRB	32	DIOD: die junction temperature measurement pad Can be left floating or grounded if not used DRRB: asynchronous data ready reset function

Table 5. JTS8388B Chip Pad List, Coordinates and Corresponding Functions

Pad Number	PosX	PosY	Chip Pad Function			
1	880	1365	V_{PLUSD}	Positive digital supply	double pad	(3)
2	670	1365	D5	In-phase (+) digital output, bit 5 (D7 is the MSB: Bit 7, D0 is the LSB: Bit 0)		
3	510	1365	D5B	Inverted phase (-) digital output, bit 5		
4	350	1365	D4	In-phase (+) digital output, bit 4		
5	190	1365	D4B	Inverted phase (-) digital output, bit 4		
6	-20	1365	D_{VEE}	-5 V digital supply	double pad	
7	-230	1365	DR	In-phase (+) data ready		
8	-390	1365	DRB	Inverted Phase (-) data ready		
9	-550	1365	D3	In-phase (+) digital output, bit 3		
10	-710	1365	D3B	Inverted phase (-) digital output, bit 3		
11	-920	1365	V_{PLUSD}	Positive digital supply	double pad	(3)
12	-1085	1115	D2	In-phase (+) digital output, bit 2		
13	-1085	955	D2B	Inverted phase (-) digital output, bit 2		
14	-1085	795	D1	In-phase (+) digital output, bit 1		
15	-1085	635	D1B	Inverted phase (-) digital output, bit 1		
16	-1085	475	D0	In-phase (+) digital output, bit 0, least significant bit		
17	-1085	315	D0B	Inverted phase (-) digital output, bit 0, least significant bit		
18	-1085	155	GORB	Gray or binary data output format select		(2)
19	-1085	-55	V_{CC}	5 V supply	double pad	
20	-1085	-325	GND	Analog ground	double pad	
21	-1085	-595	V_{CC}	5 V supply	double pad	
22	-1085	-865	V_{EE}	-5 V analog supply	double pad	
23	-1085	-1135	V_{CC}	5 V supply	double pad	
24	-905	-1365	GND	Analog ground	double pad	
25	-655	-1365	CLK	In-phase (+) clock input	double pad	
26	-455	-1365	GND	Analog ground		
27	-255	-1365	CLKB	Inverted phase (-) clock input	double pad	
28	-5	-1365	GND	Analog ground	double pad	
29	245	-1365	V_{EE}	-5 V analog supply	double pad	
30	495	-1365	V_{CC}	5 V supply	double pad	
31	745	-1365	V_{EE}	-5 V analog supply	double pad	
32	945	-1365	DIOD/DRRB	Diode input for T_J monitoring / input for asynchronous data ready reset		
33	1085	-1195	GND	Analog ground		
34	1085	-995	V_{IN}	In-phase (+) analog input	double pad	
35	1085	-795	GND	Analog ground		

Table 5. JTS8388B Chip Pad List, Coordinates and Corresponding Functions (Continued)

Pad Number	PosX	PosY	Chip Pad Function		
36	1085	-595	$V_{IN}B$	Inverted phase (-) analog input	double pad
37	1085	-345	GND	Analog ground	double pad
38	1085	-145	GAIN	ADC gain adjust input	
39	1085	55	V_{CC}	5 V supply	double pad
40	1085	265	V_{CC}	5 V supply	
41	1085	425	OR	In-phase (+) out-of-range digital output	
42	1085	585	ORB	Inverted phase (-) out-of-range digital output	
43	1085	745	D7	In-phase (+) digital output, bit 7, most significant bit	
44	1085	905	D7B	Inverted phase (-) digital output, bit 7	
45	1085	1065	D6	In-phase (+) digital output, bit 6	
46	1085	1225	D6B	Inverted phase (-) digital output, bit 6	

Note: 1. Coordinates are relative to pad centers. The coordinates origin (0, 0) is at the center of the die.
All dimensions are given in microns. Pad 1 is one pointed at by the arrow in Figure 4 on page 15
Distance between pad (glass window) and inner edge of seaf-ring: 40 µm.
Die size (inner edge of seal-ring: (-1175, -1455) (1175, 1455).
Die size (including scribe line): (-1230, -1510) (1230, 1510) (2.46 x 3.02 mm^2).
Actual die size (after separation): (-1220, -1500) (1220, 1500) (2.44 mm x 3.00 mm).

2. GORB tied to V_{CC} or floating: binary output data format. GORB tied to GND: gray output data format.
3. The common mode level of the output buffers is 1.2 V below the positive digital supply.
For ECL compatibility the positive digital supply must be set at 0 V (ground).
For LVDS compatibility (output common mode at 1.2 V) the positive digital supply must be set at 2.4 V.
If the subsequent LVDS circuitry can withstand a lower level for input common mode, it is recommended to lower the positive digital supply level in the same proportion in order to spare power dissipation.

Figure 4. JTS8388B Chip Pads Designation

Die size: 2.44 x 3.00 mm (after separation); die area: 7.32 mm^2

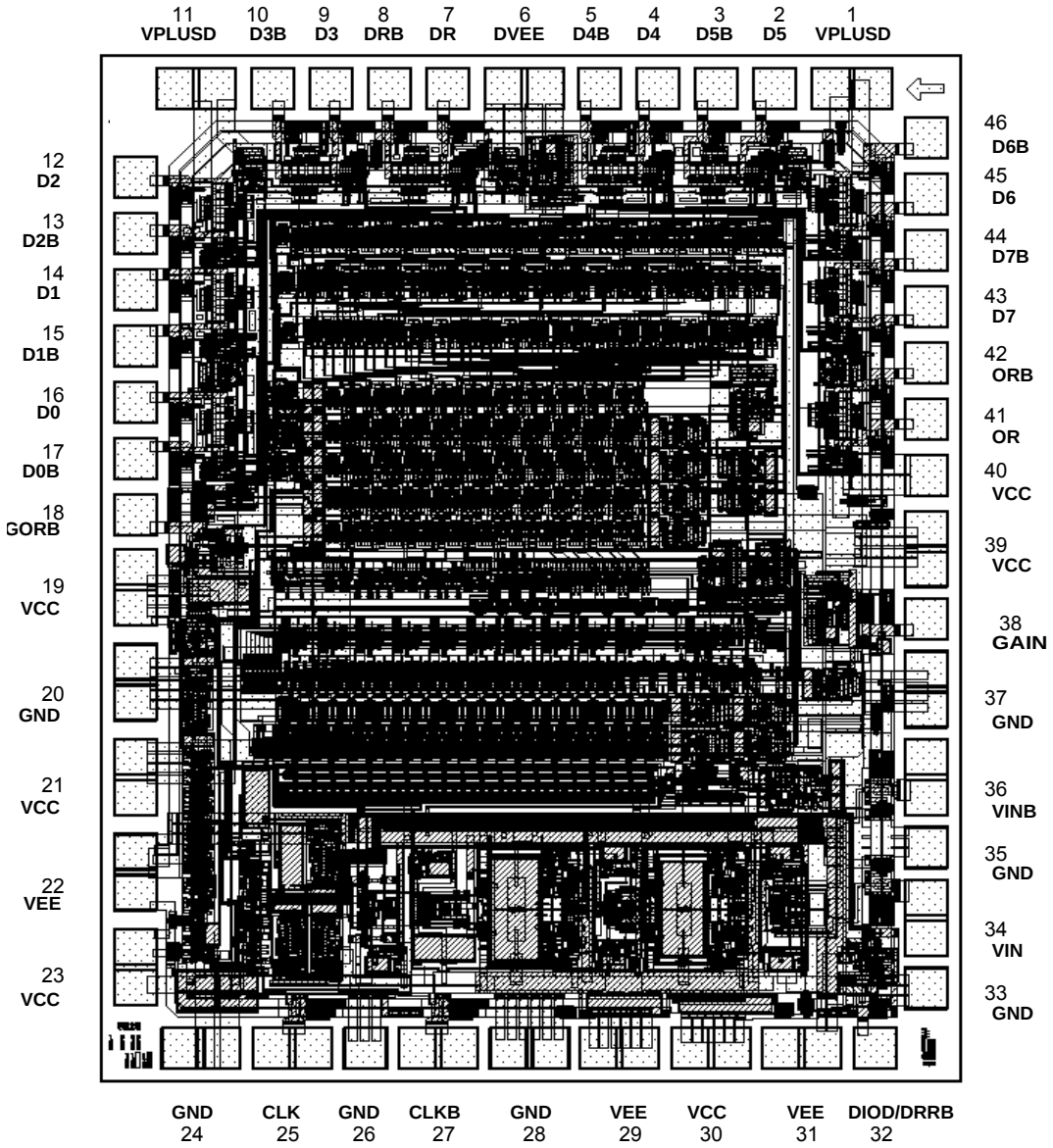


Table 6. Die Mechanical Information

Mask Reference	Description	VH25B rev B
Die size	Between scribe line axis After separation	2.46 mm x 3.02 mm 2.44 mm x 3.00 mm
Pad size	(single pad) (double pad)	100 µm x 100 µm 200 µm x 100 µm
Die thickness		380 µm ± 20 µm
Back side metallization		None
Metallization	Number of layers Material Diffusion barrier Thickness	3 Ti/TiN Al-Si-Cu TiN (on top) Ti/TiN Metal 1: 600 nm; Metal 2 & Metal 3: 800 nm
Pad metallization(1)(2)		Ti/TiN Al-Si-Cu TiN (Metal 2) Ti/TiN Al-Si-Cu (Metal 3)
Passivation		Oxide/Nitride (SiO_2/SiN_2): 300 nm / 550 nm
Back side potential		-5 V
Die transistor count		4450
Die attach		Epoxy Ag filled high conductivity glue
Bond wire		Al or Au 30 µm diameter
Qualification package		CQFP68 (with restriction on electrical performance)

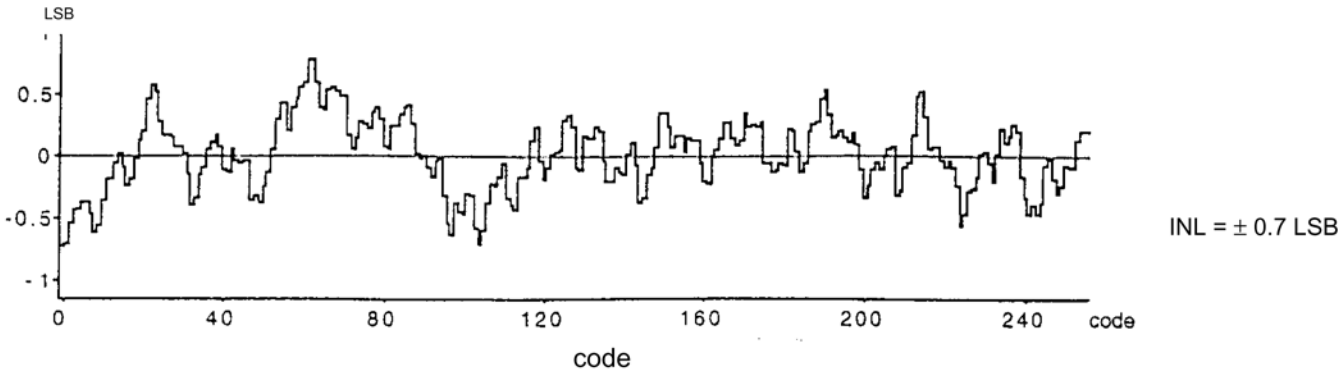
Notes: 1. The top TiN layer is etched in one step together with the passivation layer.
2. The pad is a sandwich of Metal 2 and Metal 3 over field oxyde.

Typical Characterization Results

Static Linearity

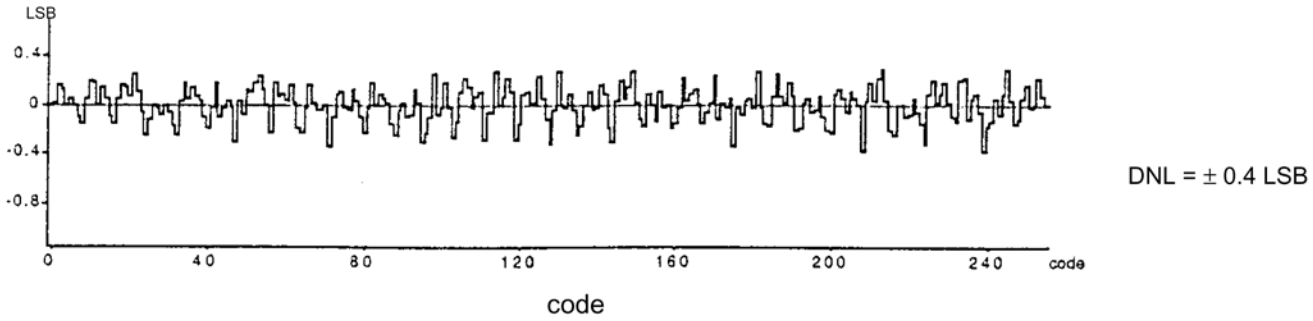
Fs = 50 Msps; Fin = 10 MHz

Figure 5. Integral Non-linearity



Clock frequency = 50 Msps
Signal frequency = 10 MHz
Positive peak: 0.78 LSB
Negative peak: -0.73 LSB

Figure 6. Differential Non-linearity



Clock frequency = 50 Msps
Signal frequency = 10 MHz
Positive peak: 0.3 LSB
Negative peak: -0.39 LSB

Effective Number of Bits Versus Power Supplies Variation

Figure 7. Effective Number of Bits (ENOB) = f (V_{EEA}); Fs = 500 Msps; Fin = 100 MHz

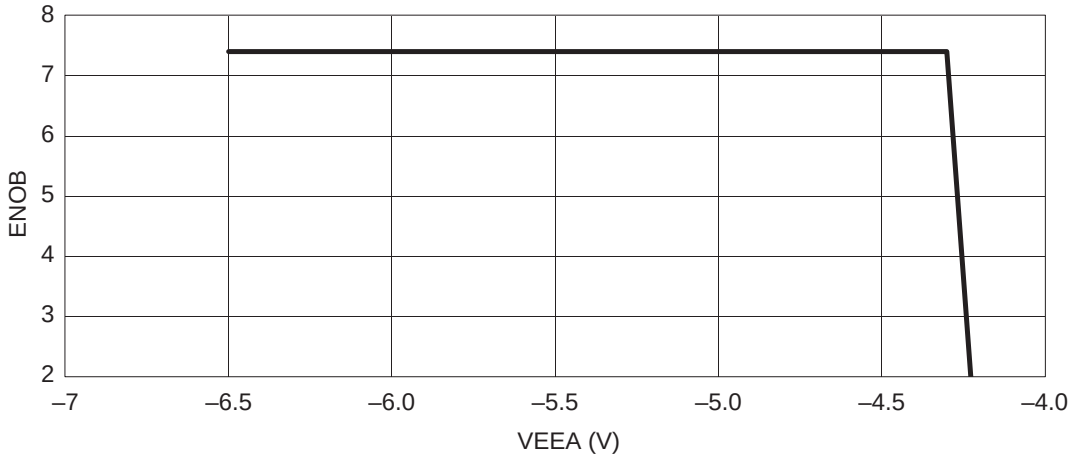
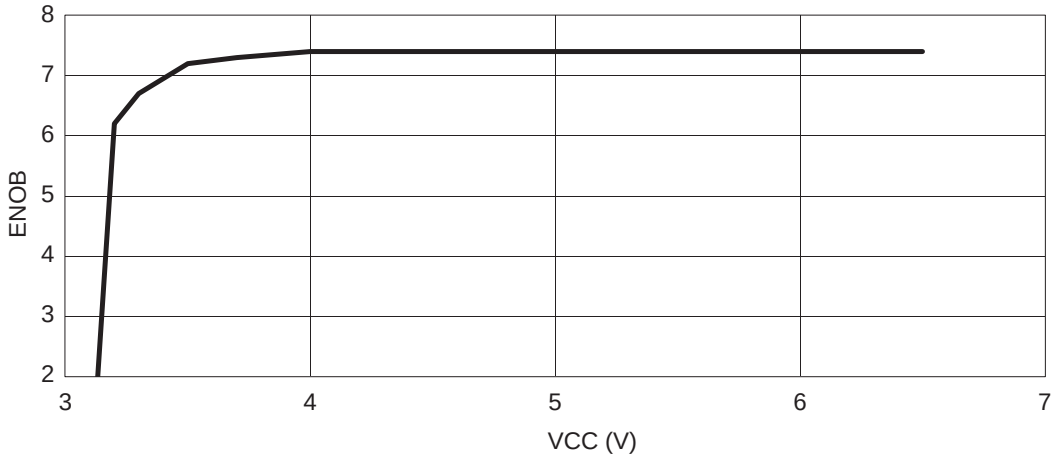
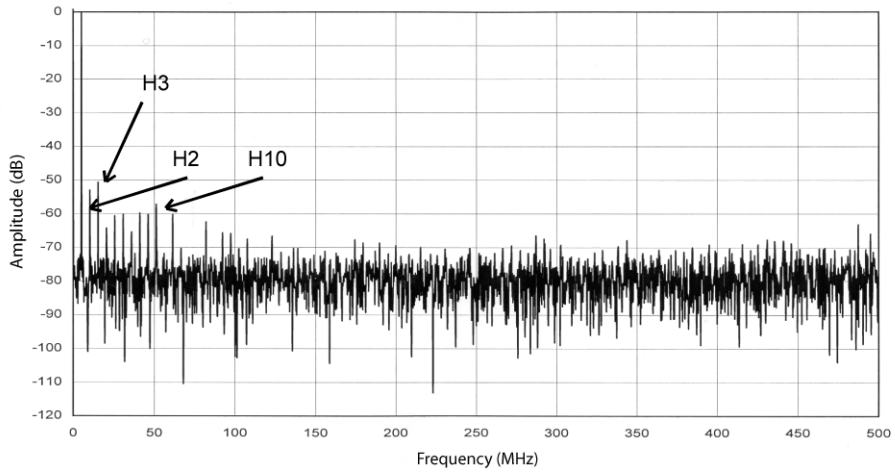


Figure 8. Effective Number of Bits = (ENOB) f (V_{CC}); Fs = 500 Msps; Fin = 100 MHz



Typical FFT Results

Figure 9. Fs = 1 Gsps; Fin = 20 MHz



Single Ended or differential

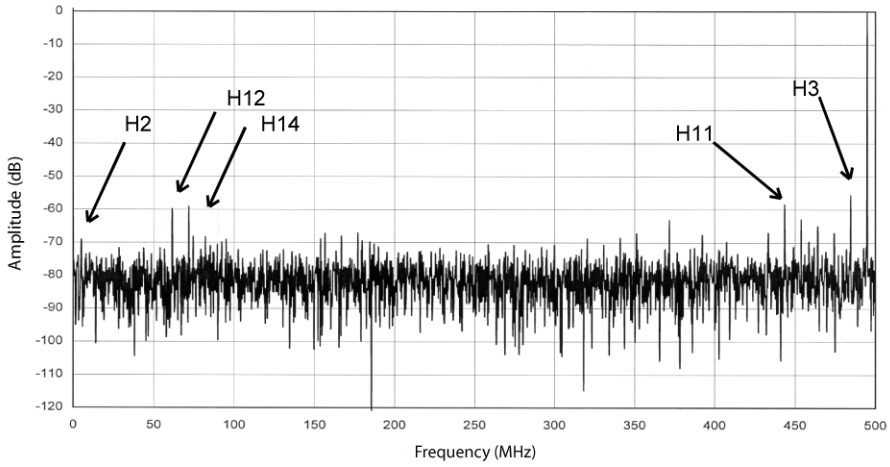
Fs =1 GSPS
Fin=995 MHz

Eff. Bits =6.6
SINAD =40.8 dB
SNR = 44 dB
THD = -48 dBc
SFDR= -50 dBc

Binary output coding

clock duty cycle = 50 %

Figure 10. Fs = 1 Gsps; Fin = 495 MHz



Single Ended or differential

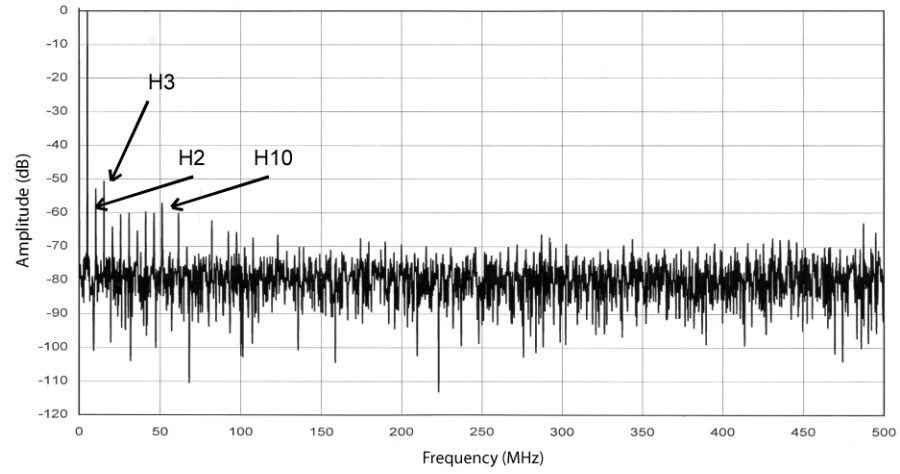
Fs =1 GSPS
Fin=495MHz

Eff. Bits =6.8
SINAD =43 dB
SNR = 44.1 dB
THD = -50 dBc
SFDR= -52 dBc

Binary output coding

clock duty cycle = 50 %

Figure 11. Fs = 1 Gsps; Fin = 995 MHz; -3 dB Full-scale Input



Single Ended or differential

Fs =1 GSPS
Fin=995 MHz

Eff. Bits =6.6
SINAD =40.8 dB
SNR = 44 dB
THD = -48 dBc
SFDR= -50 dBc

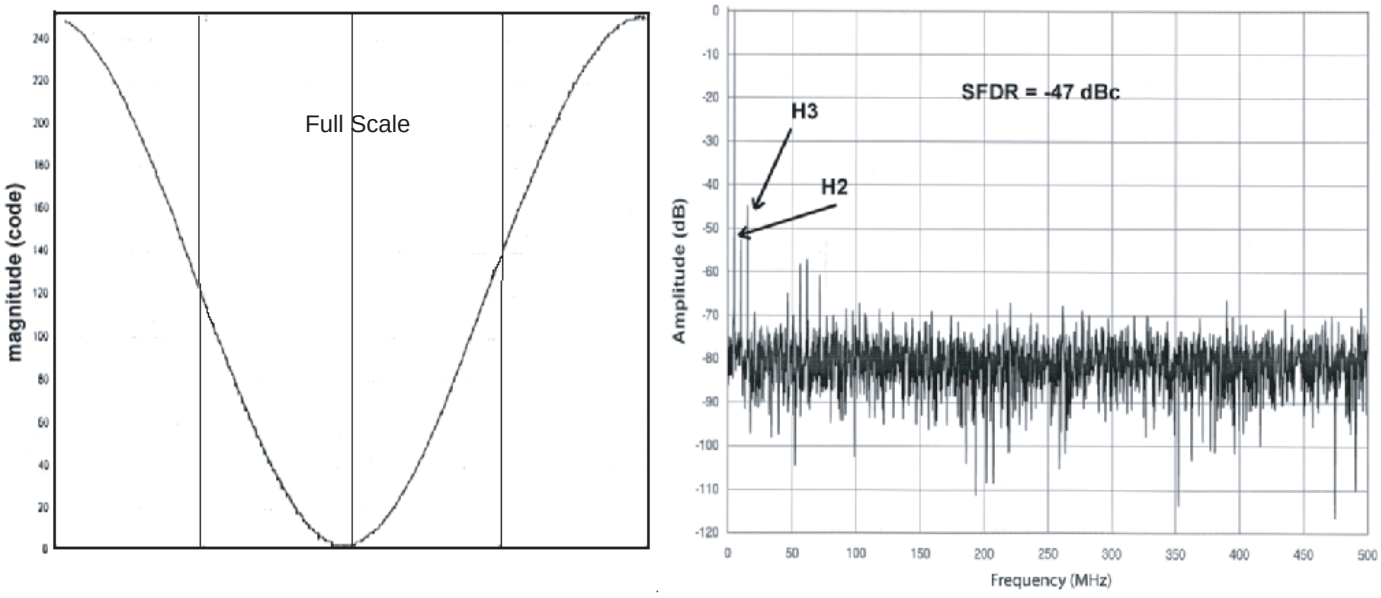
Binary output coding

clock duty cycle = 50 %

Spurious Free Dynamic Range Versus Input Amplitude

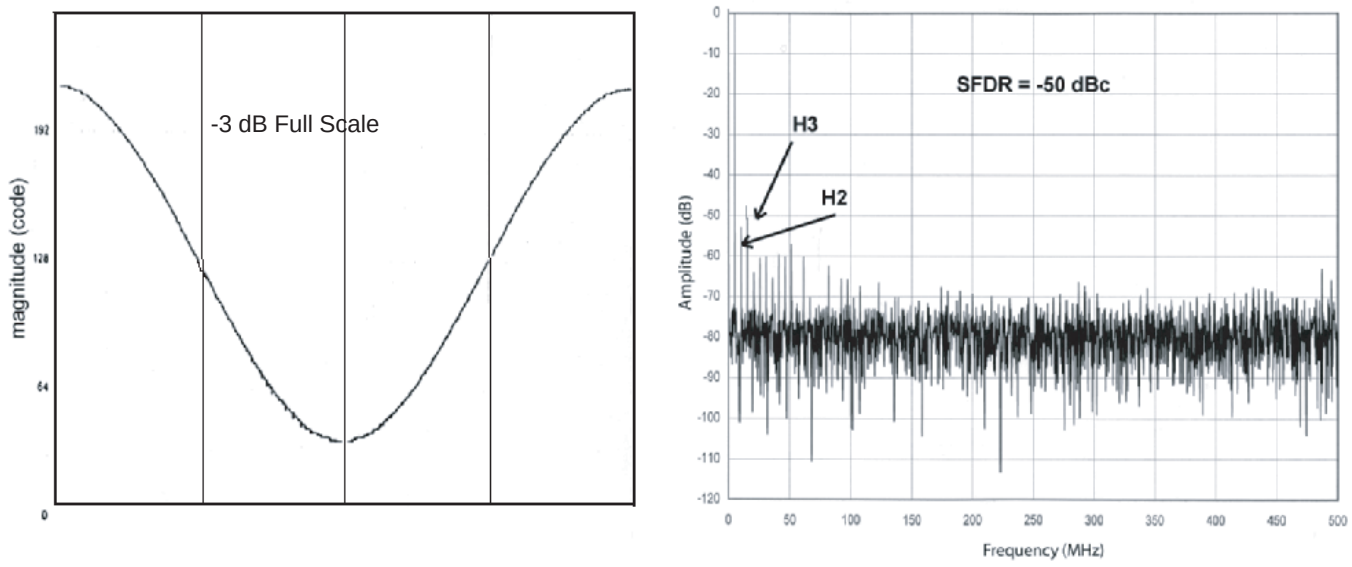
Sampling frequency Fs = 1 Gsps; Input frequency Fin = 995 MHz; Gray or binary output coding

Figure 12. Reconstructed Signal and Signal Spectrum at Fs = 1 Gsps, Fin = 995 MHz, Full-scale



ENOB = 6.7 SINAD = 41.5 dB SNR = 44.8 dB THD = -44.4 dBc SFDR = -45 dBc

Figure 13. Reconstructed Signal and Signal Spectrum at Fs = 1 Gsps, Fin = 995 MHz, -3 dB Full-scale



ENOB = 6.7 SINAD = 41.5 dB SNR = 44.8 dB THD = -44.4 dBc SFDR = -45 dBc

Dynamic Performance Versus Analog Input Frequency

Fs = 1 Gsps; Fin = 0 up to 1800 MHz; full-scale input (Fs); Fs -3 dB, Fs -10 dB

Clock duty cycle 50/50, binary/gray output coding, fully differential or single-ended analog and clock inputs

Figure 14. ENOB Versus Analog Input Frequency

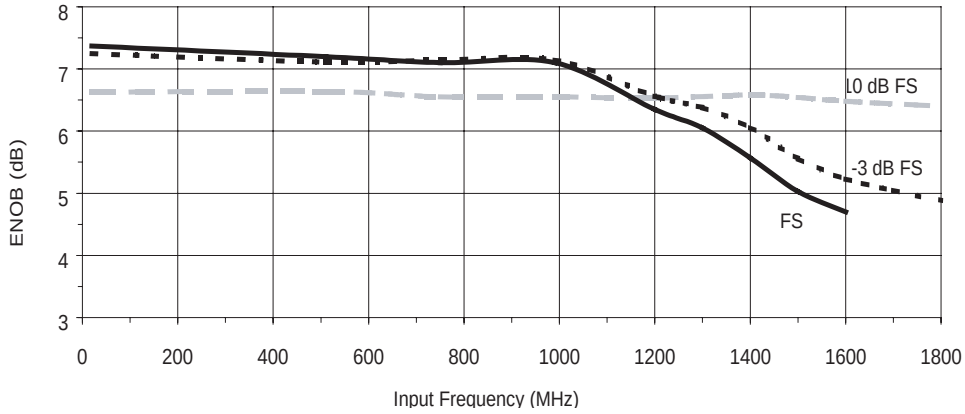


Figure 15. SNR Versus Analog Input Frequency

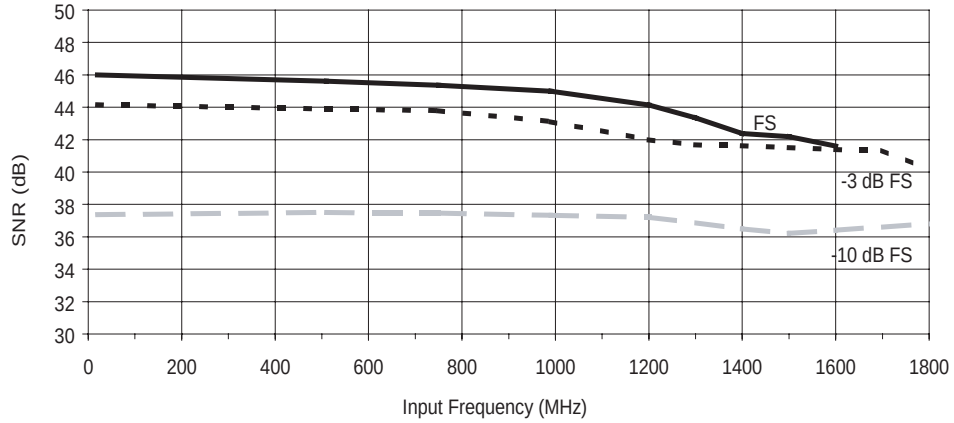


Figure 16. SFDR Versus Analog Input Frequency

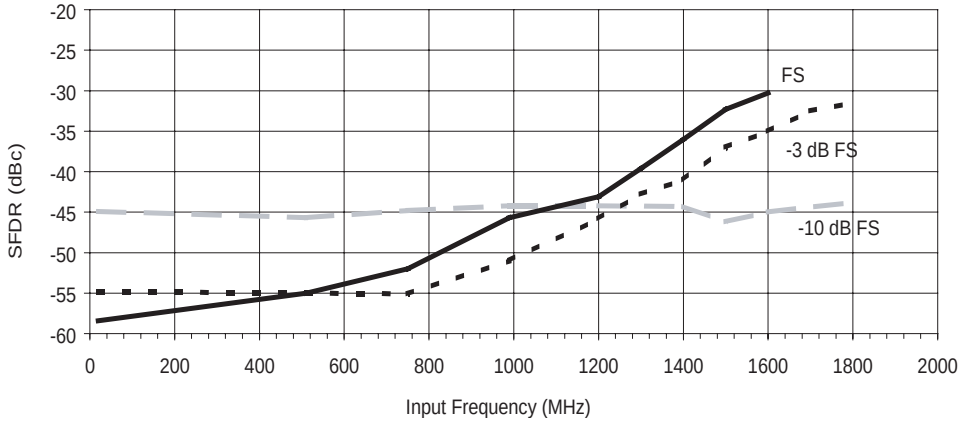


Figure 17. ENOB Versus Sampling Frequency

Analog input frequency: Fin = 500 MHz and Nyquist conditions (Fin = Fs/2)
Clock duty cycle 50/50, binary output coding

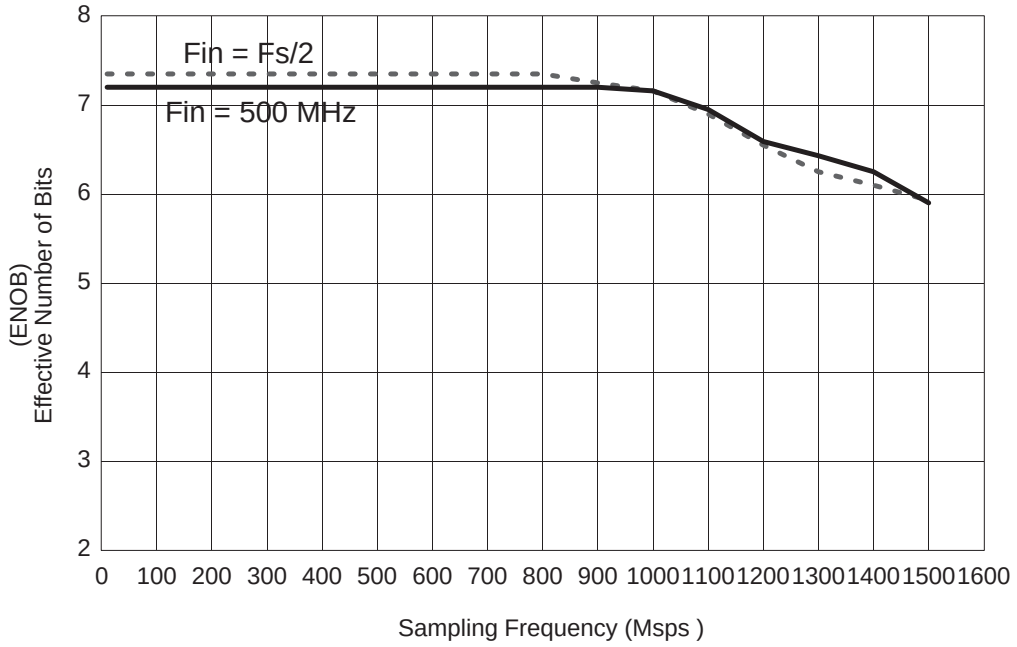
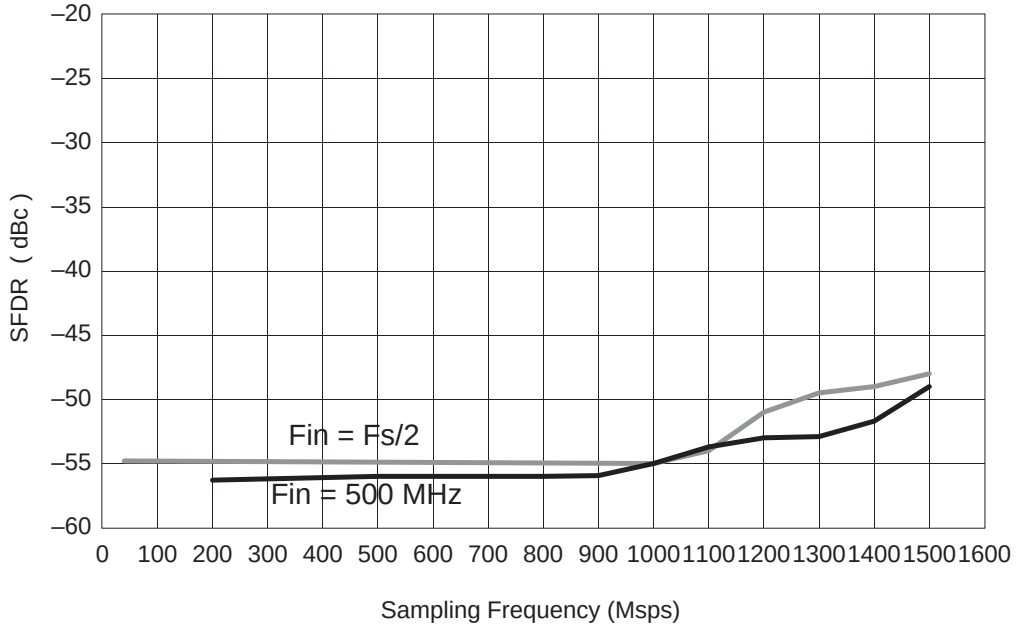


Figure 18. SFDR Versus Sampling Frequency

Analog input frequency: Fin = 500 MHz and Nyquist conditions (Fin = Fs/2)
Clock duty cycle 50/50, binary output coding



JTS8388B ADC Performances Versus Junction Temperature

Figure 19. ENOB Versus Junction Temperature

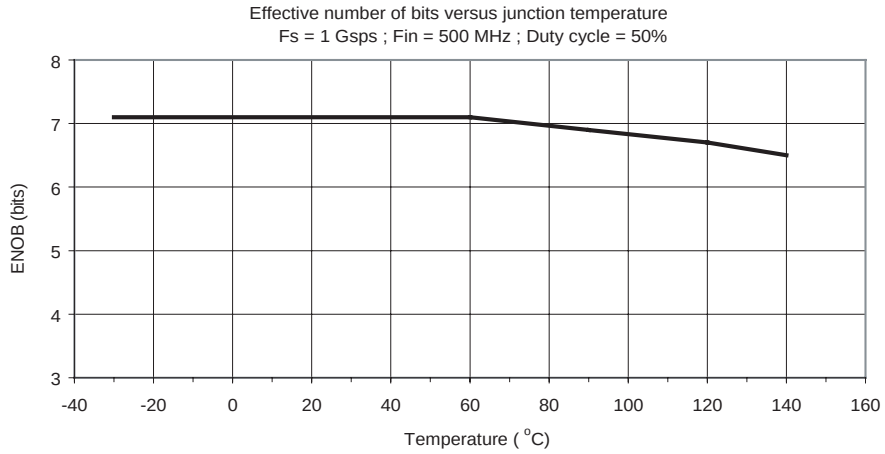


Figure 20. SNR Versus Junction Temperature

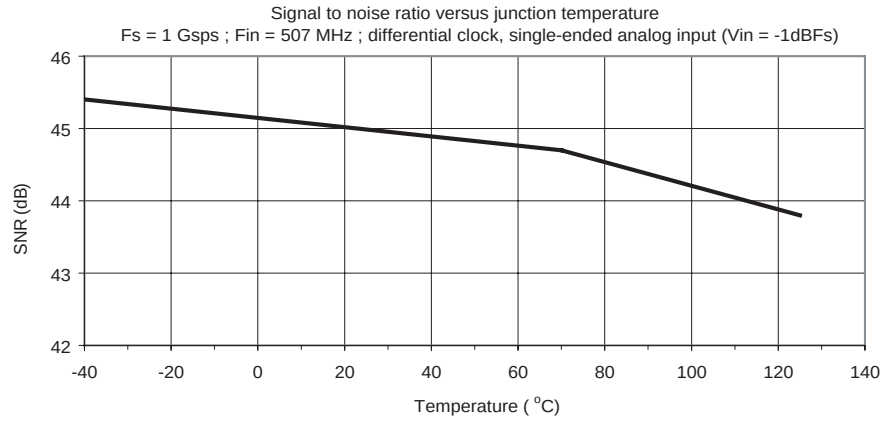


Figure 21. THD Versus Junction Temperature

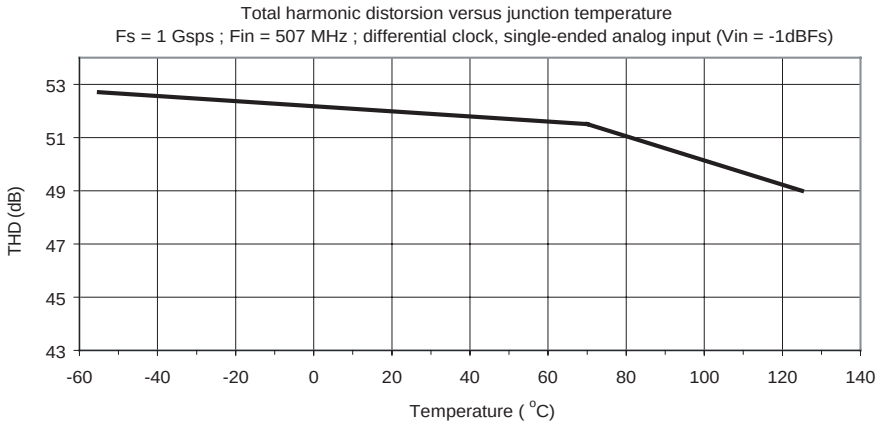


Figure 22. Power Consumption Versus Junction Temperature

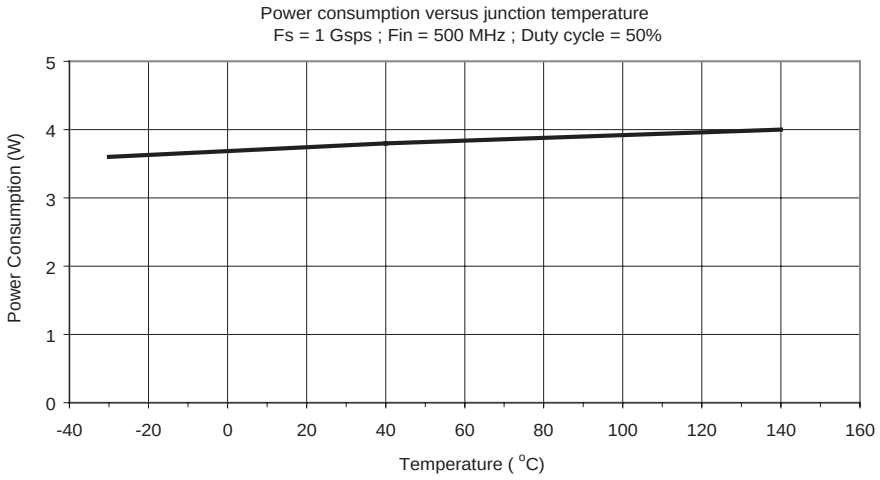
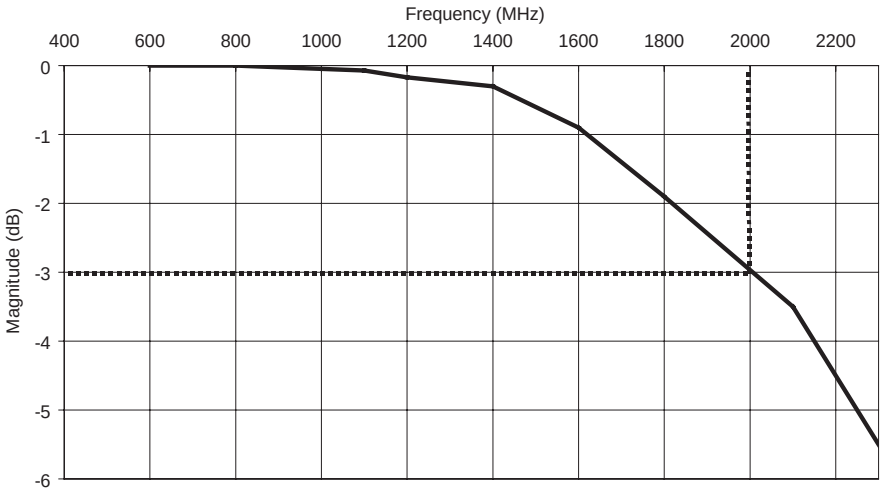


Figure 23. Typical Full Power Input Bandwidth at -3 dB (-2 dBm Full Power Input)



ADC Step Response

Test pulse input characteristics: 20% to 80% input full-scale and rise time ~ 200 ps

Figure 24. Test Pulse Digitized with 20 GHz DSO

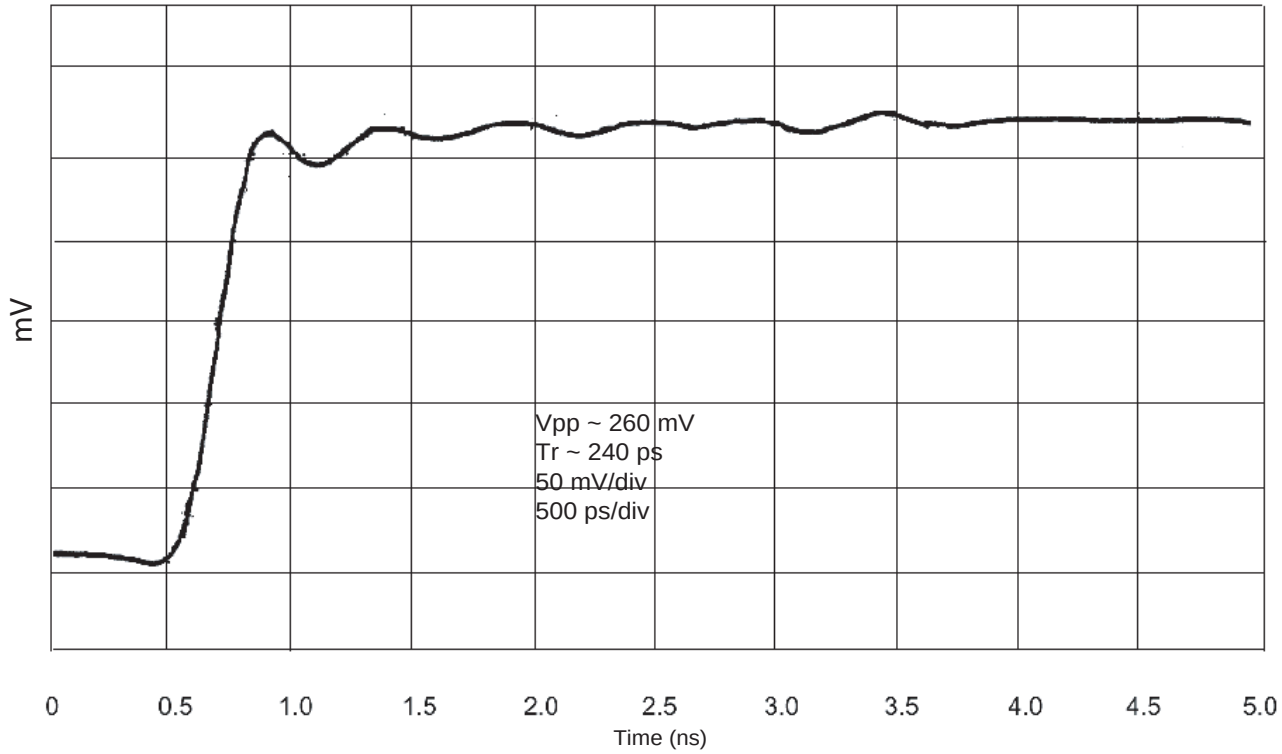
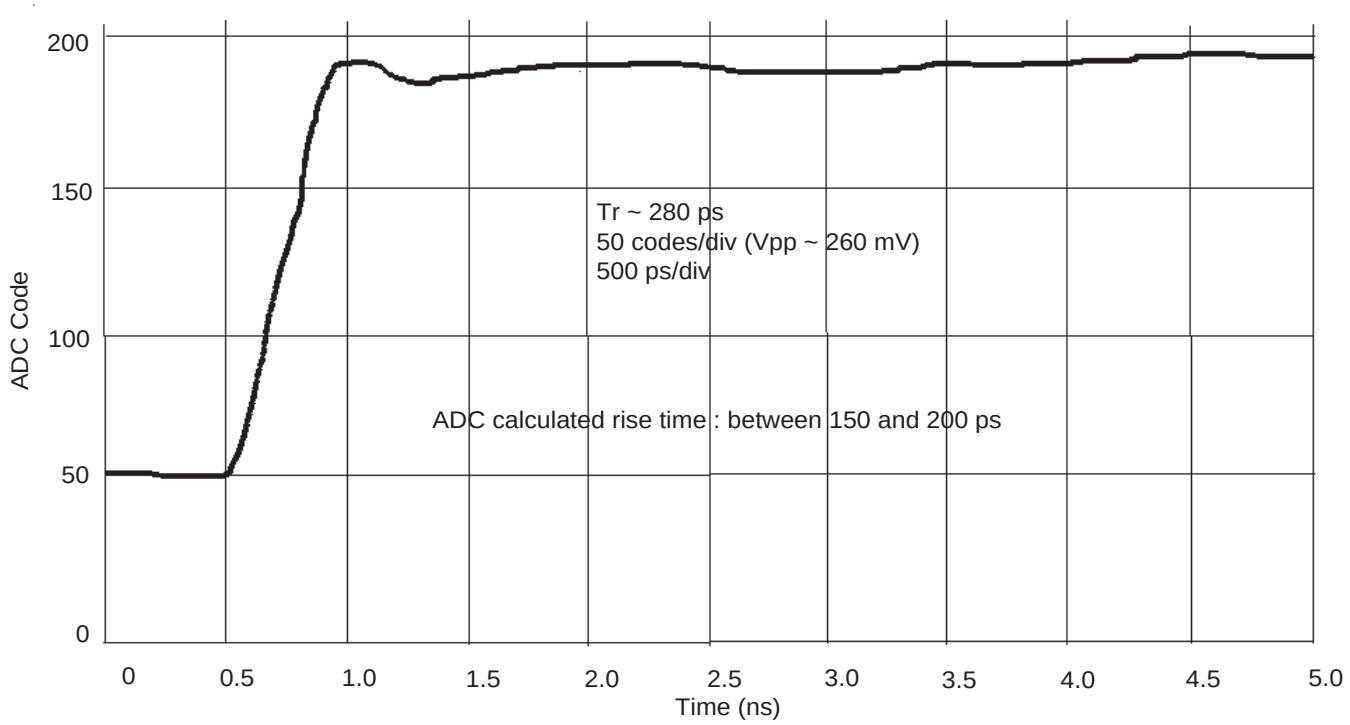


Figure 25. Same Test Pulse Digitized with JTS8388B ADC



Note: Ripples are due to the test setup (they are present on both measurements)

Jitter Performance

Sampling frequency Fs = 500 Msps; Input frequency Fin = 1900 MHz

Figure 26. Single-ended Analog and Clock Inputs

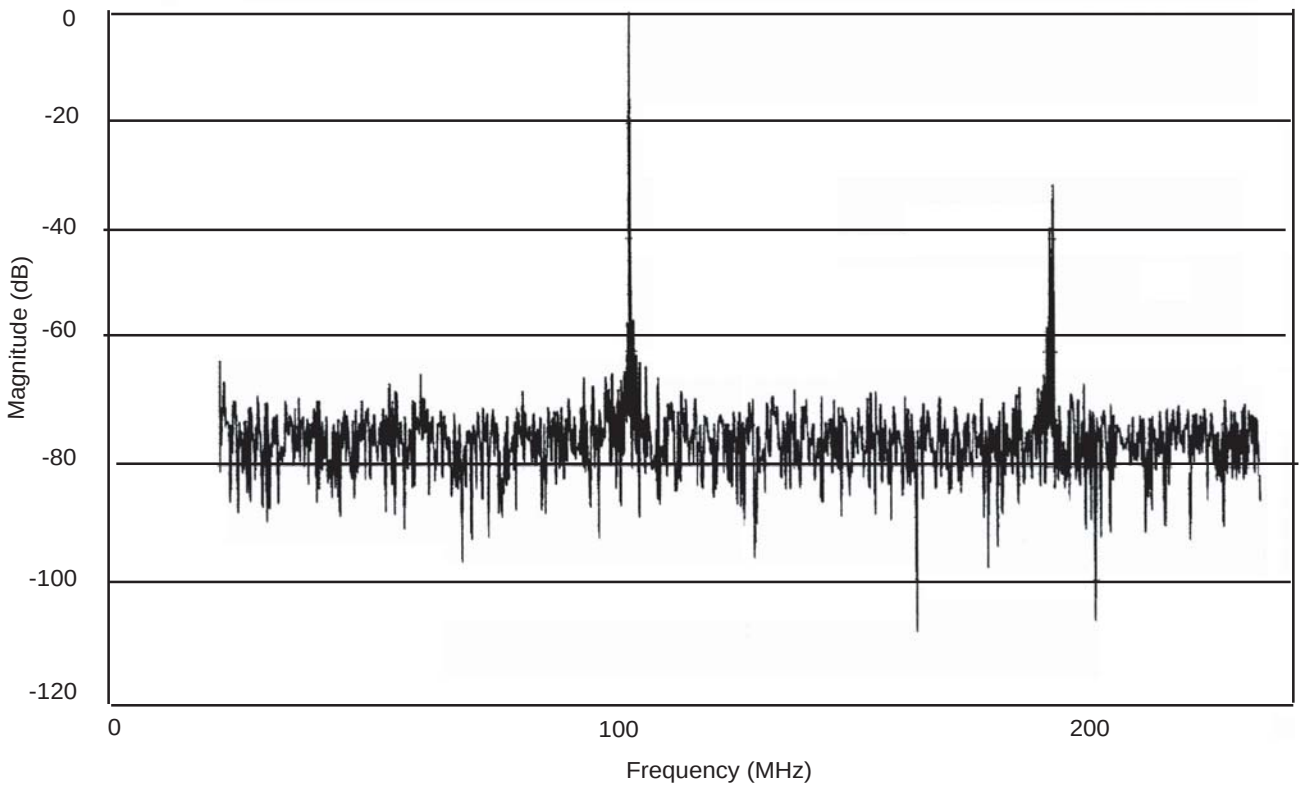
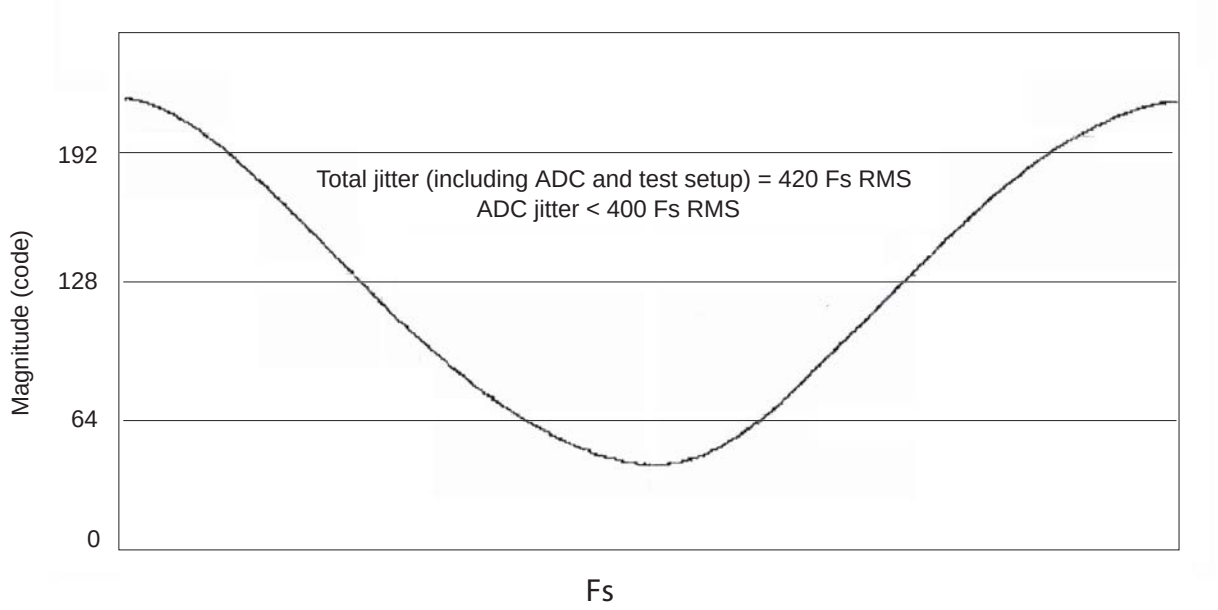


Figure 27. Single-ended Analog and Clock Inputs



Definitions of Terms

Table 7. Definitions of Terms

Term		Description
BER	Bit Error Rate	Probability to exceed a specified error threshold for a sample. An error code is a code that differs by more than ±4 LSB from the correct code
BW	Full-power Input Bandwidth	The analog input frequency at which the fundamental component in the digitally reconstructed output has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale
DG	Differential Gain	The peak gain variation (in percent) at five different DC levels for an AC signal of 20% full-scale peak to peak amplitude. F_{IN} = 5 MHz (TBC)
DNL	Differential Non-linearity	The differential non-linearity for an output code (i) is the difference between the measured step size of code (i) and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic
DP	Differential Phase	The peak phase variation (in degrees) at five different DC levels for an AC signal of 20% full-scale peak to peak amplitude. F_{IN} = 5 MHz (TBC)
ENOB	Effective Number of Bits	$ENOB = \frac{SINAD - 1.76 + 20\log\frac{A}{V/2}}{6.02}$ Where A is the actual input amplitude and V is the full-scale range of the ADC under test
IMD	Inter Modulation Distortion	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products. The input tones levels are at - 7dB full-scale
INL	Integral Non-linearity	The integral non-linearity for an output code (i) is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all INL (i)
JITTER	Aperture Uncertainty	The sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point
NPR	Noise Power Ratio	The NPR is measured to characterize the ADC's performance in response to broad bandwidth signals. When using a notch-filtered broadband white-noise generator as the input to the ADC under test, the Noise to Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
(NRZ)	Non Return to Zero	When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the out-of-range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the out-of-range bit is set to logic one (it is assumed that the input signal amplitude remains within the absolute maximum ratings)
ORT	Overvoltage Recovery Time	Time to recover 0.2% accuracy at the output, after a 150% full-scale step applied on the input is reduced to midscale
PSRR	Power Supply Rejection Ratio	PSRR is the ratio of input offset variation to a change in power supply voltage
SFDR	Spurious Free Dynamic Range	The ratio expressed in dB of the RMS signal amplitude, set at 1 dB below full-scale, to the RMS value of the next highest spectral component (peak spurious spectral component). SFDR is the key parameter for selecting a converter to be used in a frequency domain application (radar systems, digital receiver, network analyzer...). It may be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (i.e. always related back to converter full-scale)

Definitions of Terms

Table 7. Definitions of Terms (Continued)

SINAD	Signal to Noise and Distortion Ratio	The ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full-scale, to the RMS sum of all other spectral components, including the harmonics except DC
SNR	Signal to Noise Ratio	The ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full-scale, to the RMS sum of all other spectral components excluding the five first harmonics
TA	Aperture Delay	The delay between the rising edge of the differential clock inputs (CLK,CLKB) (zero crossing point), and the time at which (V_{IN}, V_{INB}) is sampled
TC	Encoding Clock Period	TC1 = minimum clock pulse width (high) TC = TC1 + TC2 TC2 = minimum clock pulse width (low)
TD1	Time Delay from Data to Data Ready	TD1 is the time difference between Data to Data ready
TD2	Time Delay from Data Ready to Data	General expression is TD1 = TC1 + TDR - TOD with TC = TC1 + TC2 = 1 encoding clock period
TF	Fall Time	Time delay for the output data signals to fall from 80% to 20% of delta between the low level and high level
THD	Total Harmonic Distortion	The ratio expressed in dBc of the RMS sum of the first five harmonic components, to the RMS value of the measured fundamental spectral component
TOD	Digital Data Output Delay	The delay from the falling edge of the differential clock inputs (CLK, CLKB) (zero crossing point) to the next point of change in the differential output data (zero crossing) with a specified load
TPD	Pipeline Delay	The number of clock cycles between the sampling edge of an input data and the associated output data being made available (not taking in account the TOD). For the JTS8388B the TPD is 4 clock periods
TR	Rise Time	Time delay for the output data signals to rise from 20% to 80% of delta between the low level and high level
TRDR	Data Ready Reset Delay	Delay between the falling edge of the Data Ready output asynchronous Reset signal (DDRB) and the reset to digital zero transition of the Data Ready output signal (DR)
TS	Settling Time	Time delay to achieve 0.2% accuracy at the converter output when an 80% full-scale step function is applied to the differential analog input

Applying the JTS8388B

Timing Information

Timing Values for JTS8388B

Timing values are given at chip inputs/outputs, taking into account pad and ESD protection capacitance, 2 mm (30 um diameter) bonding wire per pad, and specified termination loads.

Propagation delays in 50/75 Ω impedance traces are not taken into account for TOD and TDR.

Apply proper derating values corresponding to termination topology.

The min/max timing values are valid over the full temperature range in the following conditions:

- Specified termination load (differential output Data and Data Ready): 50 Ω resistor in parallel with 1 standard ECLinPS register from Motorola® (e.g. 10E452). Typical ECLinPS inputs show a typical input capacitance of 1.5 pF (including package and ESD protections). When addressing an output DMUX, if some digital outputs do not have the same termination load, apply the corresponding derating value given below.
- Output termination load derating values for TOD and TDR: ~ 60 ps/pF or 75 ps per additional ECLinPS load.
- Propagation time delay derating values also have to be applied for TOD and TDR: ~6 ps/mm (155 ps/inch) for the TSEV8388B Evaluation Board. Apply the proper time delay derating value if a different dielectric layer is used.

Propagation Time Considerations

TOD and TDR timing values are given from pad to pad and do not include the additional propagation times between die pads and input/output termination loads. For the TSEV8388B Chip Evaluation Board, the propagation time delay is 6 ps/mm (155 ps/inch) corresponding to 3.4 (at 10 GHz) dielectric constant of the RO4003 used for the board.

If a different dielectric layer is used (for instance teflon), use appropriate propagation time values. TD does not depend on propagation times because it is a differential data (TD is the time difference between Data Ready output delay and digital data output delay).

TD is also the most straightforward data to measure, again because it is differential: TD can be measured directly onto termination loads, with matched oscilloscope probes.

TOD - TDR Variation Over Temperature

Values for TOD and TDR track each other over temperature (1 percent variation for TOD - TDR per 100 degrees celsius temperature variation). Therefore, TOD - TDR variation over temperature is negligible. Moreover, the internal (onchip) and package skews between each data TOD and TDR effect can be considered negligible.

Consequently, minimum values for TOD and TDR are never more than 100 ps apart. The same is true for the TOD and TDR maximum values. In other words:

- If TOD is at 950 ps, TDR will not be at 1420 ps (maximum time delay for TDR)
- If TOD is at 1460 ps, TDR will not be at 910 ps (minimum time delay for TDR) However, external TOD - TDR values may be dictated by total digital data skews between each TOD (each digital data) and TDR: MCM board, bonding wires and differences in output line lengths, and mismatches in output termination impedance.

The external (on board) skew effect has not been taken into account for the specification of the minimum and maximum values for TOD-TDR.

Principle of Operation

The analog input is sampled on the rising edge of the external clock input (CLK,CLKB) after a TA (aperture delay) of typically 250 ps.

The digitized data is available after 4 clock periods latency (pipeline delay (TPD)), on the clock's rising edge, after 1160 ps typical propagation delay TOD.

The Data Ready differential output signal frequency (DR, DRB) is half the external clock frequency, that is it switches at the same rate as the digital outputs.

The Data Ready output signal (DR, DRB) switches on the external clock's falling edge after a propagation delay TDR of typically 1120 ps.

A Master Asynchronous Reset input command DRRB (ECL-compatible single-ended input) is available for initializing the differential Data Ready output signal (DR, DRB). This feature is mandatory in certain applications using interleaved ADCs or using a single ADC with demultiplexed outputs. Without Data Ready signal initialization, it is impossible to store the output digital data in a defined order.

Principle of Data Ready Signal Control by DRRB Input Command

Data Ready Output Signal Reset

The Data Ready signal is reset on the falling edge of the DRRB input command, on the ECL logical low level (-1.8 V). DRRB may also be tied to V_{EE} = -5 V for Data Ready output signal Master Reset. As long as DRRB remains at a logical low level, (or tied to V_{EE} = -5 V), the Data Ready output remains at a logical zero and is independent of the external free-running encoding clock.

The Data Ready output signal (DR, DRB) is reset to logical zero after TRDR = 720 ps typical.

TRDR is measured between the -1.3 V point of the falling edge of the DRRB input command and the zero crossing point of the differential Data Ready output signal (DR, DRB).

The Data Ready Reset command may be a pulse of 1 ns minimum time width.

Data Ready Output Signal Restart

The Data Ready output signal restarts on the DRRB command's rising edge, ECL logical high levels (-0.8 V).

DRRB may also be grounded, or may be allowed to float, for a normal free-running Data Ready output signal.

The Data Ready signal restart sequence depends on the logical level of the external encoding clock, at a DRRB rising edge instant.

- The DRRB rising edge occurs when the external encoding clock input (CLK,CLKB) is LOW:

  The Data Ready output's first rising edge occurs after half a clock period on the clock falling edge, after a delay time TDR = 1120 ps already defined above.
- The DRRB rising edge occurs when the external encoding clock input (CLK,CLKB) is HIGH:

The Data Ready output's first rising edge occurs after one clock period on the clock falling edge, and a delay TDR = 1120 ps.

Consequently, as the analog input is sampled on the clock's rising edge, the first digitized data corresponding to the first acquisition (N) after a Data Ready signal restart (rising edge) is always strobed by the third rising edge of the Data Ready signal.

The time delay (TD1) is specified between the last point of a change in the differential output data (zero crossing point) to the rising or falling edge of the differential Data Ready signal (DR, DRB) (zero crossing point).

- For normal initialization of the Data Ready output signal, the external encoding clock signal frequency and level must be controlled. The minimum encoding clock sampling rate for the ADC is 10 Msps and consequently the clock cannot be stopped.
- One single pad is used for both the DRRB input command and die junction temperature monitoring. The pad denomination will be DRRB/DIOD (on the former version the denomination was DIOD).
- Temperature monitoring and Data Ready control by DRRB is not possible simultaneously.

Analog Inputs (VIN) (VINB)

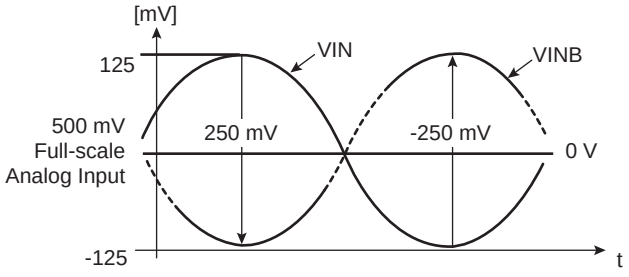
The analog input full-scale range is 0.5 V (Vpp), or -2 dBm into the 50 Ω termination resistor.

In the differential mode input configuration, that means 0.25 V on each input, or ±125 mV around 0 V. The input common mode is ground.

The typical input capacitance is 0.4 pF in die form (JTS8388B), not taking into account the bond wires capacitance.

The input capacitance is mainly due to the pad capacitance, as the ESD protections are not connected (but present) on the inputs.

Figure 28. Differential Inputs Voltage Span



(VIN, VINB) = ±250 mV = 500 mV diff

Differential Versus Single-ended Analog Input Operation

The JTS8388B can operate at full speed without any performance degradation in either a differential or single-ended configuration.

This is explained by the fact that the ADC uses a high-input impedance differential preamplifier stage, (preceding the Sample and Hold stage), which has been designed in order to be entered either in differential or single-ended mode.

This is true so long as the out-of-phase analog input pad VINB is 50 Ω terminated very closely to one of the neighboring shield ground pads (33, 35, 37), which constitute the local ground reference for the in-phase analog input pad (VIN).

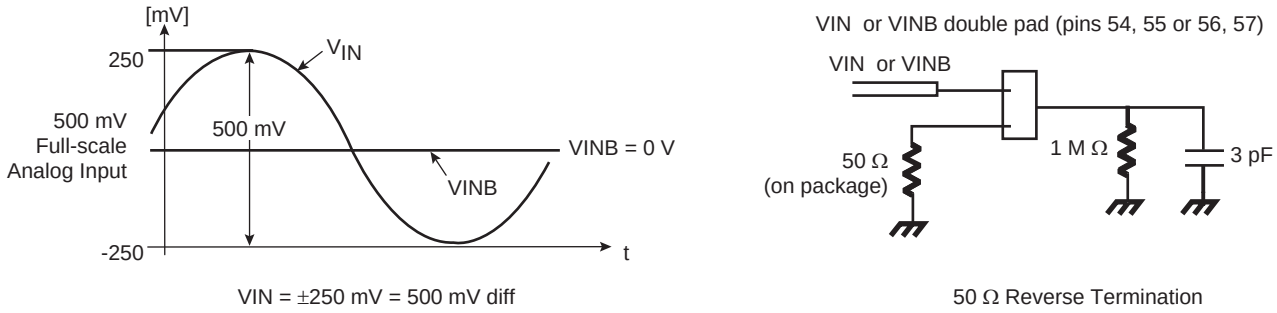
Thus, the differential analog input preamplifier will fully reject the local ground noise (and any capacitively and inductively coupled noise) as common mode effects.

In a typical single-ended configuration, enter on the (VIN) input pad, with the inverted phase input pad (VINB) grounded through the 50 Ω termination resistor.

In a single-ended input configuration, the in-phase input amplitude is 0.5 V, centered on 0 V (or -2 dBm into 50 Ω).

The inverted phase input is at ground potential through the 50 Ω termination resistor.

Figure 29. Typical Single Ended Analog Input Configuration



VIN = ±250 mV = 500 mV diff

50 Ω Reverse Termination

Clock Inputs (CLK) (CLKB)

The JTS8388B can be clocked at full speed without noticeable performance degradation in either the differential or single-ended configuration.

This is explained by the fact the ADC uses a differential preamplifier stage for the clock buffer, which has been designed to be entered either in a differential or single-ended mode.

Single-ended Clock Input (Ground Common Mode)

Although the clock inputs were intended to be driven differentially with nominal -0.8 V/-1.8 V ECL levels, the JTS8388B clock buffer can manage a single-ended sine-wave clock signal centered around 0 V. This is the most convenient clock input configuration as it does not require the use of a power splitter.

No performance degradation (e.g. due to timing jitters) is observed in this particular single-ended configuration up to 1.2 Gsps Nyquist conditions (Fin = 600 MHz).

This is true so long as the inverted phase clock input pad is 50 Ω terminated very closely to one of the neighboring shield ground pads, which constitutes the local ground reference for the in-phase clock input.

Thus, the JTS8388B differential clock input buffer will fully reject the local ground noise (and any capacitively and inductively coupled noise) as common mode effects.

Moreover, a very low-phase noise sinewave generator must be used for enhanced jitter performance.

The typical in-phase clock input amplitude is 1 V, centered on a 0 V (ground) common mode.

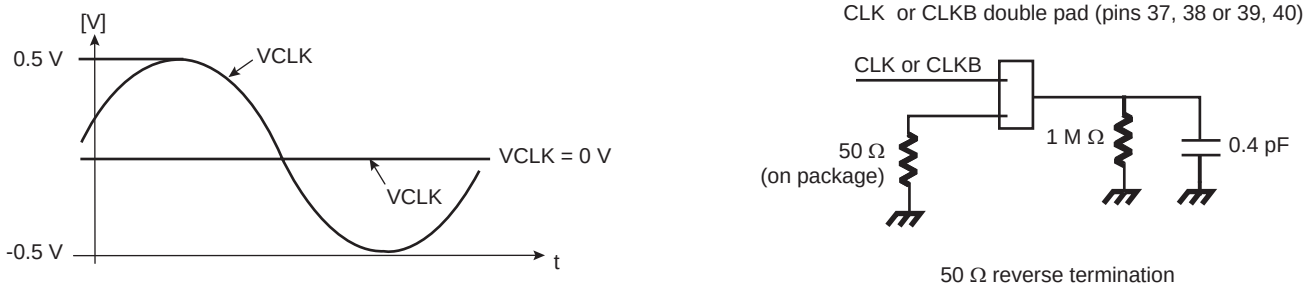
This corresponds to a typical clock input power level of 4 dBm into the 50 Ω termination resistor.

Do not exceed 10 dBm to avoid saturation of the preamplifier input transistors.

The inverted phase clock input is grounded through the 50 Ω termination resistor.

Figure 30. Single-ended Clock Input (Ground Common Mode)

VLCLK common mode = 0 V; VCLKB = 0 V; 4 dBm typical clock input power level (into 50 Ω termination resistor



Note: Do not exceed 10 dBm into the 50 Ω termination resistor for single clock input power level.

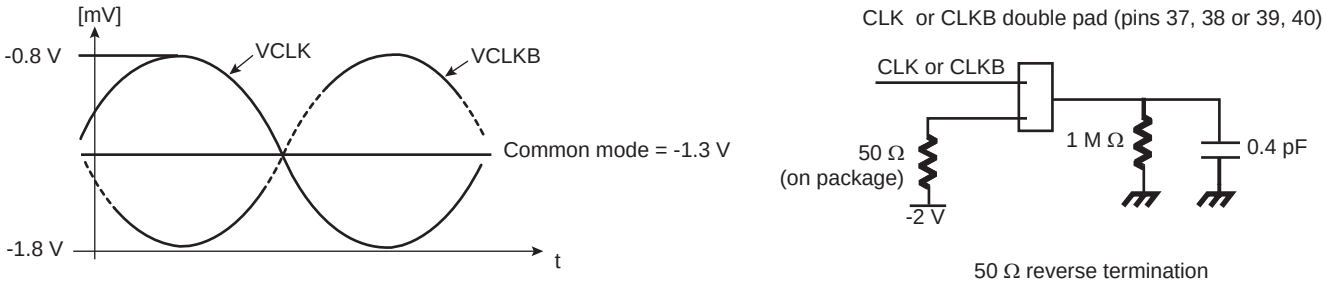
Differential ECL Clock Input

The clock inputs can be driven differentially with nominal -0.8 V/-1.8 V ECL levels.

In this mode, a low-phase noise sinewave generator can be used to drive the clock inputs, followed by a power splitter (hybrid junction) in order to obtain 180 degrees out-of-phase sinewave signals. Biasing tees can be used for offsetting the common mode voltage to ECL levels.

Note: As the biasing tees propagation times are not matching, a tunable delay line is required in order to ensure the signals are 180 degrees out-of-phase especially at fast clock rates in the Gsps range.

Figure 31. Differential Clock Inputs (ECL Levels)

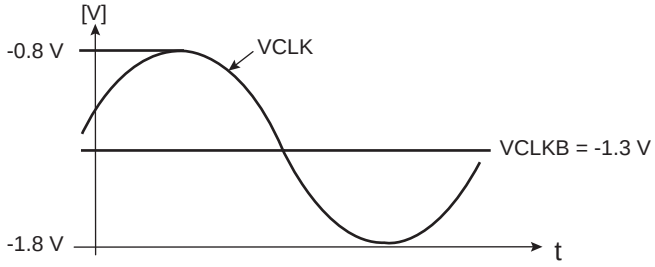


Single Ended ECL Clock Input

In a single-ended configuration enter on the CLK (resp. CLKB) pad, with the inverted phase clock input pad CLKB (respectively CLK) connected to -1.3 V through the 50 Ω termination resistor.

The in-phase input amplitude is 1 V, centered on a -1.3 V common mode.

Figure 32. Single-ended Clock Input (ECL)



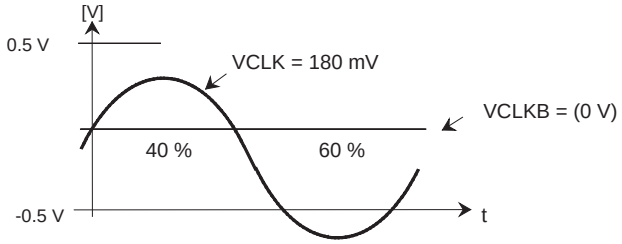
VCLK common mode = -1.3 V, VCLKB = -1.3 V

Clock Signal Duty Cycle Adjust

At fast sampling rates, (1 Gsps and above), the device performance (especially the SNR) can be improved by tuning the clock duty cycle (CLK, CLKB).

In a single-ended configuration, when using a sinewave clock generator, the clock signal duty cycle can be easily adjusted by simply offsetting the in-phase clock signal using a biasing tee, (as the out of phase clock input is at ground level).

Figure 33. Single-ended Clock Input (In-phase Clock Input Common Mode Shifted)



VCLK common mode = -180 mV, VCLKB = 0 V

Note: 1. Do not exceed 10 dBm into the 50 Ω termination resistor for single clock input power level.

2. For an input CLK signal of 4 dBm into 50 Ω, the typical offset value to achieve a 40/60 clock duty cycle is -180 mV on CLK.

Noise Immunity Information

Circuit noise immunity performance begins at the design level.

Efforts have been made on the design to make the device as insensitive as possible to chip environment perturbations resulting from the circuit itself or induced by external circuitry (cascade stages isolation, internal damping resistors, clamps, internal (on-chip) decoupling capacitors).

Furthermore, the fully differential operation from the analog input up to the digital output provides enhanced noise immunity by common mode noise rejection.

Common mode noise voltage induced on the differential analog and clock inputs will be canceled out by these balanced differential amplifiers.

Moreover, proper active signals shielding has been provided on the chip to reduce the amount of coupled noise on the active inputs:

The analog inputs and clock inputs of the TS8388B chip have been surrounded by ground pads, which must be directly connected to the external ground plane.

Digital Outputs

The JTS8388B differential output buffers are internally 75 Ω loaded. The 75 Ω resistors are connected to the digital ground pads through a -0.8 V level shift diode (see Figures 34 and 35 on page 38 and Figure 36 on page 39).

The JTS8388B output buffers are designed for driving 75 Ω (default) or 50 Ω properly terminated impedance lines or coaxial cables.

An 11 mA bias current flowing alternately into one of the 75 Ω resistors when switching, ensures a 0.825 voltage drop across the resistor (unterminated outputs).

The V_{PLUSD} positive supply voltage allows the adjustment of the output common mode level from -1.2 V (V_{PLUSD} = 0 V for ECL output compatibility) to 1.2 V (V_{PLUSD} = 2.4 V for LVDS output compatibility). Therefore, the single-ended output voltages vary approximately between -0.8 V and -1.625 V (outputs unterminated), around -1.2 V common mode voltage.

Three possible line driving and back termination scenarios are proposed (assuming V_{PLUSD} = 0 V):

1. 75 Ω impedance transmission lines, 75 Ω differentially terminated (Figure 34): each output voltage varies between -1 V and -1.42 V (respectively 1.4 V and 1 V), leading to ±0.41 V = 0.825 V in differential, around -1.21 V (respectively 1.21 V) common mode for V_{PLUSD} = 0 V (respectively 2.4 V).
2. 50 Ω impedance transmission lines, 50 Ω differentially termination (Figure 35): each output voltage varies between -1.02 V and -1.35 V (respectively 1.38 V and 1.05 V), leading to ±0.33 V = 660 mV in differential, around -1.18 V (respectively 1.21 V) common mode for V_{PLUSD} = 0 V (respectively 2.4 V).
3. 75 Ω impedance open transmission lines (Figure 36): each output voltage varies between -1.6 V and -0.8 V (respectively 0.8 V and 1.6 V), which are true ECL levels, leading to ±0.8 V = 1.6 V in differential, around -1.2 V (respectively 1.2 V) common mode for V_{PLUSD} = 0 V (respectively 2.4 V).

Therefore, it is possible to drive high input impedance storing registers directly, without terminating the 75 Ω transmission lines.

In the time domain, this means the incident wave will reflect at the 75 Ω transmission line output and travel back to the generator (i.e. the 75 Ω data output buffer). As the buffer output impedance is 75 Ω, no back reflection will occur.

Note: This is no longer true if a 50 Ω transmission line is used, as the latter is not matching the buffer 75 Ω output impedance.

Each differential output termination length must be kept identical.

It is recommended to decouple the midpoint of the differential termination with a 10 nF capacitor to avoid common mode perturbation in case of slight mismatch in the differential output line lengths.

Too large mismatches (keep < a few mm) in the differential line lengths will lead to switching currents flowing into the decoupling capacitor, in turn leading to switching ground noise.

The differential output voltage levels (75 or 50 Ω termination) are not ECL standard voltage levels. However, it is possible to drive standard logic ECL circuitry like the ECLinPS logic line from Motorola®.

At sampling rates exceeding 1 Gsps, it may be difficult to trigger the HP16500 or any other acquisition system with digital outputs.

It becomes necessary to regenerate digital data and Data Ready by means of external amplifiers, in order to be able to test the JTS8388B at its optimum performance conditions.

Differential Output Loading Configurations

(levels for ECL compatibility)

Figure 34. Differential Output: 75 Ω Terminated

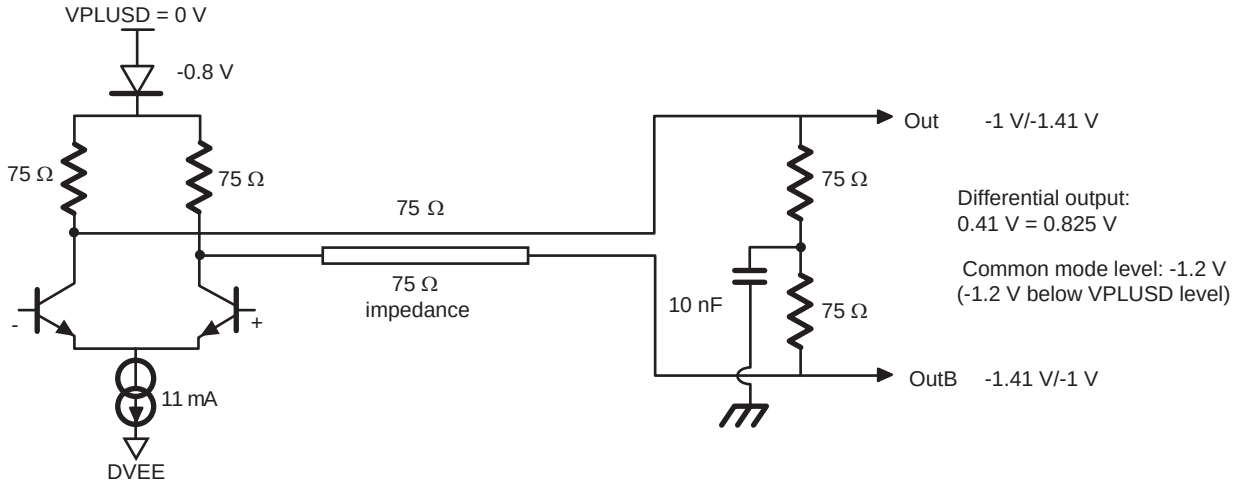


Figure 35. Differential Output: 50 Ω Terminated

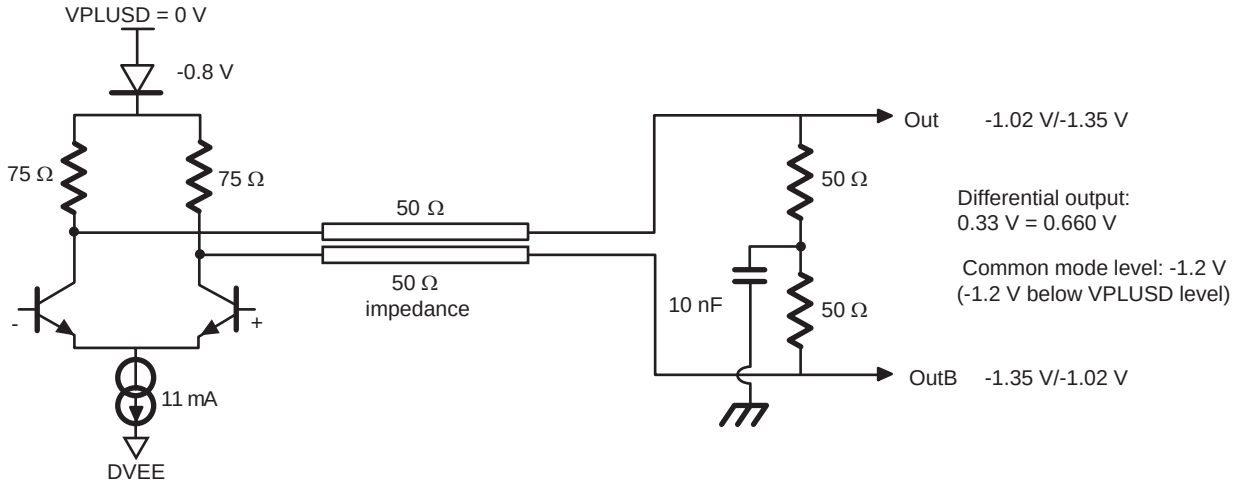
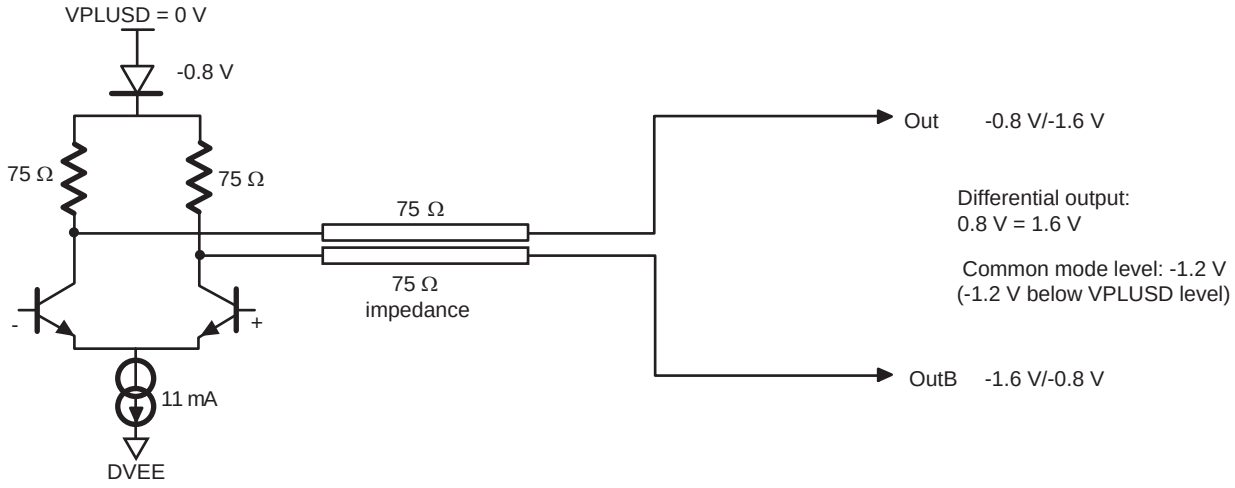


Figure 36. Differential Output: Open Loaded



Differential Output Loading Configurations

(levels for LVDS compatibility)

Figure 37. Differential Output: 75 Ω Terminated

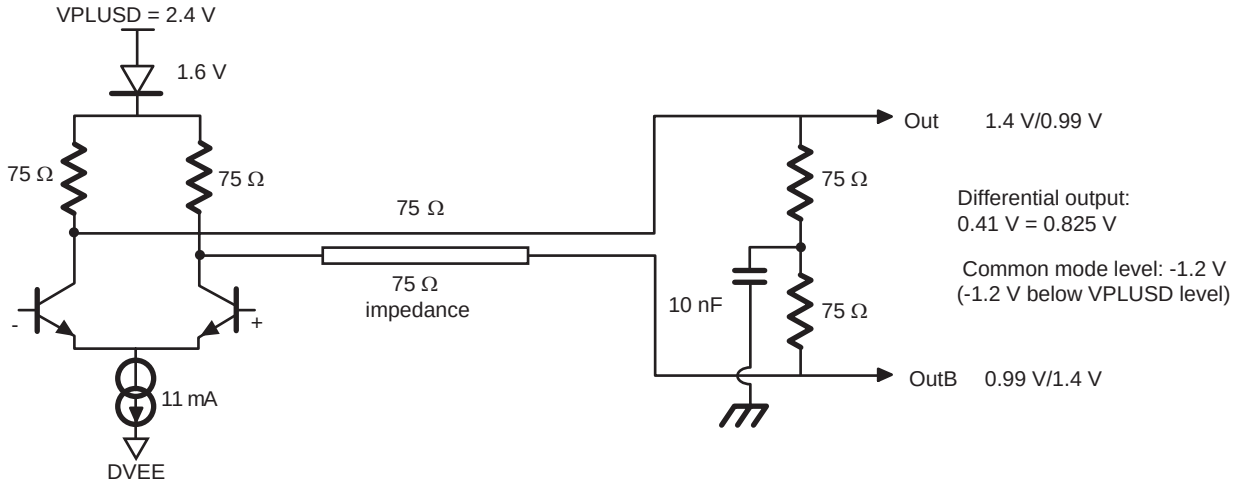


Figure 38. Differential Output: 50 Ω Terminated

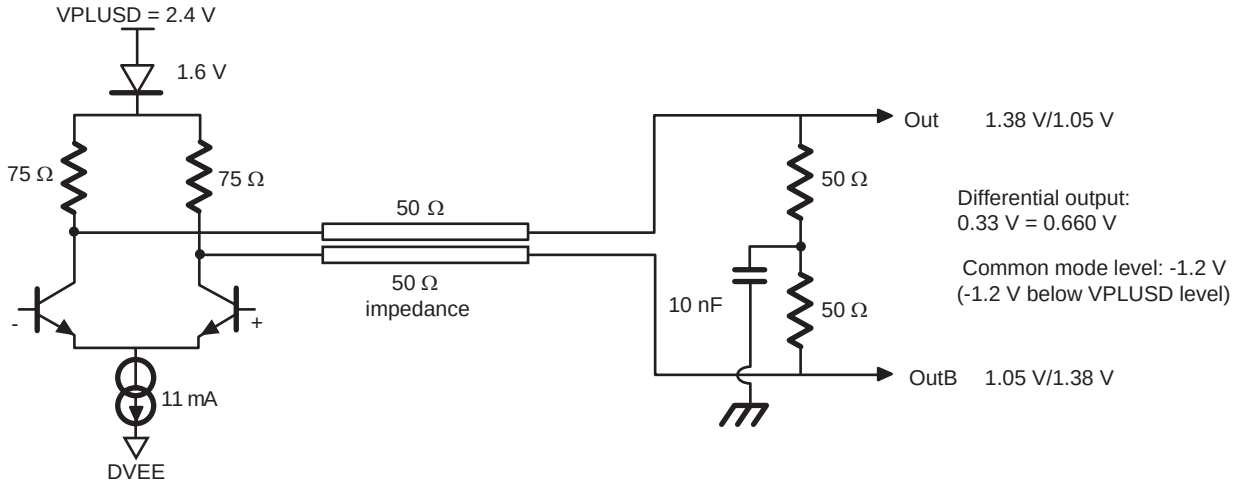
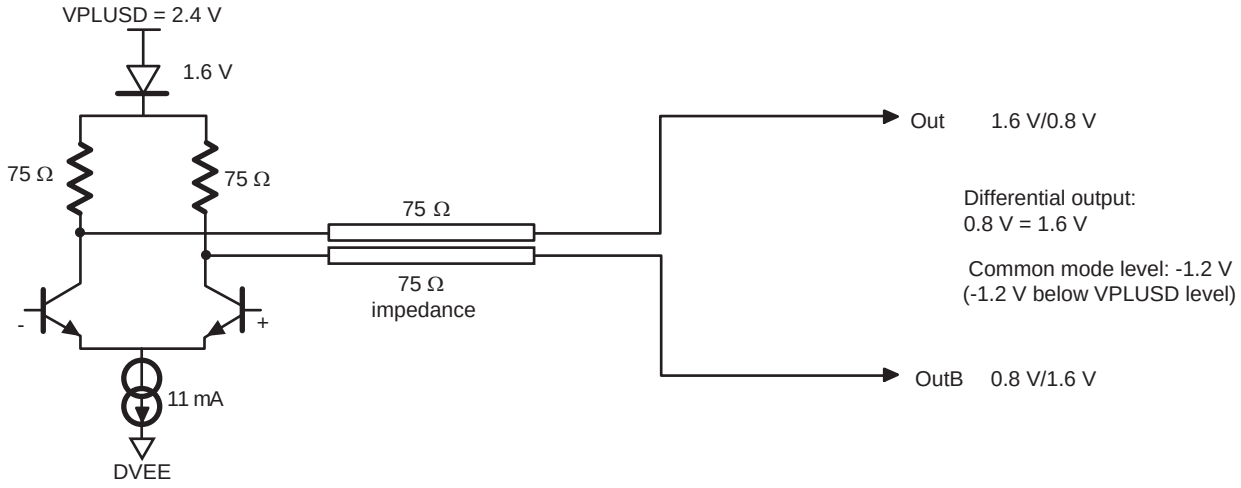


Figure 39. Differential Output: Open Loaded



Out-of-range Bit

An out-of-range (OR, ORB) bit is provided that reaches a logical high state when the input exceeds the positive full-scale or falls below the negative full-scale.

When the analog input exceeds the positive full-scale, the digital outputs remain at a logical high state with OR, ORB at a logical 1.

When the analog input falls below the negative full-scale, the digital outputs remain at a logical low state with OR, ORB at a logical 1 again.

Gray or Binary Output Data Format Select

The JTS8388B internal regeneration latches indecision (for inputs very close to the latches' threshold) may produce errors in the logic encoding circuitry and lead to large amplitude output errors.

This is due to the fact that the latches regenerate the internal analog residues into logical states with a finite voltage gain value (Av) within a given positive amount of time $\Delta(t)$:

$Av = \exp(\Delta(t)/\tau)$, with τ as the positive feedback regeneration time constant.

The JTS8388B has been designed for reducing the probability of occurrence of such errors to approximately 10^{-13} (targeted for the JTS8388B at 1 Gsps).

A standard technique for reducing the amplitude of such errors down to ±1 LSB consists of setting the digital output data in gray code format.

Though the JTS8388B has been designed to feature a Bit Error Rate of 10^{-13} with a binary output format, it is possible for the user to choose between the binary or gray output data format, in order to reduce the amplitude of such errors when they occur, by storing gray output codes.

Digital data format selection:

- Binary output format if GORB is floating or V_{CC}
- Gray output format if GORB is connected to ground (0 V)

JTS8388B Thermal Requirements

The JTS8388B is currently mounted on its dedicated Chip Evaluation Board (CEB), which fulfills the device's thermal requirements in still air at room temperature.

For operation in the military temperature range, forced convection is required to maintain the device junction temperature below the specified maximum value.

The JTS8388B's power dissipation is 3.6 W at a 70°C junction temperature, and 3.8 W at a 125°C junction temperature. The die dimensions are 2.44 mm x 3 mm = 7.32 mm^2.

The maximum junction temperature is 145°C.

To correctly manage the power dissipation of the JTS8388B device, the following thermal fixture profile is used, taking into account the die dimensions and power dissipation:

- 7.5°C/W typical value for die attach Ag filled Epoxy glue, but depending on glue film thickness
- 0.5°C/W Copper block
- 1°C/W isolation foil
- 6.5°C/W heatsink (still air)

The heatsink used is the 3334B pin fin heatsink from Thermalloy (also used for cooling the 604 Power PC µP). Its dimensions are 50.70 mm x 50.39 mm x 16.51 mm (1.996 " x 1.984 " x 0.650 ").

The measured die junction to ambient thermal resistance (RTHJA) for the Chip Evaluation Board is approximately 15.5°C/W in still air.

At room temperature (25°C), this yields to a device junction temperature of approximately 80°C, in thermal steady-state conditions.

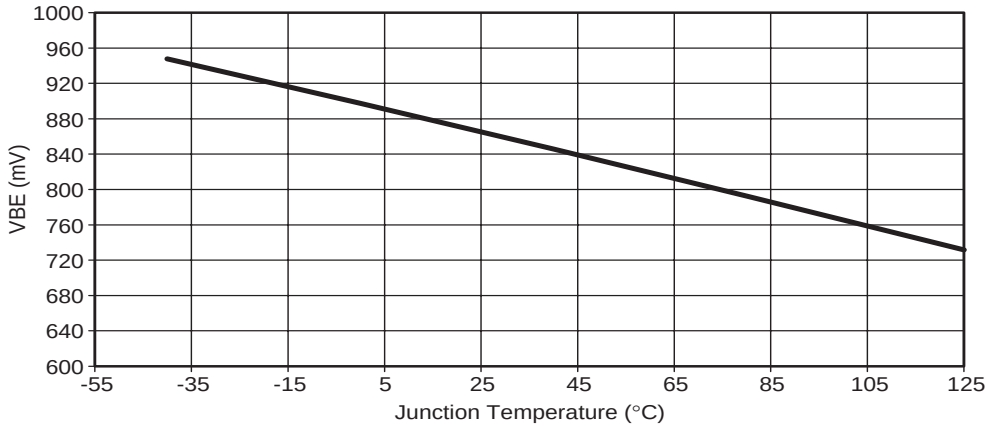
Diode Pad 32

The DIODE pad 32 is provided for die junction temperature monitoring.

The operating die junction temperature must be kept below 145°C, therefore an adequate cooling system has to be set up.

The diode mounted transistor measured Vbe value versus the junction temperature is given below:

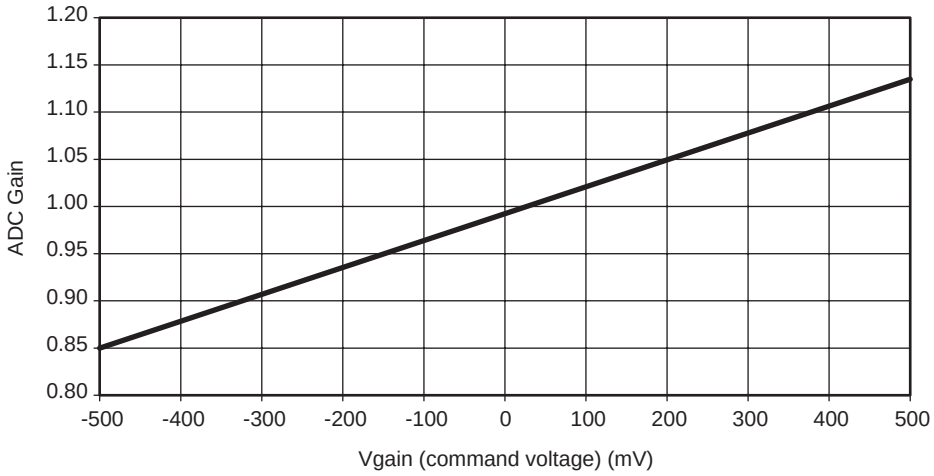
Figure 40. Diode Pad 32



ADC Gain Control Pad 38

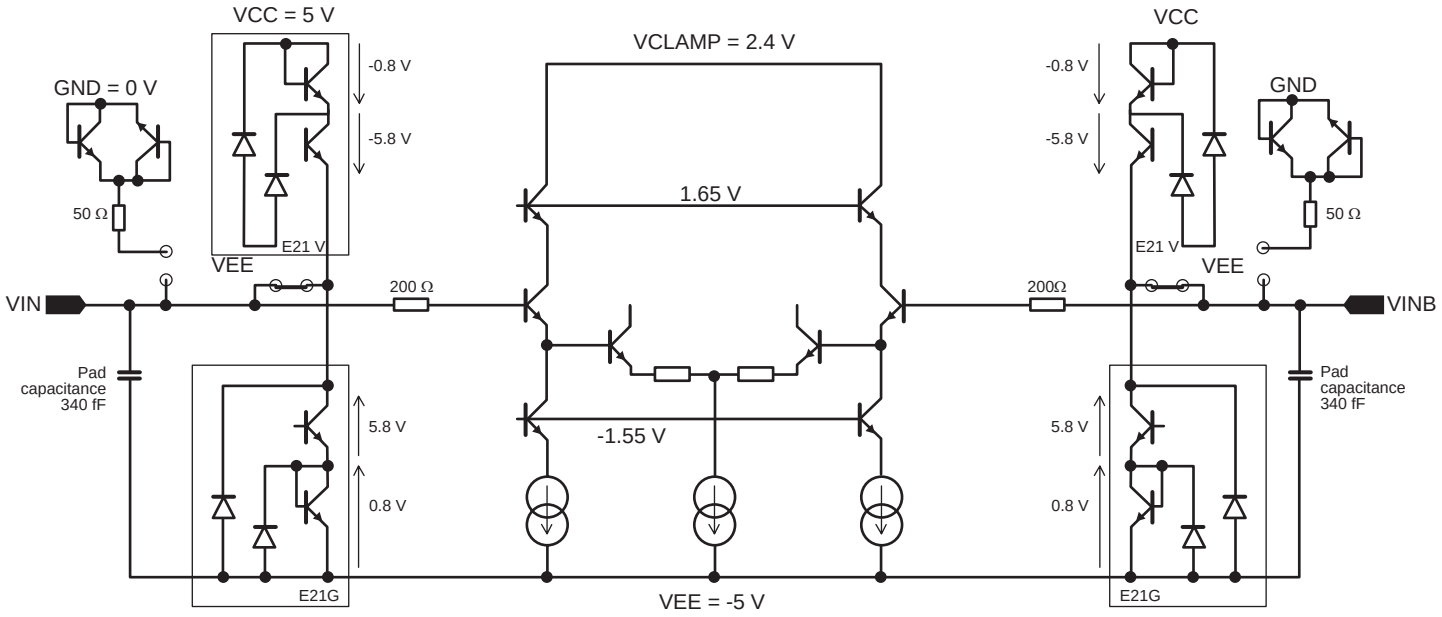
The ADC gain is adjustable by means of pad 38 (input impedance is 1 MΩ in parallel with 2 pF).
The gain adjust transfer function is given below:

Figure 41. ADC Gain Control Pad 38



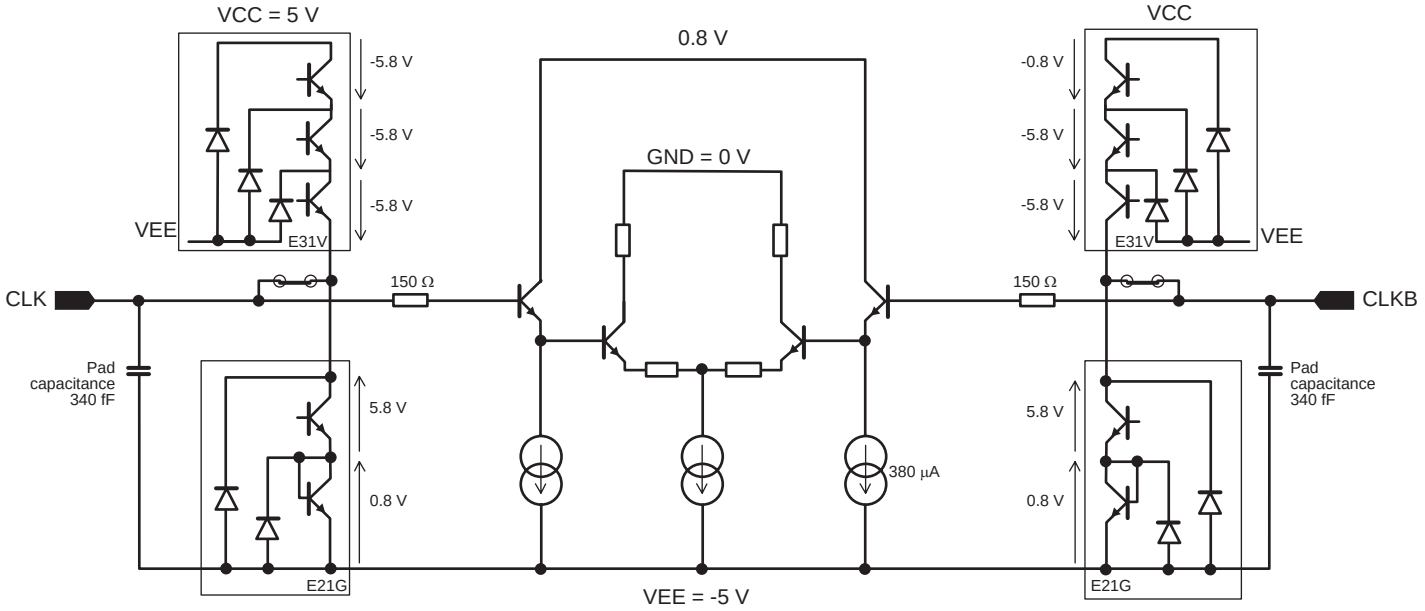
Equivalent Input / Output Schematics

Figure 42. Equivalent Analog Input Circuit and ESD Protections



Note: The ESD protections are present but not connected for Vin and Vinb.

Figure 43. Equivalent Analog Clock Input Circuit and ESD Protections



Note: The ESD protections are present but not connected for Clk and Clkb.

Figure 44. Equivalent Data Output Buffer Circuit and ESD Protections

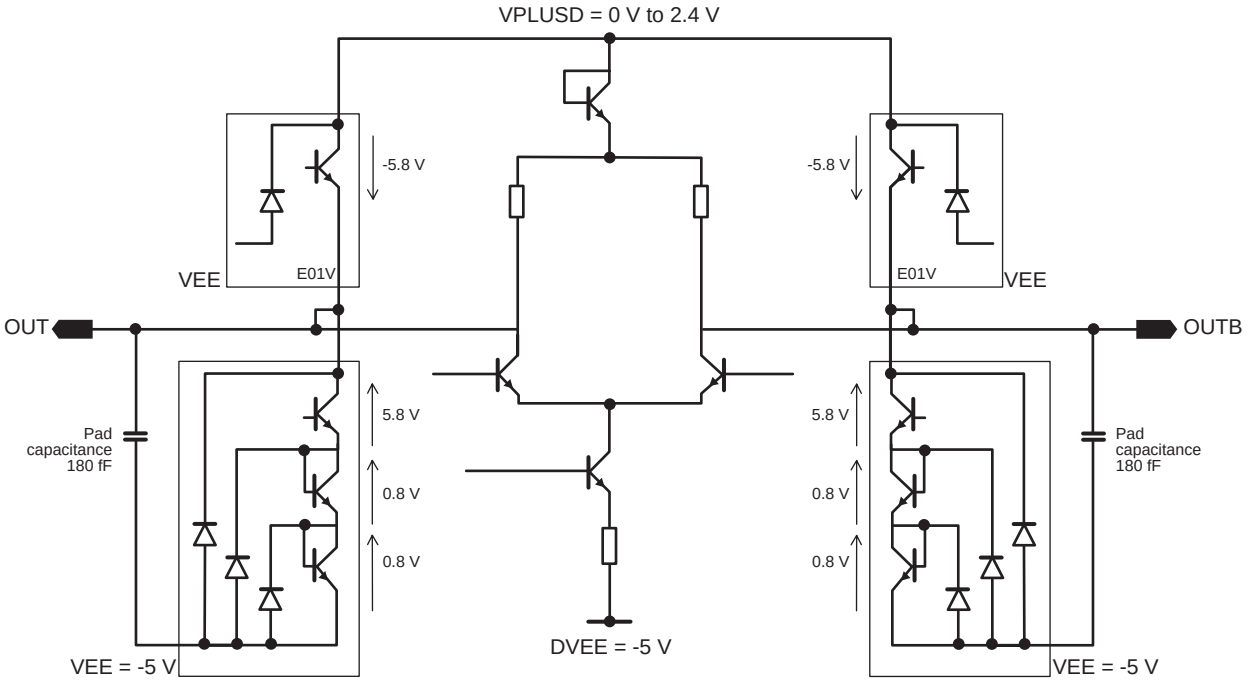


Figure 45. ADC Gain Adjust Equivalent Input Circuits and ESD Protections

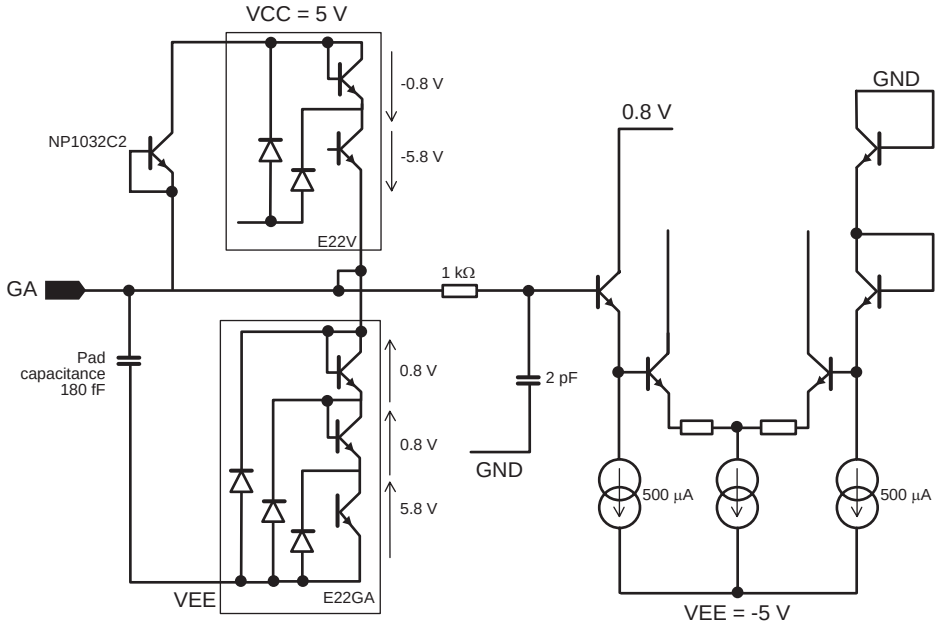
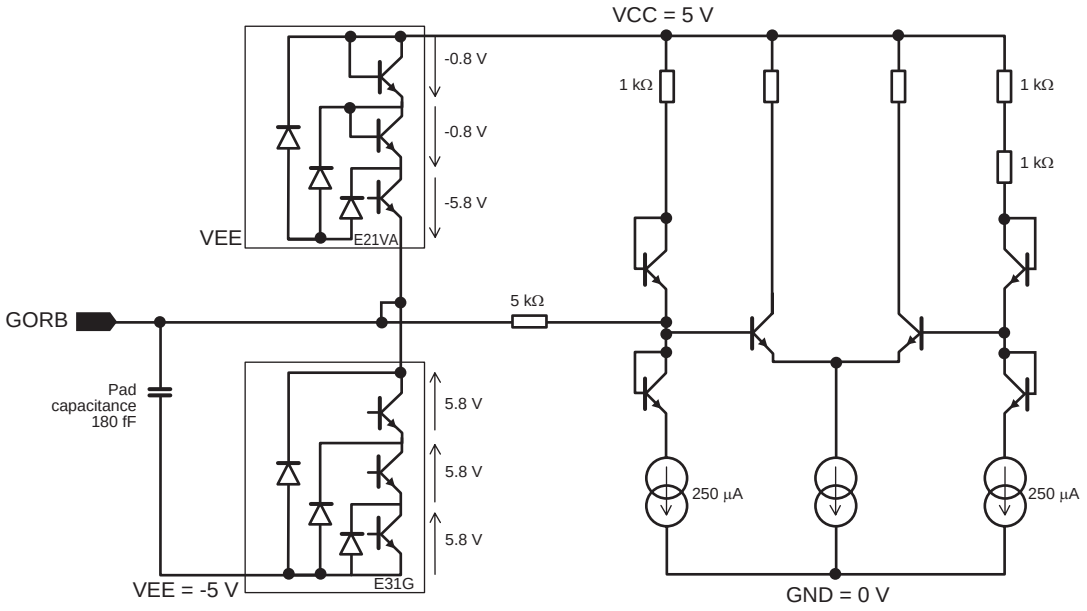
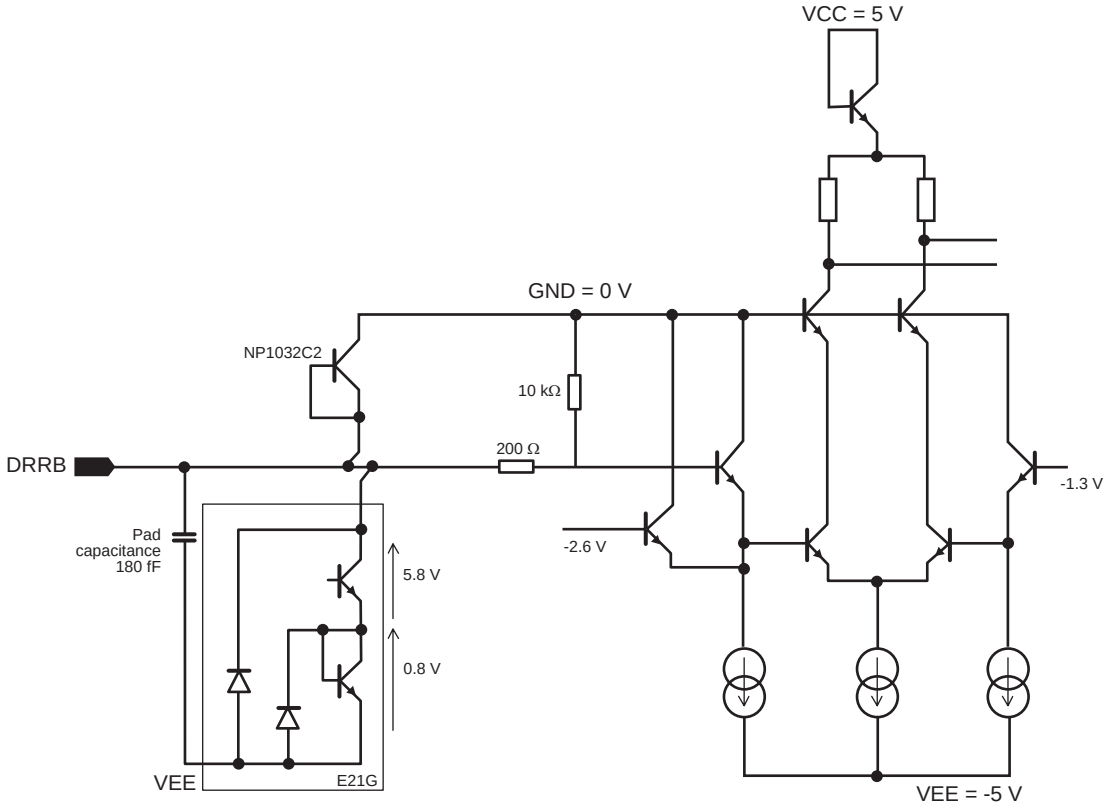


Figure 46. GORB Equivalent Input Schematic and ESD Protections



GORB: gray or binary select input; floating or tied to V_{CC} -> binary

Figure 47. DRRB Equivalent Input Schematic and ESD Protections



Actual protection range: 6.6 V above V_{EE}, in fact stresses above GND are clipped by the CB diode used for T_J monitoring

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