XCR3384XL: 384 Macrocell CPLD

DS024 (v1.7) August 21, 2003 **Preliminary Product Specification**

Features

- Low power 3.3V 384 macrocell CPLD
- 7.5 ns pin-to-pin logic delays
- System frequencies up to 135 MHz
- 384 macrocells with 9,000 usable gates
- Available in small footprint packages
  - 144-pin TQFP (118 user I/O)
  - 208-pin PQFP (172 user I/O)
  - 256-ball FBGA (212 user I/O)
  - 324-ball FBGA (220 user I/O)
- Optimized for 3.3V systems
  - Ultra low power operation
  - 5V tolerant I/O pins with 3.3V core supply
  - Advanced 0.35 micron five layer metal EEPROM process
  - Fast Zero Power™ (FZP) CMOS design technology
  - 3.3V PCI electrical specification compatible outputs (no internal clamp diode on any input or I/O)
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 clocks available per function block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - Eight product term control terms per function block
- Fast ISP programming times
- Port Enable pin for additional I/O
- 2.7V to 3.6V supply voltage at industrial grade voltage range
- Programmable slew rate control per output
- Security bit prevents unauthorized access
- Refer to XPLA3 family data sheet (**DS012**) for architecture description

Description

The XCR3384XL is a 3.3V, 384 macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of 24 function blocks provide 9,000 usable gates. Pin-to-pin propagation delays are 7.5 ns with a maximum system frequency of 135 MHz.

TotalCMOS Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its sum of products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 1 and Table 1 showing the I_{CC} vs. Frequency of our XCR3384XL TotalCMOS CPLD (data taken with 24 resetable up/down, 16-bit counters at 3.3V, 25°C).

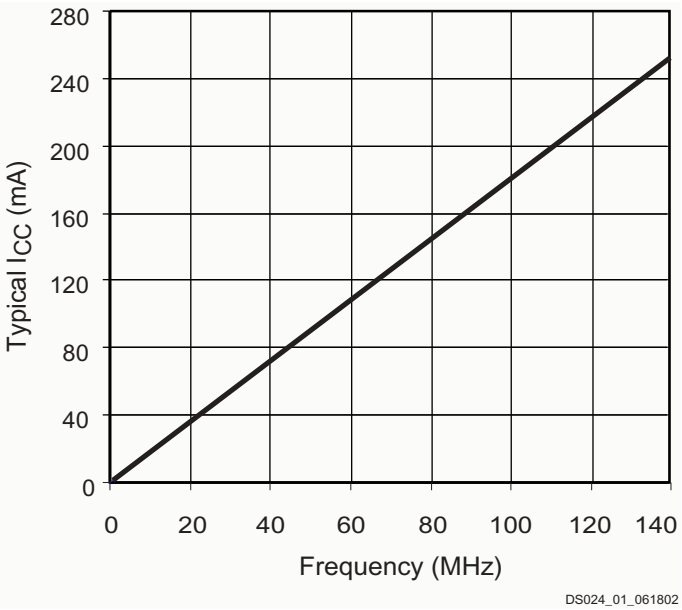


Figure 1: **XCR3384XL Typical I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C**

Table 1: **Typical I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C**

Frequency (MHz)	0	1	10	20	40	60	80	100	120	140
Typical I_{CC} (mA)	0.02	2.2	24.4	42.4	82.6	123.0	155.6	187.8	227.5	258.1

DC Electrical Characteristics Over Recommended Operating Conditions(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}(2)	Output High voltage	V_{CC} = 3.0V to 3.6V, I_{OH} = –8 mA	2.4	-	V
		V_{CC} = 2.7V to 3.0V, I_{OH} = –8 mA	2.0	-	V
		I_{OH} = –500 µA	90% V_{CC}(3)	-	V
V_{OL}	Output Low voltage	I_{OL} = 8 mA	-	0.4	V
I_{IL}	Input leakage current	V_{IN} = GND or V_{CC} to 5.5V	–10	10	µA
I_{IH}	I/O High-Z leakage current	V_{IN} = GND or V_{CC} to 5.5V	–10	10	µA
I_{CCSB}	Standby current	V_{CC} = 3.6V	-	100	µA
I_{CC}	Dynamic current(4,5)	f = 1 MHz	-	5	mA
		f = 50 MHz	-	140	mA
C_{IN}	Input pin capacitance(6)	f = 1 MHz	-	8	pF
C_{CLK}	Clock input capacitance(6)	f = 1 MHz	-	12	pF
$C_{I/O}$	I/O pin capacitance(6)	f = 1 MHz	-	10	pF

Notes:
1. See XPLA3 family data sheet (**DS012**) for recommended operating conditions
2. See Figure 2 for output drive characteristics of the XPLA3 family.
3. This parameter guaranteed by design and characterization, not by testing.
4. See Table 1, Figure 1 for typical values.
5. This parameter measured with a 16-bit, resetable up/down counter loaded into every function block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
6. Typical values, not tested.

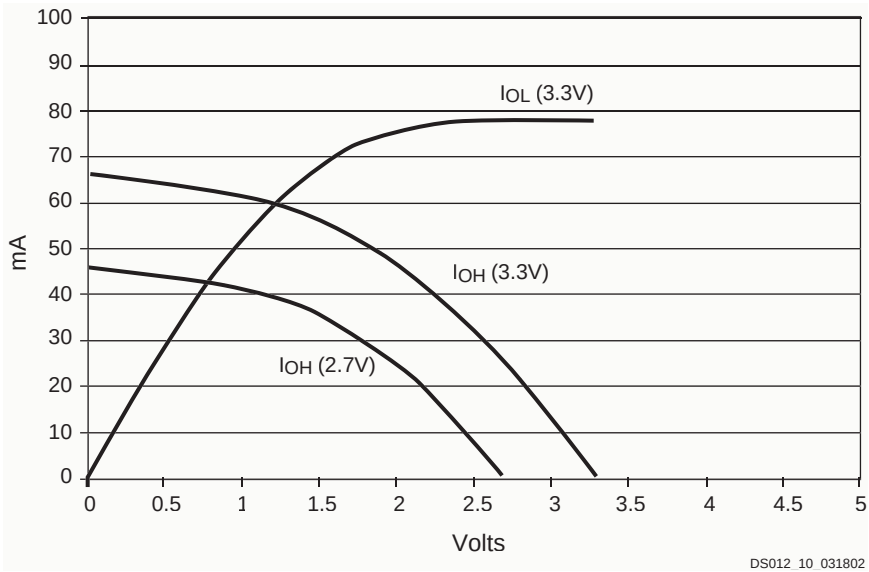


Figure 2: **Typical I/V Curve for the XPLA3 Family, 25°C**

AC Electrical Characteristics Over Recommended Operating Conditions(1,2)

Symbol	Parameter	-7		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
T_{PD1}	Propagation delay time (single p-term)	-	7.0	-	9.0	-	10.8	ns
T_{PD2}	Propagation delay time (OR array)(3)	-	7.5	-	10.0	-	12.0	ns
T_{CO}	Clock to output (global synchronous pin clock)	-	4.5	-	5.8	-	6.9	ns
T_{SUF}	Setup time(fast input register)	2.5	-	3.0	-	3.0	-	ns
T_{SU1}(4)	Setup time (single p-term)	4.3	-	5.5	-	6.7	-	ns
T_{SU2}	Setup time (OR array)	4.8	-	6.5	-	7.9	-	ns
T_H(4)	Hold time	0	-	0	-	0	-	ns
T_{WLH}(4)	Global Clock pulse width (High or Low)	3.0	-	4.0	-	5.0	-	ns
Tt_{PLH}(4)	P-term clock pulse width	4.5	-	6.0	-	7.5	-	ns
T_R(4)	Input rise time	-	20	-	20	-	20	ns
T_L(4)	Input fall time	-	20	-	20	-	20	ns
f_{SYSTEM}(4)	Maximum system frequency	-	135	-	102	-	83	MHz
T_{CONFIG}(4)	Configuration time(5)	-	200	-	200	-	200	µs
T_{INIT}(4)	ISP initialization time	-	200	-	200	-	200	µs
T_{POE}(4)	P-term OE to output enabled	-	9.0	-	11.0	-	13.0	ns
T_{POD}(4)	P-term OE to output disabled(6)	-	9.0	-	11.0	-	13.0	ns
T_{PCO}(4)	P-term clock to output	-	8.0	-	10.3	-	12.4	ns
T_{PAO}(4)	P-term set/reset to output valid	-	9.0	-	11.0	-	13.0	ns

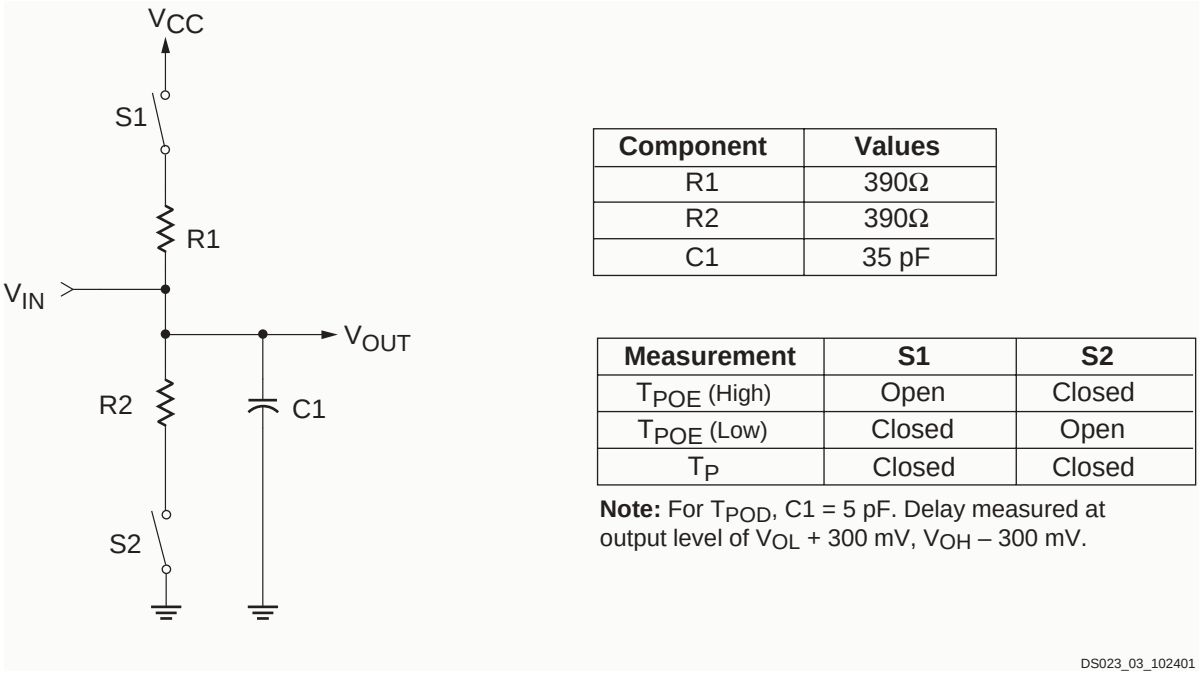
Notes:
1. Specifications measured with one output switching.
2. See XPLA3 family data sheet (**DS012**) for recommended operating conditions.
3. See Figure 4 for derating.
4. These parameters guaranteed by design and/or characterization, not testing.
5. Typical current draw during configuration is 13 mA at 3.6V.
6. Output C_L = 5 pF.

Internal Timing Parameters(1,2)

Symbol	Parameter	-7		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Buffer Delays								
T_{IN}	Input buffer delay	-	2.5	-	3.3	-	4.0	ns
T_{FIN}	Fast input buffer delay	-	2.7	-	3.3	-	3.3	ns
T_{GCK}	Global clock buffer delay	-	1.0	-	1.3	-	1.5	ns
T_{OUT}	Output buffer delay	-	2.5	-	3.2	-	3.8	ns
T_{EN}	Output buffer enable/disable delay	-	4.5	-	5.2	-	6.0	ns
Internal Register and Combinatorial Delays								
T_{LDI}	Latch transparent delay	-	1.3	-	1.6	-	2.0	ns
T_{SUI}	Register setup time	0.8	-	1.0	-	1.2	-	ns
T_{HI}	Register hold time	0.3	-	0.5	-	0.7	-	ns
T_{ECSU}	Register clock enable setup time	2.0	-	2.5	-	3.0	-	ns
T_{ECHO}	Register clock enable hold time	3.0	-	4.5	-	5.5	-	ns
T_{COI}	Register clock to output delay	-	1.0	-	1.3	-	1.6	ns
T_{AOI}	Register async. S/R to output delay	-	2.0	-	2.0	-	2.2	ns
T_{RAI}	Register async. recovery	-	5.0	-	7.0	-	8.0	ns
T_{PTCK}	Product term clock delay	-	2.0	-	2.5	-	3.0	ns
T_{LOGI1}	Internal logic delay (single p-term)	-	2.0	-	2.5	-	3.0	ns
T_{LOGI2}	Internal logic delay (PLA OR term)	-	2.5	-	3.5	-	4.2	ns
Feedback Delays								
T_F	ZIA delay	-	3.1	-	4.0	-	5.0	ns
Time Adders								
T_{LOGI3}	Fold-back NAND delay	-	2.0	-	2.5	-	3.0	ns
T_{UDA}	Universal delay	-	2.2	-	2.8	-	3.5	ns
T_{SLEW}	Slew rate limited delay	-	4.0	-	5.0	-	6.0	ns

Notes:
1. These parameters guaranteed by design and/or characterization, not testing.
2. See XPLA3 family data sheet (**DS012**) for timing model.

Switching Characteristics



Component	Values
R1	390Ω
R2	390Ω
C1	35 pF

Measurement	S1	S2
T_{POE} (High)	Open	Closed
T_{POE} (Low)	Closed	Open
T_P	Closed	Closed

Note: For T_{POD}, C1 = 5 pF. Delay measured at output level of V_{OL} + 300 mV, V_{OH} – 300 mV.

Figure 3: **AC Load Circuit**

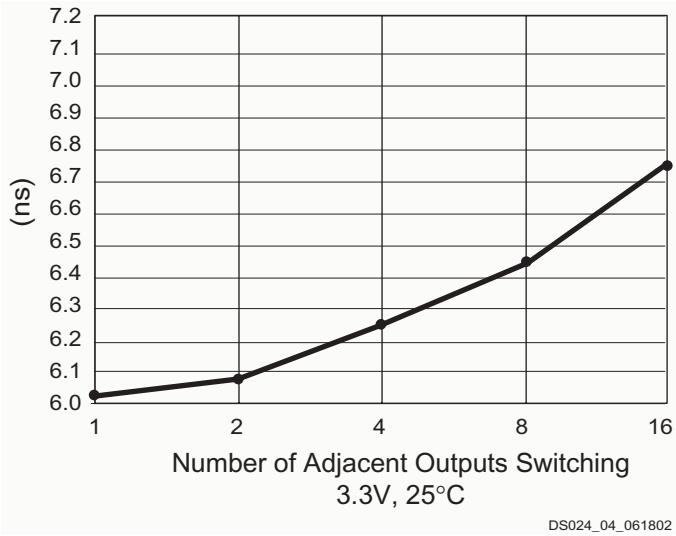
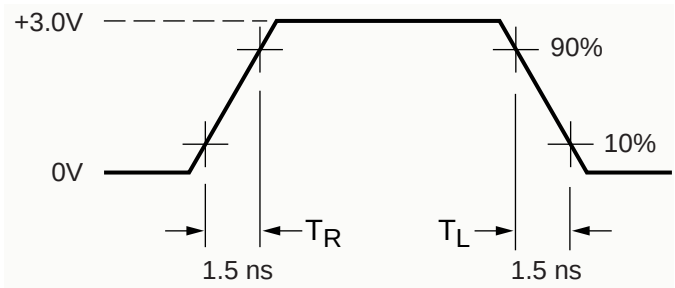


Figure 4: **Derating Curve for T_{PD2}**



Measurements:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

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Figure 5: **Voltage Waveform**

Pin Descriptions

Table 2: **XCR3384XL User I/O Pins**

	TQ144[1]	PQ208	FT256	FG324
Total User I/O Pins	118	172	212	220

Notes:
1. XCR3384XL TQ144 JTAG pins are not compatible with other members of the XPLA3 family in the TQ144 package.

Table 3: **XCR3384XL I/O Pins**

Function Block	Macro-cell	TQ144[1]	PQ208	FT256	FG324
1	1	94	-	E15	G22
1	2	-	-	F13	H20
1	3	-	13	E16	H21
1	4	-	15	F14	J19
1	5	93	16	F15	J21
1	6	-	-	-	-
1	7	-	-	-	-
1	8	-	-	-	-
1	9	-	-	-	-
1	10	-	-	-	-
1	11	-	-	-	-
1	12	-	-	-	-
1	13	92	17	G12	J22
1	14	-	18	G15	K19
1	15	-	19	G13	K21
1	16	91	20	F16	K22
2	1	-	12	E14	G21
2	2	96	11	D16	G19
2	3	97	10	F12	F22
2	4	98	9	C16	F21
2	5	99	8	E13	F20
2	6	-	-	-	-
2	7	-	-	-	-
2	8	-	-	-	-
2	9	-	-	-	-
2	10	-	-	-	-
2	11	-	-	-	-
2	12	-	-	-	-
2	13	100	-	D15	E22
2	14	101	7	D14	E21
2	15	102	6	B16	F19
2	16	103	-	C15	E20
3	1	-	21	G14	L19

Table 3: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macro-cell	TQ144[1]	PQ208	FT256	FG324
3	2	-	22	G16	L20
3	3	-	-	H13	L21
3	4	90	-	-	M20
3	5	89	24	H12	M19
3	6	-	-	-	-
3	7	-	-	-	-
3	8	-	-	-	-
3	9	-	-	-	-
3	10	-	-	-	-
3	11	-	-	-	-
3	12	-	-	-	-
3	13	-	25	H15	M22
3	14	88	26	H14	N22
3	15	-	27	H16	N21
3	16	87	28	J14	N19
4	1	104	4	A16	D22
4	2	106	3	E12	C22
4	3	107	-	-	B21
4	4	110	-	C14	B20
4	5	111	207	D13	C19
4	6	-	-	-	-
4	7	-	-	-	-
4	8	-	-	-	-
4	9	-	-	-	-
4	10	-	-	-	-
4	11	-	-	-	-
4	12	-	-	-	-
4	13	112	206	A15	B19
4	14	113	205	B15	A20
4	15	114	204	B14	C18
4	16	116	203	C13	B18
5	1	-	29	J15	P22
5	2	86[1,2]	30[2]	J13[2]	P20[2]
5	3	-	31	J16	P19
5	4	-	-	L14	R22
5	5	84	-	K15	R21
5	6	-	-	-	-
5	7	-	-	-	-
5	8	-	-	-	-
5	9	-	-	-	-
5	10	-	-	-	-
5	11	-	-	-	-

Table 3: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macro-cell	TQ144[1]	PQ208	FT256	FG324
5	12	-	-	-	-
5	13	-	33	K14	R20
5	14	83	34	K16	T22
5	15	82	35	K13	T21
5	16	81	36	L15	T20
6	1	67	62	R13	AA16
6	2	-	61	M11	Y16
6	3	-	60	T14	W16
6	4	-	59	N12	AB17
6	5	-	58	R14	AA17
6	6	-	-	-	-
6	7	-	-	-	-
6	8	-	-	-	-
6	9	-	-	-	-
6	10	-	-	-	-
6	11	-	-	-	-
6	12	-	-	-	-
6	13	-	57	P13	AB18
6	14	-	56	T15	AA18
6	15	68	-	P14	W17
6	16	69	-	T16	AA19
7	1	80	37	K12	T19
7	2	79	38	L16	U22
7	3	78	39	M15	U21
7	4	77	40	N15	U20
7	5	-	-	L13	V22
7	6	-	-	-	-
7	7	-	-	-	-
7	8	-	-	-	-
7	9	-	-	-	-
7	10	-	-	-	-
7	11	-	-	-	-
7	12	-	-	-	-
7	13	-	-	M16	U19
7	14	-	42	M14	V21
7	15	75	43	N16	V20
7	16	-	44	L12	W22
8	1	70	55	M12	Y18
8	2	71	51	R15	AA20
8	3	72	-	N13	Y19
8	4	-	-	-	AA21
8	5	-	49	P16	Y20

Table 3: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macro-cell	TQ144[1]	PQ208	FT256	FG324
8	6	-	-	-	-
8	7	-	-	-	-
8	8	-	-	-	-
8	9	-	-	-	-
8	10	-	-	-	-
8	11	-	-	-	-
8	12	-	-	-	-
8	13	-	48	N14	Y21
8	14	-	47	R16	W20
8	15	-	46	M13	W21
8	16	74	45	P15	Y22
9	1	122	187	D9	C13
9	2	-	188	A9	D13
9	3	121[1,2]	189[2]	C10[2]	B14[2]
9	4	-	190	A10	C14
9	5	120	-	D10	D14
9	6	-	-	-	-
9	7	-	-	-	-
9	8	-	-	-	-
9	9	-	-	-	-
9	10	-	-	-	-
9	11	-	-	-	-
9	12	-	-	-	-
9	13	-	-	B11	A15
9	14	-	192	C11	B15
9	15	-	193	B12	C15
9	16	-	194	E10	A16
10	1	-	178	B8	B11
10	2	-	177	D8	C11
10	3	131[1,2]	176[2]	A7[2]	D11[2]
10	4	132	175	C8	A10
10	5	-	-	-	B10
10	6	-	-	-	-
10	7	-	-	-	-
10	8	-	-	-	-
10	9	-	-	-	-
10	10	-	-	-	-
10	11	-	-	-	-
10	12	-	-	-	
10	13	-	-	C7	C10
10	14	-	173	B7	D10
10	15	133	172	D7	A9

Table 3: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macro-cell	TQ144[1]	PQ208	FT256	FG324
10	16	134	171	A6	B9
11	1	-	-	A14	A19
11	2	-	202	E11	D17
11	3	-	201	A13	A18
11	4	-	-	D12	C17
11	5	117	199	B13	B17
11	6	-	-	-	-
11	7	-	-	-	-
11	8	-	-	-	-
11	9	-	-	-	-
11	10	-	-	-	-
11	11	-	-	-	-
11	12	-	-	-	-
11	13	-	198	C12	A17
11	14	-	197	A12	D16
11	15	118	196	D11	C16
11	16	119	195	A11	B16
12	1	139	163	E6	D7
12	2	-	164	A4	C7
12	3	138	-	C5	B7
12	4	137	-	B5	A7
12	5	-	166	D6	C8
12	6	-	-	-	-
12	7	-	-	-	-
12	8	-	-	-	-
12	9	-	-	-	-
12	10	-	-	-	-
12	11	-	-	-	-
12	12	-	-	-	-
12	13	136	167	A5	B8
12	14	-	168	C6	A8
12	15	-	169	B6	D9
12	16	-	170	E7	C9
13	1	61	70	N10	W13
13	2	-	69	P11	AB14
13	3	62	68	M10	AA14
13	4	63	67	R11	Y14
13	5	-	66	T12	W14
13	6	-	-	-	-
13	7	-	-	-	-
13	8	-	-	-	-
13	9	-	-	-	-

Table 3: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macro-cell	TQ144[1]	PQ208	FT256	FG324
13	10	-	-	-	-
13	11	-	-	-	-
13	12	-	-	-	-
13	13	-	65	R12	AB15
13	14	65	64	N11	AA15
13	15	-	-	T13	Y15
13	16	66	-	P12	AB16
14	1	-	91	R6	AA8
14	2	47	92	M7	Y8
14	3	46	93	T5	AB7
14	4	-	-	T6	AA7
14	5	-	-	R5	Y7
14	6	-	-	-	-
14	7	-	-	-	-
14	8	-	-	-	-
14	9	-	-	-	-
14	10	-	-	-	-
14	11	-	-	-	-
14	12	-	-	-	-
14	13	45	95	N6	W7
14	14	44	96	T4	AB6
14	15	-	97	P5	AA6
14	16	43	98	R4	Y6
15	1	-	-	T11	Y13
15	2	-	-	-	AA13
15	3	60	71	R10	AB13
15	4	-	73	P10	W12
15	5	56	76	T10	AA12
15	6	-	-	-	-
15	7	-	-	-	-
15	8	-	-	-	-
15	9	-	-	-	-
15	10	-	-	-	-
15	11	-	-	-	-
15	12	-	-	-	-
15	13	55	77	N9	AB12
15	14	-	78	R9	Y11
15	15	-	79	P9	AA11
15	16	54	80	T9	W11
16	1	-	90	N7	AB8
16	2	48	89	T7	W9
16	3	-	88	P6	Y9

Table 3: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macro-cell	TQ144[1]	PQ208	FT256	FG324
16	4	49	87	R7	AA9
16	5	-	86	P7	AB9
16	6	-	-	-	-
16	7	-	-	-	-
16	8	-	-	-	-
16	9	-	-	-	-
16	10	-	-	-	-
16	11	-	-	-	-
16	12	-	-	-	-
16	13	-	-	T8	W10
16	14	-	-	N8	Y10
16	15	-	84	R8	AA10
16	16	53	81	P8	AB11
17	1	-	147	E4	E2
17	2	-	148	D1	F3
17	3	6	149	F5	F4
17	4	5	150	C2	D1
17	5	4	151	D3	D2
17	6	-	-	-	-
17	7	-	-	-	-
17	8	-	-	-	-
17	9	-	-	-	-
17	10	-	-	-	-
17	11	-	-	-	-
17	12	-	-	-	-
17	13	-	-	C1	E3
17	14	-	-	-	C2
17	15	2	153	B1	B2
17	16	1	154	B2	D3
18	1	7	146	D2	E1
18	2	8	145	E3	F2
18	3	9	144	E1	G4
18	4	10	-	F4	G3
18	5	-	-	F1	G2
18	6	-	-	-	-
18	7	-	-	-	-
18	8	-	-	-	-
18	9	-	-	-	-
18	10	-	-	-	-
18	11	-	-	-	-
18	12	-	-	-	-
18	13	-	142	G5	H3

Table 3: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macro-cell	TQ144[1]	PQ208	FT256	FG324
18	14	-	141	E2	H2
18	15	11	140	F3	H1
18	16	12	139	F2	J4
19	1	-	155	C3	C4
19	2	143	156	D4	B4
19	3	-	-	A2	C5
19	4	142	-	A1	B5
19	5	141	158	B3	A4
19	6	-	-	-	-
19	7	-	-	-	-
19	8	-	-	-	-
19	9	-	-	-	-
19	10	-	-	-	-
19	11	-	-	-	-
19	12	-	-	-	-
19	13	-	159	C4	D6
19	14	-	160	A3	A5
19	15	140	161	D5	C6
19	16	-	162	B4	B6
20	1	14	138	G4	J3
20	2	-	137	G1	J2
20	3	-	136	G3	K4
20	4	15	135	H1	K3
20	5	-	-	H4	K2
20	6	-	-	-	-
20	7	-	-	-	-
20	8	-	-	-	-
20	9	-	-	-	-
20	10	-	-	-	-
20	11	-	-	-	-
20	12	-	-	-	-
20	13	-	-	G2	K1
20	14	16	133	H3	L4
20	15	-	132	J1	L3
20	16	18	131	J3	L2
21	1	-	99	M6	AB5
21	2	-	100	T3	W6
21	3	42	101	N5	AB4
21	4	41	102	R3	AA5
21	5	-	103	P4	Y5
21	6	-	-	-	-
21	7	-	-	-	-

Table 3: **XCR3384XL I/O Pins *(Continued)***

Function Block	Macro-cell	TQ144[1]	PQ208	FT256	FG324
21	8	-	-	-	-
21	9	-	-	-	-
21	10	-	-	-	-
21	11	-	-	-	-
21	12	-	-	-	-
21	13	40	104	T2	AA4
21	14	39	-	-	AB3
21	15	38	-	R2	Y4
21	16	37	106	N4	AA3
22	1	19	-	H2	M2
22	2	-	130	J5	M3
22	3	20	129	J2	M4
22	4	21	128	J4	N1
22	5	22[1,2]	127[2]	K1[2]	N2[2]
22	6	-	-	-	-
22	7	-	-	-	-
22	8	-	-	-	-
22	9	-	-	-	-
22	10	-	-	-	-
22	11	-	-	-	-
22	12	-	-	-	-
22	13	23	126	K3	N3
22	14	-	-	-	N4
22	15	-	124	K2	P1
22	16	25	123	L1	P2
23	1	36	108	M5	AA2
23	2	-	109	P2	Y3
23	3	-	110	P3	Y2
23	4	-	111	T1	W3
23	5	-	-	N3	W2
23	6	-	-	-	-
23	7	-	-	-	-
23	8	-	-	-	-
23	9	-	-	-	-
23	10	-	-	-	-
23	11	-	-	-	-
23	12	-	-	-	-
23	13	-	-	R1	W1
23	14	35	112	M4	V3
23	15	-	113	P1	U4
23	16	-	114	L5	V2
24	1	26	122	K4	P3
24	2	27	121	L3	P4
24	3	28	120	K5	R1
24	4	29	119	M1	R2
24	5	30	-	L2	R3
24	6	-	-	-	-
24	7	-	-	-	-
24	8	-	-	-	-
24	9	-	-	-	-
24	10	-	-	-	-
24	11	-	-	-	-
24	12	-	-	-	-
24	13	31	118	M2	T2
24	14	32	117	L4	T3
24	15	-	-	M3	U2
24	16	34	115	N2	U3

Notes:

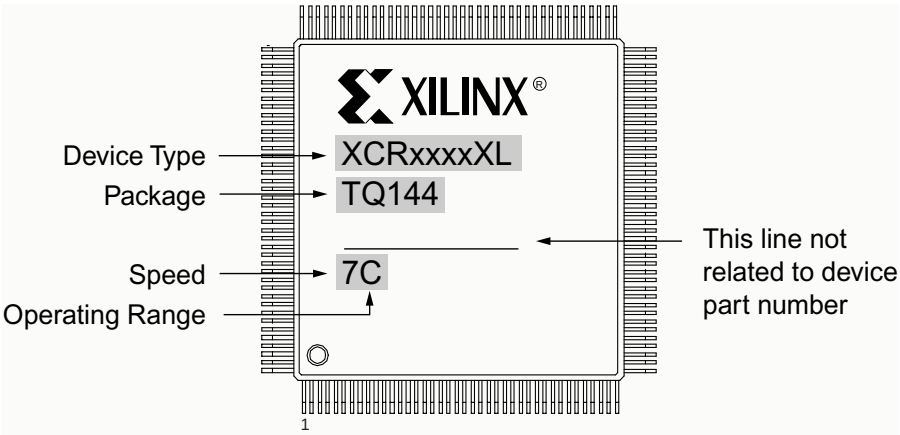
1. XCR3384XL TQ144 JTAG pins are not compatible with other members of the XPLA3 family in the TQ144 package.
2. JTAG pins.

Table 4: **XCR3384XL Global, JTAG, Port Enable, Power, and No Connect Pins**

Pin Type	TQ144(1)	PQ208	FT256	FG324
IN0 / CLK0	128	181	B9	C12
IN1 / CLK1	127	182	A8	B12
IN2 / CLK2	126	183	C9	D12
IN3 / CLK3	125	184	B10	A12
TCK	86(1)	30	J13	P20
TDI	131(1)	176	A7	D11
TDO	121(1)	189	C10	B14
TMS	22(1)	127	K1	N2
PORT_EN	33(2)	116(2)	N1(2)	T4(2)
V_{CC}	24, 50, 51, 58, 73, 76, 95, 115, 123, 130, 144	5, 23, 41, 63, 74, 83, 85, 107, 125,143, 165, 179, 186, 191	E8, E9, F7, F8, F9, F10, G6, G11, H5, H6, H11, J6, J11, J12, K6, K11, L7, L8, L9, L10, M8, M9	A11, A13, D8, D15, H4, H19, J10, J11, J12, J13, K9, K14, L9, L14, M1, M9, M14, N9, N14, N20, P10, P11, P12, P13, R4, R19, W8, W15, Y12, AB10
GND	3, 13, 17, 52, 57, 59, 64, 85, 105, 124, 129, 135,	14, 32, 50, 72, 75, 82, 94, 134, 152, 174, 180, 185, 200	E5, F6, F11, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, L6, L11	D4, D5, D18, D19, E4, E19, J9, J14, K10, K11, K12, K13, L10, L11, L12, L13, M10, M11, M12, M13, N10, N11, N12, N13, P9, P14, V4, V19, W4, W5, W18, W19
No Connects	108, 109	1, 2, 52, 53, 54, 105, 157, 208	-	A1, A2, A3, A6, A14, A21, A22, B1, B3, B13, B22, C1, C3, C20, C21, D20, D21, F1, G1, G20, H22, J1, J20, K20, L1, L22, M21, P21, T1, U1, V1, Y1, Y17, AA1, AA22, AB1, AB2, AB19, AB20, AB21, AB22

Notes:
1. XCR3384XL TQ144 JTAG pins are not compatible with other members of the XPLA3 family in the TQ144 package.
2. Port Enable is brought High to enable JTAG pins when JTAG pins are used as I/O. See family data sheet (**DS012)** for full explanation.

Device Part Marking and Ordering Combination Information



Sample package with part marking.

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XCR3384XL-7TQ144C	7.5 ns	TQ144	144-pin	Thin Quad Flat Pack (TQFP)	C
XCR3384XL-7PQ208C	7.5 ns	PQ208	208-pin	Plastic Quad Flat Pack (PQFP)	C
XCR3384XL-7FT256C	7.5 ns	FT256	256-ball	Fine-Pitch BGA (FT)	C
XCR3384XL-7FG324C	7.5 ns	FG324	324-ball	Fineline BGA Package (FG)	C
XCR3384XL-10TQ144C	10 ns	TQ144	144-pin	Thin Quad Flat Pack (TQFP)	C
XCR3384XL-10PQ208C	10 ns	PQ208	208-pin	Plastic Quad Flat Pack (PQFP)	C
XCR3384XL-10FT256C	10 ns	FT256	256-ball	Fine-Pitch BGA (FT)	C
XCR3384XL-10FG324C	10 ns	FG324	324-ball	Fineline BGA Package (FG)	C
XCR3384XL-10TQ144I	10 ns	TQ144	144-pin	Thin Quad Flat Pack (TQFP)	I
XCR3384XL-10PQ208I	10 ns	PQ208	208-pin	Plastic Quad Flat Pack (PQFP)	I
XCR3384XL-10FT256I	10 ns	FT256	256-ball	Fine-Pitch BGA (FT)	I
XCR3384XL-10FG324I	10 ns	FG324	324-ball	Fineline BGA Package (FG)	I
XCR3384XL-12TQ144C	12 ns	TQ144	144-pin	Thin Quad Flat Pack (TQFP)	C
XCR3384XL-12PQ208C	12 ns	PQ208	208-pin	Plastic Quad Flat Pack (PQFP)	C
XCR3384XL-12FT256C	12 ns	FT256	256-ball	Fine-Pitch BGA (FT)	C
XCR3384XL-12FG324C	12 ns	FG324	324-ball	Fineline BGA Package (FG)	C
XCR3384XL-12TQ144I	12 ns	TQ144	144-pin	Thin Quad Flat Pack (TQFP)	I
XCR3384XL-12PQ208I	12 ns	PQ208	208-pin	Plastic Quad Flat Pack (PQFP)	I
XCR3384XL-12FT256I	12 ns	FT256	256-ball	Fine-Pitch BGA (FT)	I
XCR3384XL-12FG324I	12 ns	FG324	324-ball	Fineline BGA Package (FG)	I

Notes:
1. C = Commercial: T_A = 0° to +70°C; I = Industrial: T_A = –40° to +85°C

Revision History

The following table shows the revision history for this document

Date	Version	Revision
02/08/01	1.0	Initial Xilinx release.
04/11/01	1.1	Update TSUF spec to meet UMC characterization data. Added Typical I/V curve, Figure 2; added Table 2: Total User I/O; changed V_{OH} spec. Added 324-ball Fineline BGA pinouts and package.
04/19/01	1.2	Updated Typical I/V curve, Figure 2: added voltage levels.
08/10/01	1.3	Updated AC Electrical Characterisitics; Internal Timing Parameters; added TQ144 package and pinouts.
01/08/02	1.4	Updated T_{SUF} spec to match software timing. Added single p-term setup time (T_{SU1}) to AC Table, renamed T_{SU} to T_{SU2} for setup time through the OR array. Updated T_{INIT} spec and T_{CONFIG} spec. Updated T_{HI} spec to correct a typo. Updated AC Load Circuit diagram to more closely resemble true test conditions, added note for T_{POD} delay measurement. Changed TQ144 pinout for pins 34 and 35.
01/06/03	1.5	Changed to Preliminary, updated AC and DC specs per characterization review. Updated Note 5 on AC Specifications from 10 mA to 13 mA at 3.6V. Updated T_{PCO} (added T_{PTCK}). Updated Ordering Information format.
07/15/03	1.6	Updated test conditions for I_{IL} and I_{IH}.
08/21/03	1.7	Updated Package Device Marking Pin 1 orientation.