A Basis for LDO and It's Thermal Design

Introduction

The AIC LDO family device, a 3-terminal regulator, can be easily used with all protection features that are expected in high performance voltage regulation application. These devices provide short-circuit protection, thermal shutdown protection and internal current limit protection against any overload condition that would create over heating junction temperature.

(1)Current Limit Protection

Like other power regulation IC, the AIC LDO family has safety protection area. The current limit protection works while outputting heavy-loading current and keeps the output current within a safe operating scope. The output voltage decreases to a lower voltage level at the same time. The AIC LDO family protection function is designed to set up output current limit when over-current happen and the downstream devices can be protected from being damaged.

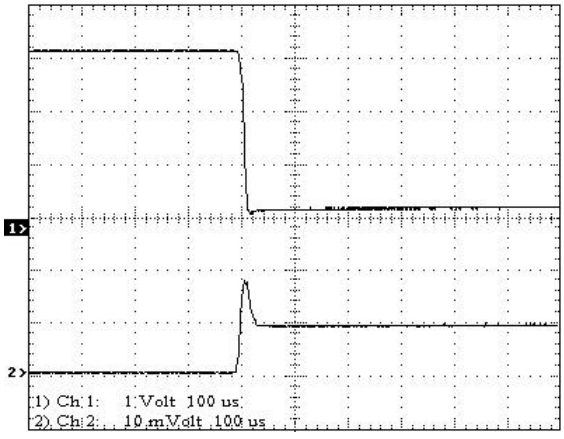

Figure 1 AIC1086 Current Limit Test

Upper: output voltage (1V/DIV)

Lower: output current (2A/DIV)

(2) Protection Diodes

During normal operation, the AIC LDO device needs no protection diode. The internal diode between input and output pins can handle microsecond surge current. Even with large output capacitance, it is very difficult to get those values of surge current in normal operation. The damage will not occur, unless the high value output capacitors and the input pin are shorted to ground instantaneously. A crowbar circuit at the input of the LDO device can generate those kinds of current and a diode from output-to-input is then recommended. Normal power supply cycling or even plugging and unplugging in the system will not generate sufficient large current to damage device (see Figure 2).

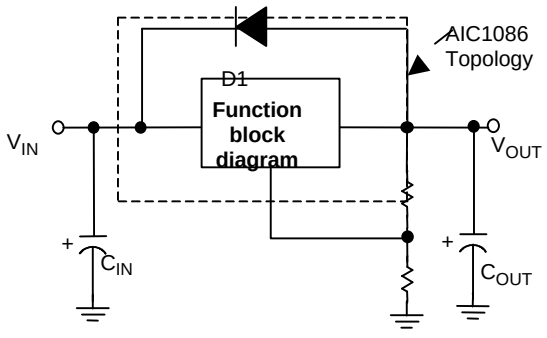

Figure 2 AIC1086 Protection Diodes Diagram

(3) Ripple Rejection

It is recommended to use the AIC LDO family

device in the application required improving ripple rejection.

By connecting a bypass capacitor from the ADJ pin to the ground can reduce the output voltage ripple significantly (see Figure3). The bypass capacitor prevents output ripple from being amplified as the output voltage or loading current increases. The function is defined by:

$$\frac{1}{2p * Fr * C_{ADJ}} \le R1$$

Here the Fr is the output ripple frequency and the C_{ADJ} is a bypass capacitor (For figure 4). The ripple rejection capability intensifies as output capacitor increases, the output ripple will then be reduced. For more information, please refer to AIC LDO family datasheet.

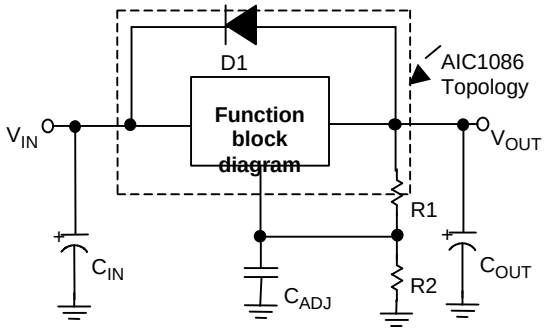

Figure 3 AIC1086 and Bypass Capacitor (C_{ADJ})

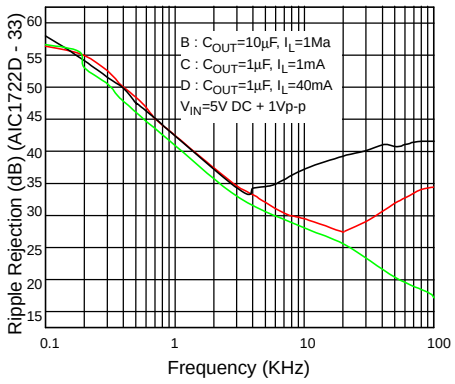

Figure 4 AIC 1722D-33 Frequency and Ripple Rejection

(4) Load Regulation

Being a three-terminal device, the AIC LDO family is unable to provide true remote load sensing. The resistance of the wire connecting the regulator to the load will limit the load regulation. Please refer to the datasheet for the detail measurement.

(a) Figure 5: When the fixed type regulator is used, the load should be connected to the output terminal on the positive side and the ground terminal on the negative side. The output voltage is measured as the following equation:

$$V_L = V_{out} - I_o(RS1 + RS2)$$

(b) Figure 6: When the adjustable type regulator is used, the load should be connected to the output terminal on the positive side and the ground terminal on the negative side. The output voltage is measured as the following equation:

$$V_L = V_{REF} \times \frac{R1 + R2}{R1} - I_o(RS1 + RS2)$$

(c) Load regulation is the circuit's ability to maintain the specified output voltage level under different load conditions, which is defined as:

$$\frac{\Delta V_{OUT}}{\Delta I_O}$$

Figure 7 shows a PMOS voltage regulator. The ratio of output voltage variation to the given load current variation ($\Delta V_{OUT}/\Delta Io$) under constant input voltage Vi can be calculated as follow.

Here, Q1 is the series pass element, and β is the current gain of Q1. Gm is the transconductance of the error amplifier at its operating point.

Assume that there is a small output current change (ΔIo), The change of output current causes the output voltage to change was calculated as:

$$\Delta V_{out} = \Delta I_o R_{EQ} (R_{EQ} = (R1 + R2) \| R_L \approx R_L)$$

Where R_{EQ} is the equivalent output resistor .The change of sensed voltage multiplied by Gm of the error amplifier input difference and β of the PMOS current gain (Figure7) must be large enough to achieve the specified change of output current. Thus,

$$\Delta Io = \beta G_M \Delta V + = \beta G_M \left(\frac{R2}{R1 + R2}\right)\Delta V_{OUT}$$

Then, the load regulator is obtained from above equation.

$$\frac{\Delta V_{OUT}}{\Delta I_o} = \frac{1}{\beta Gm}\frac{R1 + R2}{R2}$$

Since load regulation is a steady-state parameter, all frequency components are neglected. The load regulation is limited by the open loop current gain of the system. As noted from the above equation, increasing dc open loop current gain improved load regulation.

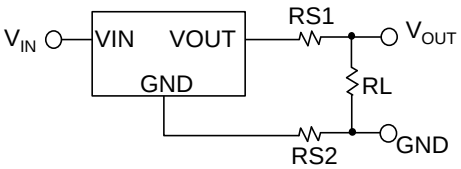

Figure 5 AIC LDO Fixed Regulator

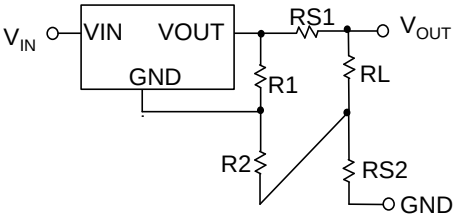

Figure 6 AIC LDO Adjustable Regulator

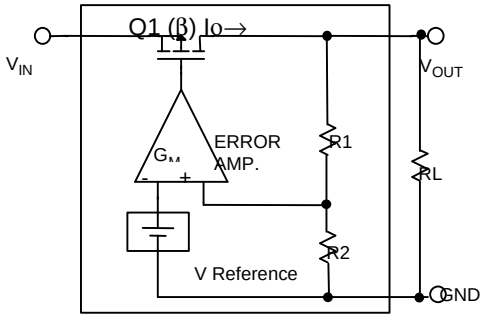

Figure 7 PMOS Voltage Regulator

(5) Quiescent Current or Ground Current

Quiescent current or ground current is the difference between input and output current for AIC LDO family. Minimum quiescent current is necessary to maximize current efficiency. It is defined:

$$I_q = I_i - I_o$$

Quiescent current consists of bias current and drive current of the series pass element, which does not contribute to output power. The series pass element, function diagram, ambient temperature, and etc, determine the value of quiescent current. Linear dropout voltage usually employ bipolar or MOS transistors as series pass elements.

(a) Figure 8 :The collector current of bipolar transistors is defined by:

$$I_C = \beta I_B$$

Where I_C is the collector current of bipolar transistor, β is the common-emitter current gain of bipolar transistor and I_B is the base current of bipolar transistor. The base current of bipolar transistor is proportional to the collector current. When the output current increases, the base current increases, too. Since the base current contributes to quiescent current, bipolar transistors have higher quiescent current than MOS transistors. At the same time, during the dropout region the quiescent current will increase, because of the additional parasitic current path between the emitter and the base of bipolar transistors, which is caused by a lower base voltage than that of the output voltage.

(b) Figure 9 the drain source current of MOS transistors is defined by:

$$I_D = K(V_{GS} - V_T)^2(1+\lambda V_{DS})(\lambda V_{DS} \approx 0)$$

$$\Rightarrow I_D = K(V_{DS} - V_T)^2$$

K is a MOS transistor conductivity parameter
Vgs is the gate to source voltage
Vt is the MOS threshold voltage

The drain current is a function of the gate to source voltage, not the gate current.

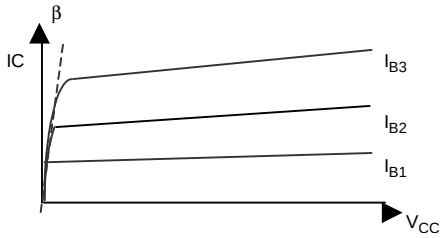

Figure 8 I-V Characteristics of Bipolar Transistors

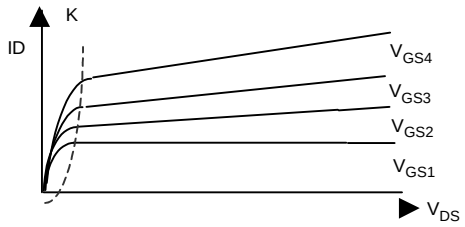

Figure 9 I-V Characteristic of MOS Transistors

For bipolar transistors, the quiescent current increases proportionally with the output current because the series pass element is a current-driven device. For MOS transistors, the quiescent current has a near constant value with respect to the load current since the device is voltage-driven. The only things that contribute to the quiescent current for MOS transistors are the biasing currents of band-gap, sampling resistor, and error amplifier. In most applications where power consumption is critical or where small bias current is requested in comparison with the output current, an LDO voltage regulator using MOS transistors is an essential choice.

Figure 10 and figure 11 show the ground current with respect to input voltage and temperature.

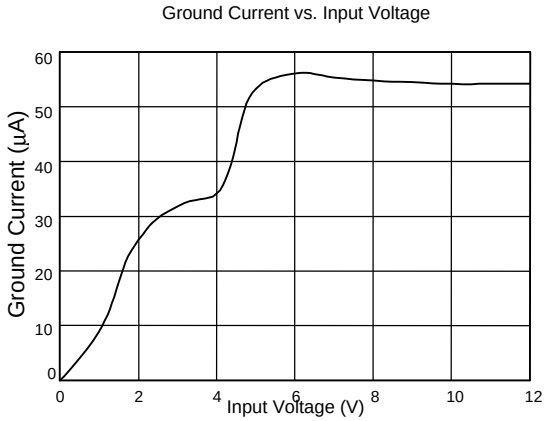

Figure 10 AIC1722 Input and Ground Current Characteristics

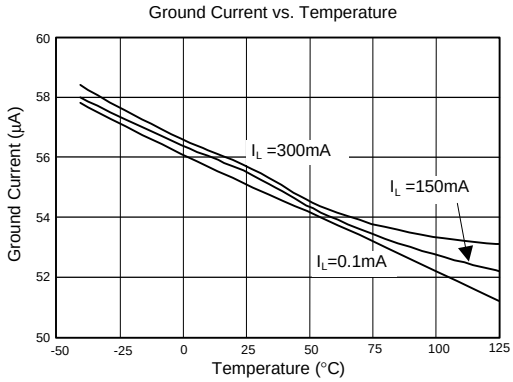

Figure 11 AIC 1722 Temperature and Ground Current Characteristics

(6) Thermal Considerations

The AIC LDO family has internal power and thermal-limiting circuitry, which is designed to protect the device against overload conditions. For continuous normal load conditions, however, maximum ratings of junction temperature must not be exceeded. It is important to pay more attention to all sources of thermal resistance from junction to ambient . This includes junction-to-case, case-to-heat sink interface, and heat sink resistance itself.

We take the following condition as an example of AIC 1086.

V_{IN} (max continuous)=5V,

V_{OUT}=3.3V,

I_{OUT}=1A ,

T_A=70ºC

$\theta_{HEAT\ SINK}$=1ºC/W,

$\theta_{CASE\text{-}TO\text{-}HEATSINK}$=0.2ºC/W for TO-220 package with thermal compound.

Power dissipation under these conditions can be calculated:

$P_D=(V_{IN}-V_{OUT})(I_{OUT})=1.7W$

Junction temperature will be equal to:

$T_J=T_A+P_D(\theta_{HEAT\ SINK}+\theta_{CASE\text{-}TO\text{-}HEAT\ SINK}+\theta_{JC})$

For the operating junction temperature range:

T_J =70ºC+1.7W(1ºC/W+0.2ºC/W+0.7ºC/W)

=73.23ºC

73.23ºC<125ºC=T_{JMAX}

(Operating Junction Temperature Range)

For the storage temperature range:

T_J =70ºC +1.7W (1ºC / W+0.2ºC / +3ºC /W)

=77.14ºC

77.14ºC<150ºC=T_{JMAX}

(Storage Temperature Range)

In the above two cases, the junction temperature are lower than the maximum rating, and this ensure a reliable operation.

(7) Efficiency

The quiescent or ground current and input/output voltage are with respect to the efficiency of a LDO regulator input/output voltage with following equation:

$$E=\frac{I_o V_o}{(I_o+I_g)V_i}\times 100\%$$

In order to achieve a higher efficiency for LDO regulator, The dropout voltage and quiescent current must be reduced. In addition, the dropout voltage between input and output must be minimized since the power dissipation of LDO regulators affects to the efficiency significantly.

Power dissipation = (Vi – Vo) Io

For example of AIC1722:

Input voltage is 5V

Output voltage is 3.3V

Output current is 300mA

Ground (max) current is 80μA

$$E=\frac{300mA\times 3.3}{(300mA+88\mu 8)\times 5}\times 100\%$$
$$=66\%$$

(8) Layout Note

According to the following parameter, we can achieve the maximum allowable Temperature Rise, (T_R)

$T_R=T_J$(max)- T_A (max)

where T_J (max) is the maximum allowable junction temperature (125ºC), and T_A (max) is the maximum ambient temperature suitable in the application. Use the calculated values for T_R and P_D, the maximum allowable value of the junction-to-ambient thermal resistance (θ_{JA}) can be calculated:

$\theta_{JA}=T_R/P_D$

If the maximum allowable value for θ_{JA} is achieved to be ≥ 133ºC /W for SOT-223 package or ≥ 74ºC /W for TO-220 package or ≥102ºC /W for TO-263 package, no heatsink is needed since the package will dissipate heat to satisfy these requirements. If the calculated value for θ_{JA} falls below these limits, extra heatsink for LDO device is required.

TABLE 1. q_{JA} Different Heatsink Area

Table 1 shows the values of the θ_{JA} of SOT-223 and TO-263 for different heatsink area. The

copper patterns that we used to measure these θ_{JA} are shown as below.

Layout	Copper Area		Thermal Resistance	
	Top Side (in^2)*	Bottom Side (in^2)*	(q_{JA} °C/W) TO-263	(q_{JA} °C/W) SOT-223
1	0.012	0	102	133
2	0.064	0	83	122
3	0.3	0	61	82
4	0.52	0	53	73
5	0.75	0	51	67
6	1	0	46	63
7	0	0.2	83	117
8	0	0.4	69	94
9	0	0.6	62	87
10	0	0.8	54	81
11	0	1	55	78
12	0.065	0.065	88	123
13	0.174	0.174	71	92
14	0.283	0.283	60	82
15	0.391	0.391	55	75
16	0.4	0.4	53	70

TABLE 2. AIC LDO Series Temperature table

(✸)➔Since IC's temperature can rise up, these operation conditions are not recommended.

Test IC TYPE：AIC1722-33CZL(TO-92) without heat sink			
Long time test: Ta: 28ºC Test time: 20min. No load: Input voltage: $5V_{DC}$ Output voltage :$3.322V_{DC}$	Power dissipation	0.5W	0.7W(✸)
	Load current	298mA	417mA
	Output voltage	3.302V	3.307V
	Package	70ºC	81ºC
Test IC TYPE：AIC1722-33CZL(SOT-89)IC stick on PCB			
Long time test Ta: 28ºC Test time: 20min. No load: Input voltage: $5V_{DC}$ Output voltage:$3.278V_{DC}$	Power dissipation	0.5W	0.6W(✸)
	Load current	290mA	348mA
	Output voltage	3.305V	3.299V
	Package	70ºC	80ºC

Test IC TYPE：AIC1723-33CE(TO-252)IC stick on PCB				
Long time test Ta: 28ºC Test time: 20min. No load : Input voltage: $5V_{DC}$ Output voltage:$3.328V_{DC}$	Power dissipation	0.5W	0.9W	1W(✸)
	Load current	300mA	538mA	598mA
	Output voltage	3.321V	3.313V	3.316V
	Package	40ºC	50ºC	57ºC
Test IC TYPE：AIC1723-33CF(TO-251) without heat sink				
Long time test Ta: 28ºC Test time: 20min. No load: Input voltage: $5V_{DC}$ Output voltage:$3.284V_{DC}$	Power Dissipation	0.9W	1W	1.1W(✸)
	Load Current	524mA	582mA	641mA
	Output Voltage	3.294V	3.295V	3.296V
	Package	63ºC	66ºC	73ºC
	Junction	80ºC	87ºC	96ºC
Test IC TYPE：AIC1084CT(TO-220) without heat sink				
Long time test Ta: 28ºC Test time: 20min. No load: Input voltage: $5V_{DC}$ Output voltage:$3.335V_{DC}$	Power Dissipation	1W	3W(✸)	6W(✸)
	Load Current	600mA	1.802A	3.604A
	Output Voltage	3.331V	3.311V	3.291V
	Package	55ºC	99ºC	127ºC
	Junction	66ºC	124ºC	176ºC
Test IC TYPE：AIC1084CT(TO-220) with heat sink				
Long time test Ta: 28ºC Test time: 20min. No load: Input voltage: $5V_{DC}$ Output voltage:$3.335V_{DC}$	Power Dissipation	1W	3W	6W(✸)
	Load Current	600mA	1.802A	3.604A
	Output Voltage	3.333V	3.322V	3.219V
	Package	47ºC	61ºC	88ºC
	Junction	54ºC	85ºC	113ºC
Test IC TYPE：AIC1084CT(TO-220) IC stick on PCB				
Long time test Ta : 28ºC Test time: 20min. No load: Input voltage: $5V_{DC}$ Output voltage:$3.335V_{DC}$	Power Dissipation	1W	3W	6W(✸)
	Load Current	600mA	1.802A	3.604A
	Output Voltage	3.333V	3.324V	3.197V
	Package	41ºC	66ºC	93ºC
	Junction	46ºC	75ºC	110ºC

Test IC TYPE：AIC1084CM(TO-263) IC stick on PCB					
Long time test Ta: 28ºC Test time: 20min. No load: Input voltage : $5V_{DC}$ Output voltage:$3.318V_{DC}$	Power Dissipation	1W	3W	6W(✸)	7W(✸)
	Load Current	594mA	1.784A	3.567A	4.162A
	Output Voltage	3.314V	3.296V	3.242V	3.077V
	Package	40ºC	74ºC	88ºC	100ºC
	Junction	44ºC	90ºC	108ºC	120ºC

Test IC TYPE：AIC1085CT(TO-220) without heat sink				
Long time test Ta: 28ºC Test time: 20min. No load: Input voltage: $5V_{DC}$ Output voltage:$3.200V_{DC}$	Power Dissipation	1W	3W(✸)	6W(✸)
	Load Current	556mA	1.667A	3.333A
	Output Voltage	3.193V	3.173V	3.285V
	Package	56ºC	90ºC	130ºC
	Junction	76ºC	146ºC	193ºC

Test IC TYPE：AIC1085CT(TO-220) with heat sink				
Long time test Ta : 28ºC Test time: 20min. No load: Input voltage: $5V_{DC}$ Output voltage:$3.200V_{DC}$	Power Dissipation	1W	3W	6W(✸)
	Load Current	556mA	1.667A	3.333A
	Output Voltage	3.192V	3.179V	3.176V
	Package	40ºC	56ºC	95ºC
	Junction	50ºC	80ºC	138ºC

Test IC TYPE：AIC1085CT(TO-220) IC stick on PCB				
Long time test Ta : 28 Test time: 20min. No load: Input voltage: $5V_{DC}$ Output voltage:$3.200V_{DC}$	Power Dissipation	1W	3W	6W(✸)
	Load Current	556mA	1.667A	3.333A
	Output Voltage	3.199V	3.192V	3.174V
	Package	45ºC	65ºC	100ºC
	Junction	54ºC	85ºC	132ºC

Test IC TYPE：AIC1085CM(TO-263) IC stick on PCB				
Long time test Ta : 28ºC Test time: 20min. No load: Input voltage: $5V_{DC}$ Output voltage:$3.322V_{DC}$	Power Dissipation	1W	3W	6W(✸)
	Load Current	595mA	1.788A	3.576A
	Output Voltage	3.321V	3.310V	3.192V
	Package	40ºC	64ºC	80ºC
	Junction	47ºC	88ºC	100ºC

Test IC TYPE：AIC1117CE(TO-252) IC stick on PCB				
Long time test Ta : 28ºC Test time: 20min. No load: Input voltage : $5V_{DC}$ Output voltage:$3.217V_{DC}$	Power Dissipation	1W	1.5W	2W(✸)
	Load Current	561mA	841mA	1.122A
	Output Voltage	3.204V	3.192V	3.184V
	Package	55ºC	68ºC	80ºC
	Junction	60ºC	70ºC	84ºC

(9) Summary

Install a 10μF (or greater) capacitor is required between the AIC LDO family device's output and ground pins for the reason of stability. Without this capacitor, the part will oscillate. Even though most types of capacitor may work, the equivalent series resistance (ESR) should be held to 5Ω or less, if aluminum electrolytic type is used. Many Aluminum electrolytic capacitors have electrolytes that will freeze under -30°C, so solid tantalums are recommended for operation below -25°C. The value of this capacitor may be increased without limit.

A 10μF (or greater) capacitor should be placed from the AIC LDO family input to ground if the lead inductance between the input and power source exceeds 500nH (approximately 10 inches of trace).