RENESAS

Data Sheet

NP20N10YDF

MOS FIELD EFFECT TRANSISTOR

R07DS0705EJ0100
Rev.1.00
Apr 17, 2012

Description

The NP20N10YDF is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
  $R_{DS(on)}$ = 55 mΩ MAX. (V_{GS} = 10 V, I_D = 10 A)
  $R_{DS(on)}$ = 68 mΩ MAX. (V_{GS} = 5 V, I_D = 10 A)
  $R_{DS(on)}$ = 74 mΩ MAX. (V_{GS} = 4.5 V, I_D = 10 A)
- Low C_{iss}: C_{iss} = 1000 pF TYP. (V_{DS} = 25 V, V_{GS} = 0 V)
- Logic level drive type
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing		Package
NP20N10YDF-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP20N10YDF-E2-AY *1			Taping (E2 type)	

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	100	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±20	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±40	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	61	W
Total Power Dissipation (T_A = 25°C) *2	P_{T2}	1.0	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Single Avalanche Current *3	I_{AS}	16	A
Single Avalanche Energy *3	E_{AS}	26	mJ

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	2.46	°C/W
Channel to Ambient Thermal Resistance *2	$R_{th(ch-A)}$	150	°C/W

Notes: *1 T_C = 25°C, $P_W \le$ 10 μs, Duty Cycle ≤ 1%
*2 Mounted on glass epoxy substrate of 40 mm × 40 mm × 1.6 mmt with 4% copper area (35 μm)
*3 $T_{ch(start)}$ = 25°C, V_{DD} = 50 V, R_G = 25 Ω, L = 100 μH, V_{GS} = 20 V → 0 V

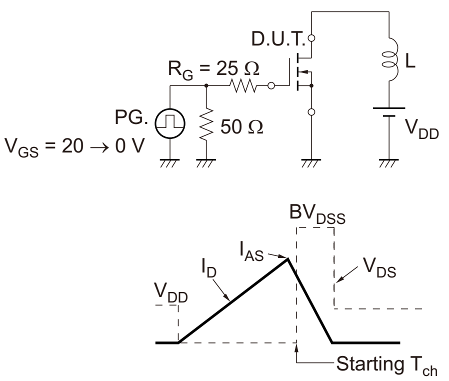
Caution: This product is an electrostatic-sensitive device due to low ESD capability and should be handled with caution for electrostatic discharge. HBM (C = 100 pF, R = 1.5 kΩ) ±700 V.

Electrical Characteristics (T_A = 25°C)

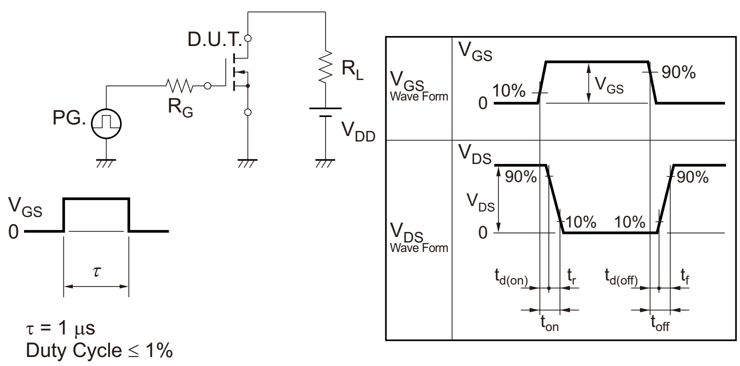
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 100 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	±100	nA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	1.5	2.0	2.5	V	V_{DS} = V_{GS}, I_D = 250 μA
Forward Transfer Admittance *1	$\lvert y_{fs} \rvert$	8	17	—	S	V_{DS} = 5 V, I_D = 10 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$	—	45	55	mΩ	V_{GS} = 10 V, I_D = 10 A
	$R_{DS(on)2}$	—	50	68	mΩ	V_{GS} = 5 V, I_D = 10 A
	$R_{DS(on)3}$	—	53	74	mΩ	V_{GS} = 4.5 V, I_D = 10 A
Input Capacitance	C_{iss}	—	1000	1500	pF	V_{DS} = 25 V V_{GS} = 0 V f = 1 MHz
Output Capacitance	C_{oss}	—	100	150	pF	
Reverse Transfer Capacitance	C_{rss}	—	50	90	pF	
Turn-on Delay Time	$t_{d(on)}$	—	13	26	ns	V_{DD} = 50 V, I_D = 10 A V_{GS} = 10 V R_G = 0 Ω
Rise Time	t_r	—	10	25	ns	
Turn-off Delay Time	$t_{d(off)}$	—	40	80	ns	
Fall Time	t_f	—	4	10	ns	
Total Gate Charge	Q_G	—	24	36	nC	V_{DD} = 80 V V_{GS} = 10 V I_D = 20 A
Gate to Source Charge	Q_{GS}	—	4	—	nC	
Gate to Drain Charge	Q_{GD}	—	7	—	nC	
Body Diode Forward Voltage *1	$V_{F(S-D)}$	—	0.92	1.5	V	I_F = 20 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}	—	56	—	ns	I_F = 20 A, V_{GS} = 0 V di/dt = 100 A/μs
Reverse Recovery Charge	Q_{rr}	—	128	—	nC	

Note: *1 Pulsed test

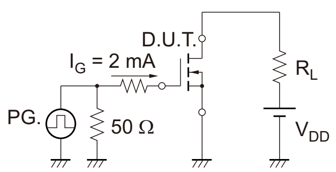
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

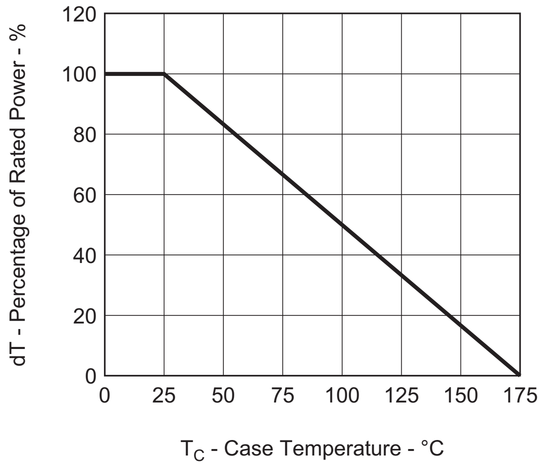


TEST CIRCUIT 3 GATE CHARGE

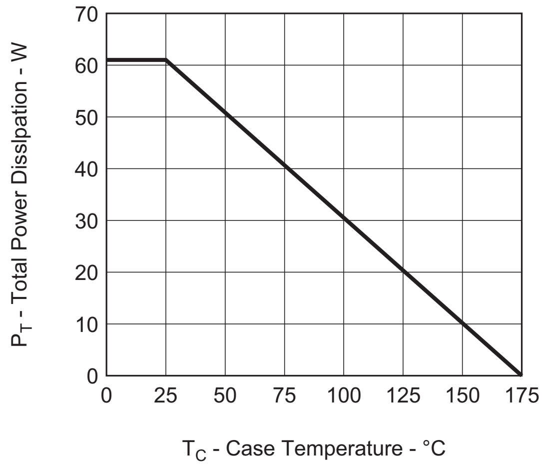


Typical Characteristics (T_A = 25°C)

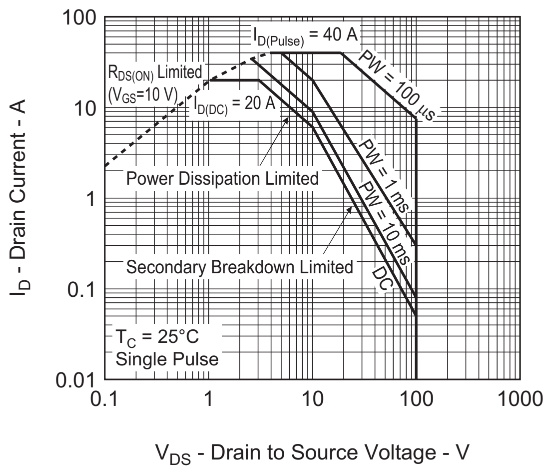
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



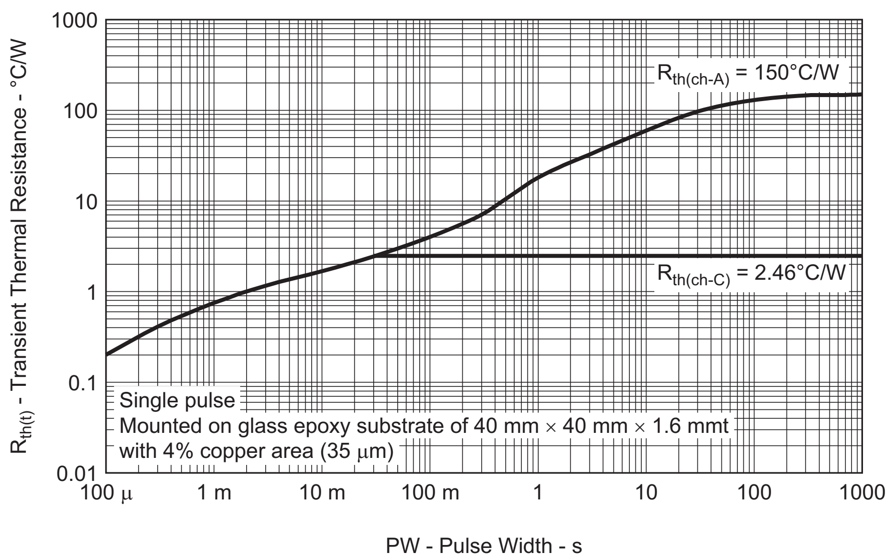
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



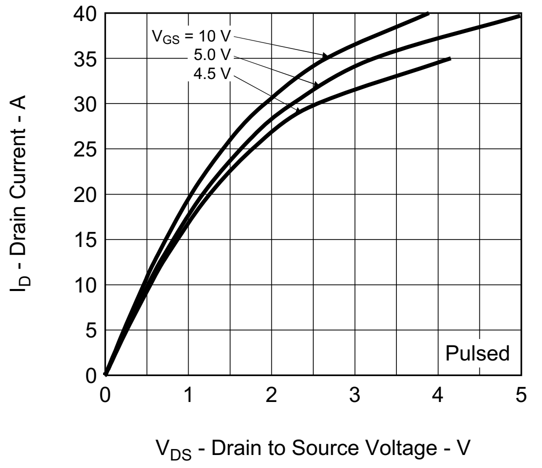
FORWARD BIAS SAFE OPERATING AREA



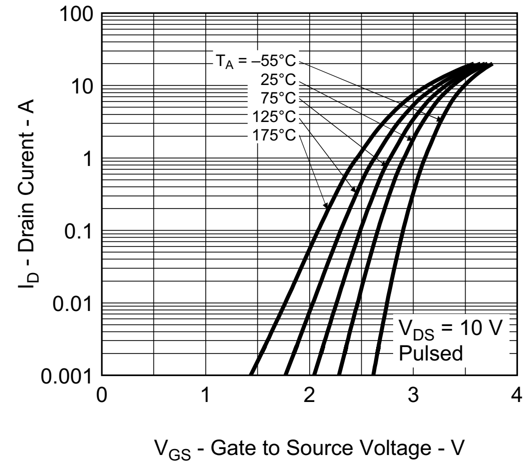
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



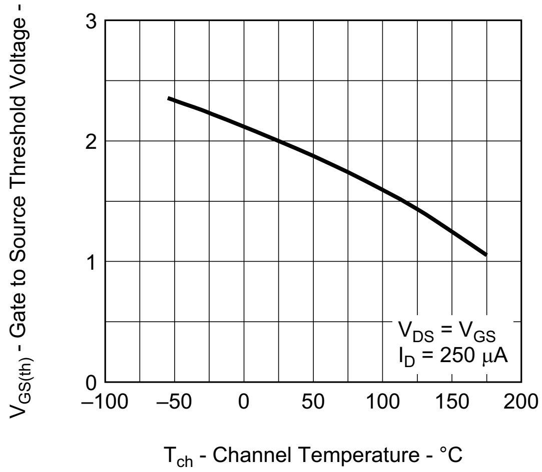
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



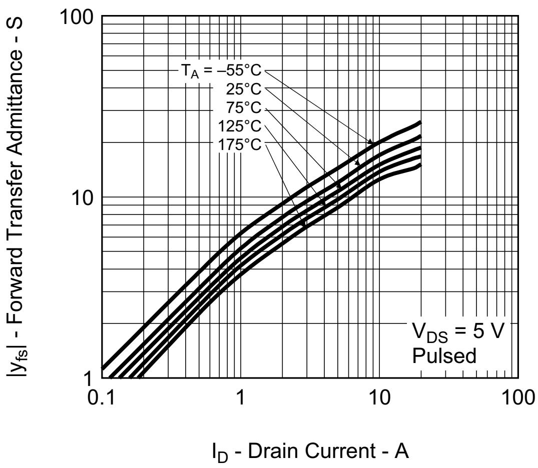
FORWARD TRANSFER CHARACTERISTICS



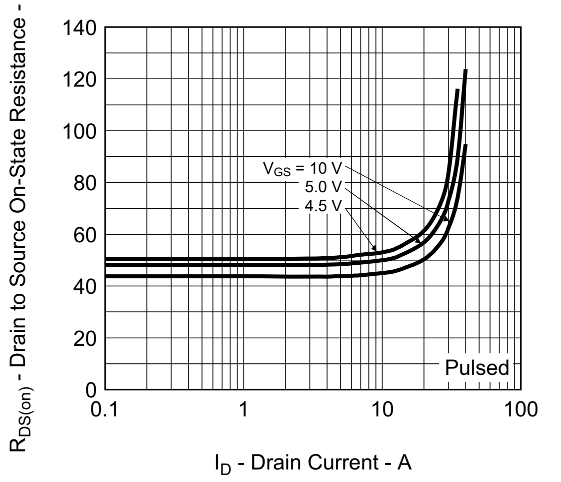
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



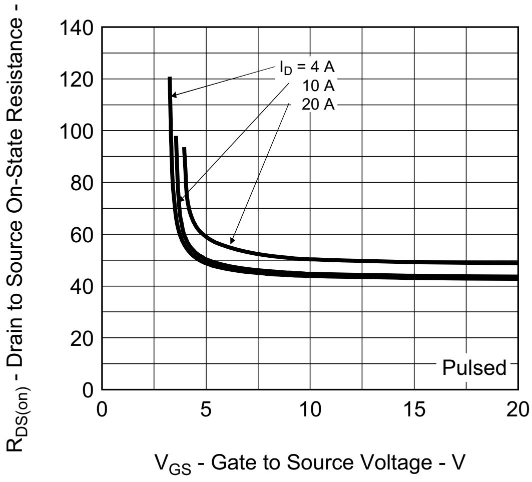
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT

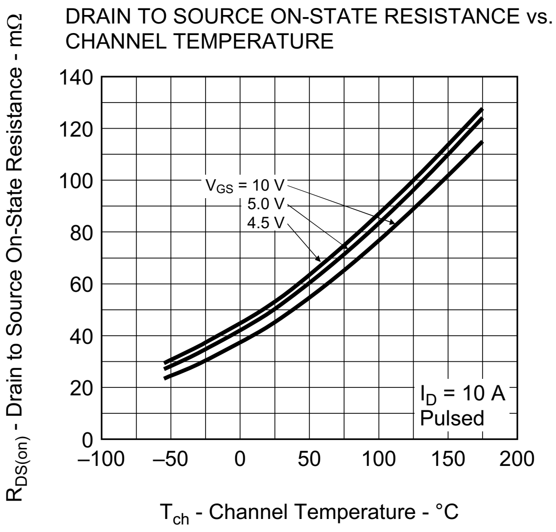


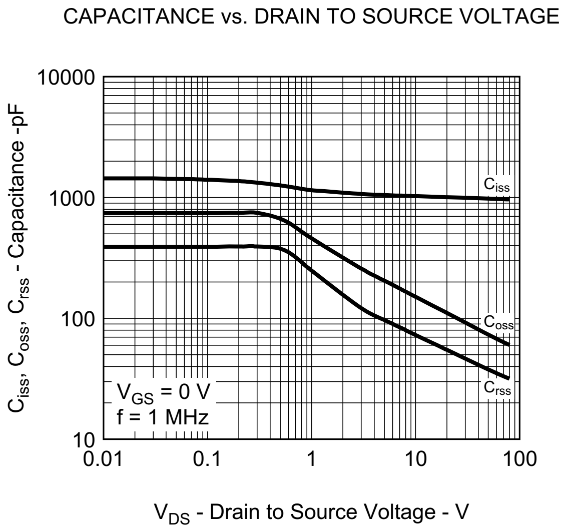
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT

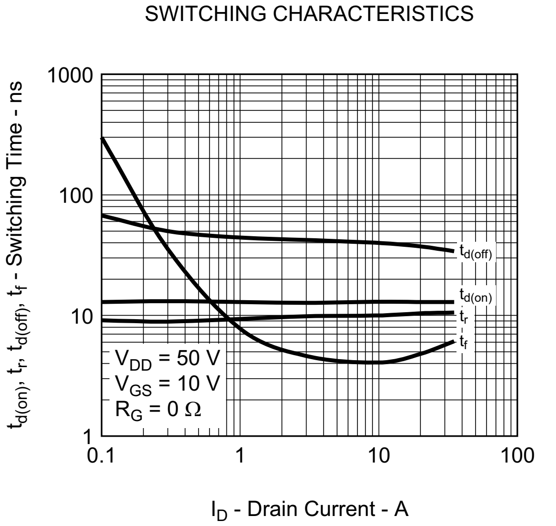


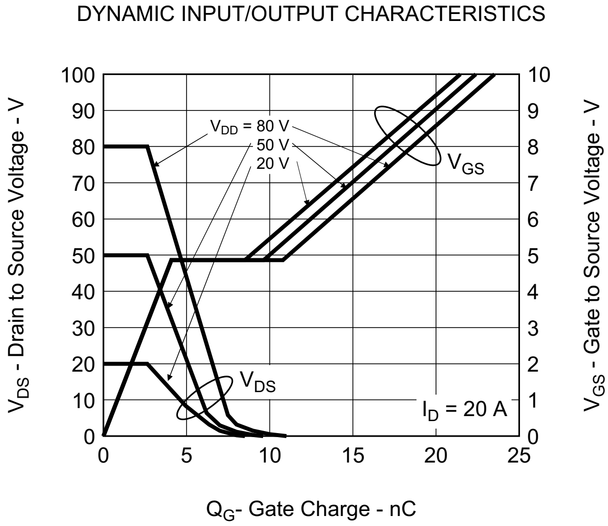
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE

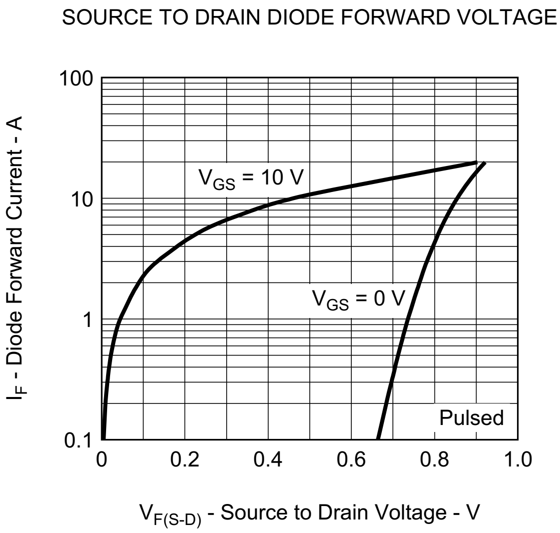


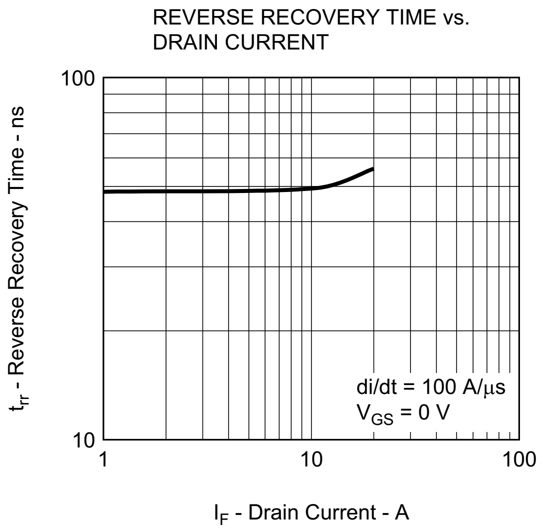

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE
$R_{DS(on)}$ - Drain to Source On-State Resistance - mΩ
V_{GS} = 10 V
5.0 V
4.5 V
I_D = 10 A
Pulsed
T_{ch} - Channel Temperature - °C


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE
C_{iss}, C_{oss}, C_{rss} - Capacitance -pF
C_{iss}
C_{oss}
C_{rss}
V_{GS} = 0 V
f = 1 MHz
V_{DS} - Drain to Source Voltage - V


SWITCHING CHARACTERISTICS
$t_{d(on)}$, t_r, $t_{d(off)}$, t_f - Switching Time - ns
$t_{d(off)}$
$t_{d(on)}$
t_r
t_f
V_{DD} = 50 V
V_{GS} = 10 V
R_G = 0 Ω
I_D - Drain Current - A

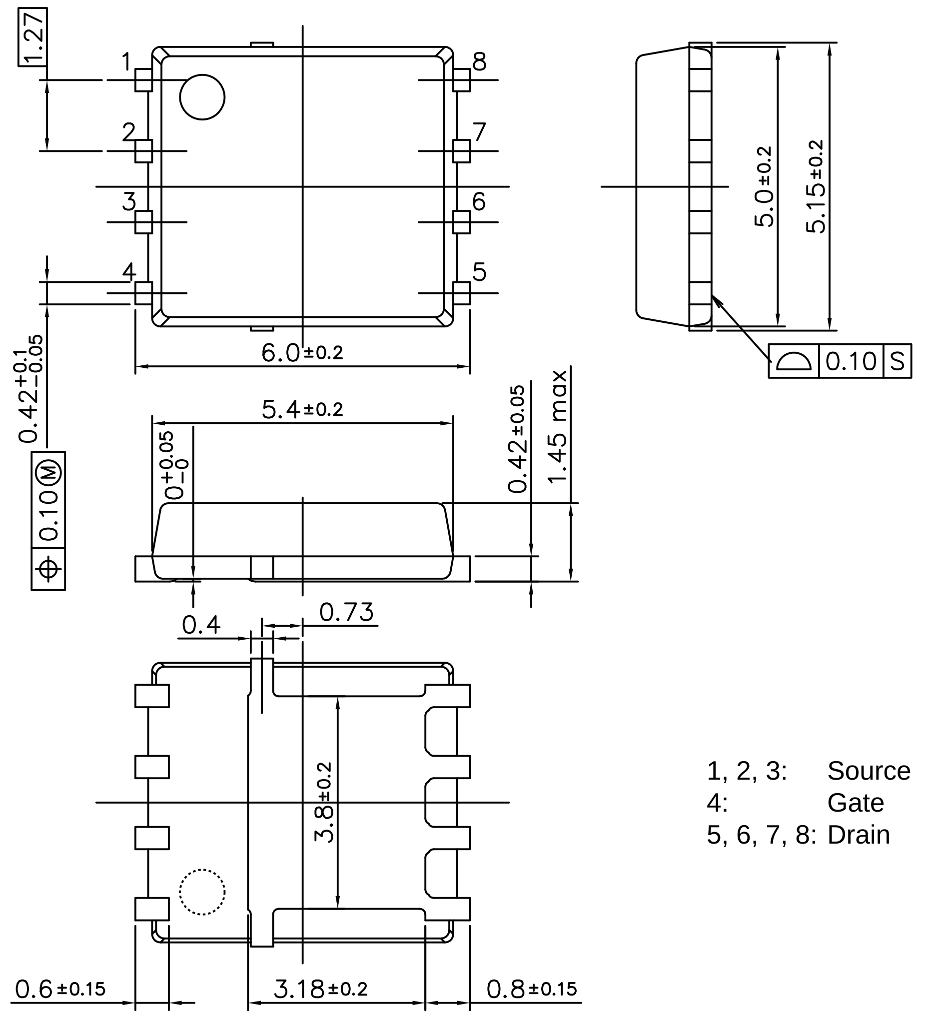

DYNAMIC INPUT/OUTPUT CHARACTERISTICS
V_{DS} - Drain to Source Voltage - V
V_{GS} - Gate to Source Voltage - V
V_{DD} = 80 V
50 V
20 V
V_{GS}
V_{DS}
I_D = 20 A
Q_G- Gate Charge - nC


SOURCE TO DRAIN DIODE FORWARD VOLTAGE
I_F - Diode Forward Current - A
V_{GS} = 10 V
V_{GS} = 0 V
Pulsed
$V_{F(S-D)}$ - Source to Drain Voltage - V

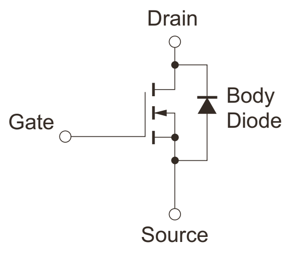

REVERSE RECOVERY TIME vs.
DRAIN CURRENT
t_{rr} - Reverse Recovery Time - ns
di/dt = 100 A/µs
V_{GS} = 0 V
I_F - Drain Current - A

Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)



Equivalent Circuit



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	**NP20N10YDF Data Sheet**

Rev.	Date	Description	
		Page	Summary
1.00	Apr 17, 2012	—	First Edition Issued

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Refer to "http://www.renesas.com/" for the latest and detailed information.

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