19-1627; Rev 3; 6/05

DBS Direct Downconverter

General Description

The MAX2106 low-cost, direct-conversion tuner IC is designed for use in digital direct-broadcast satellite (DBS) television set-top box units and is a pin-for-pin upgrade for the MAX2104. Its direct-conversion architecture reduces system cost compared to devices with IF-based architectures. The MAX2106 directly tunes L-band signals to baseband using a broadband I/Q downconverter. The operating frequency range spans 925MHz to 2175MHz.

The IC includes a low-noise amplifier (LNA) with gain control, I and Q downconverting mixers, lowpass filters with gain and frequency control, a local oscillator (LO) buffer with a 90° quadrature network, and a charge-pump-based phase-locked loop (PLL) for frequency control. The MAX2106 has an on-chip LO, requiring only an external varactor-tuned LC tank for operation. The LO's output drives the internal quadrature generator and has a buffer amplifier to drive off-chip circuitry. The MAX2106 comes in a 48-pin thin quad flat-pack package with exposed paddle (EP).

Applications

U.S. DSS Set-Top Receivers

European DVB-Compliant Systems

Cellular Base Stations

Wireless Local Loop

Broadband Systems

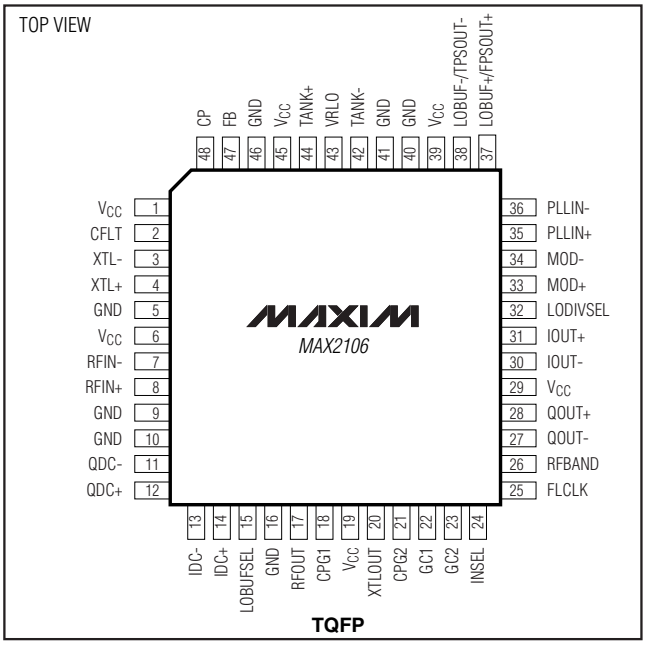
LMDS

Professional Receivers

VSAT

Microwave Links

Pin Configuration



Advantages Over MAX2104

- Improved Front End Achieves 10.2dB NF at 1550MHz
- Higher Input IIP3: 11.5dBm at 1550MHz
- Reduced Spurious Downconversion Products
- Capable of Using an External Synthesizer

Features

- **Drop-In Replacement for MAX2104 Designs Requires Only Minor Software Upgrade and Two External Resistor Value Changes**
- **Complete Low-Cost Solution for DBS Direct Downconversion**
- **High Level of Integration Minimizes Component Count**
- **1MBaud to 45MBaud Operation**
- **Selectable LO Buffer**
- **+5V Single-Supply Operation**
- **925MHz to 2175MHz Input Frequency Range**
- **On-Chip Quadrature Generator, Dual-Modulus Prescaler (/32, /33)**
- **On-Chip Crystal Oscillator Amplifier**
- **PLL Phase Detector with Gain-Controlled Charge Pump**
- **Input Levels: -25dBm to -68dBm per Carrier**
- **Over 50dB Gain Control Range**
- **Noise Figure = 10.2dB; IIP3 = +11.5dBm (at 1550MHz)**
- **Automatic Baseband Offset Correction**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2106UCM	0°C to +85°C	48 TQFP-EP*
MAX2106UCM+	0°C to +85°C	48 TQFP-EP*

*EP = *Exposed paddle.*
+Denotes lead-free package.

Functional Diagram appears at end of data sheet.

DBS Direct Downconverter

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +7V
All Other Pins to GND .....-0.3V to (V_{CC} + 0.3V)
RFIN+ to RFIN-, TANK+ to TANK-,
IDC+ to IDC-, QDC+ to QDC- .....±2V
IOUT_, QOUT_ to GND Short-Circuit Duration 10s
LOBUF+/PSOUT+, LOBUF-/PSOUT- Short-Circuit Duration..10s
Continuous Current (any pin other than V_{CC} or GND).....20mA

Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP-EP (derate 27mW/°C above +70°C) 1.5W
Operating Temperature .....0°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.25V, V_{FB} = +2.4V, $C_{IOUT\_}$ = $C_{QOUT\_}$ = 10pF, f_{FLCLK} = 2MHz, RFIN_ = unconnected, $R_{IOUT\_}$ = $R_{QOUT\_}$ = 10kΩ, $V_{LOBUFSEL}$ = 0.5V, V_{RFBAND} = V_{INSEL} = V_{CPG1} = V_{CPG2} = +2.4V, V_{PLLIN+} = V_{MOD+} = +1.3V, V_{PLLIN-} = V_{MOD-} = +1.1V, T_A = +25°C, unless otherwise noted. Typical values are at V_{CC} = +5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_{CC}		4.75		5.25	V
Operating Supply Current	I_{CC}			195	275	mA
STANDARD DIGITAL INPUTS (INSEL, CPG1, CPG2, LOBUFSEL, LODIVSEL)						
Input Voltage High	V_{IH}		2.4			V
Input Voltage Low	V_{IL}				0.5	V
Input Current	I_{IN}		-15		10	µA
RFBAND Input Current			-200		200	µA
SLEW-RATE-LIMITED DIGITAL INPUT (f_{LCLK})						
FLCLK Input Voltage High			1.85			V
FLCLK Input Voltage Low					1.45	V
FLCLK Input Current (Note 1)		R_{SOURCE} = 50kΩ, V_{FLCLK} = 1.65V	-1		1	µA
DIFFERENTIAL DIGITAL INPUTS (MOD+, MOD-, PLLIN+, PLLIN-)						
Common-Mode Input Voltage	V_{CMI}		1.08	1.2	1.32	V
Input Voltage Low		Referenced to V_{CMI}			-100	mV
Input Voltage High		Referenced to V_{CMI}	100			mV
Input Current (Note 1)			-5		5	µA
DIFFERENTIAL DIGITAL OUTPUTS (LOBUF+/PSOUT+, LOBUF-/PSOUT-)						
Common-Mode Output Voltage	V_{CMO}		2.16	2.4	2.64	V
Output Voltage Low (Note 2)		Referenced to V_{CMO}, LOBUFSEL ≤ 0.5V			-150	mV
Output Voltage High (Note 2)		Referenced to V_{CMO}, LOBUFSEL ≤ 0.5V	150			mV
FREQUENCY SYNTHESIZER/LO BUFFER						
Prescaler Ratio		(V_{MOD+} - V_{MOD-}) ≥ 200mV, LOBUFSEL ≤ 0.5V	32		32	
		(V_{MOD+} - V_{MOD-}) ≤ -200mV, LOBUFSEL ≤ 0.5V	33		33	
		LOBUFSEL ≥ 2.4V, LODIVSEL ≤ 0.5V	2		2	
		LOBUFSEL ≥ 2.4V, LODIVSEL ≥ 2.4V	1		1	
Reference Divider Ratio			8		8	
XTLOUT Output DC Voltage				1.9		V
Charge-Pump Output High Measured at FB		V_{CPG1} ≤ 0.5V, V_{CPG2} ≤ 0.5V	0.08	0.1	0.12	mA
		V_{CPG1} ≤ 0.5V, V_{CPG2} ≥ 2.4V	0.24	0.3	0.36	
		V_{CPG1} ≥ 2.4V, V_{CPG2} ≤ 0.5V	0.48	0.6	0.72	
		V_{CPG1} ≥ 2.4V, V_{CPG2} ≥ 2.4V	1.44	1.8	2.16	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.75V to +5.25V, V_{FB} = +2.4V, $C_{IOUT\_}$ = $C_{QOUT\_}$ = 10pF, f_{FLCLK} = 2MHz, RFIN_ = unconnected, $R_{IOUT\_}$ = $R_{QOUT\_}$ = 10kΩ, $V_{LOBUFSEL}$ = 0.5V, V_{RFBAND} = V_{INSEL} = V_{CPG1} = V_{CPG2} = +2.4V, V_{PLLIN+} = V_{MOD+} = +1.3V, V_{PLLIN-} = V_{MOD-} = +1.1V, T_A = +25°C, unless otherwise noted. Typical values are at V_{CC} = +5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charge-Pump Output Low Measured at FB		$V_{CPG1} \le 0.5V$, $V_{CPG2} \le 0.5V$	-0.12	-0.1	-0.08	mA
		$V_{CPG1} \le 0.5V$, $V_{CPG2} \ge 2.4V$	-0.36	-0.3	-0.24	
		$V_{CPG1} \ge 2.4V$, $V_{CPG2} \le 0.5V$	-0.72	-0.6	-0.48	
		$V_{CPG1} \ge 2.4V$, $V_{CPG2} \ge 2.4V$	-2.16	-1.8	-1.44	
Charge-Pump Output Current Matching Positive to Negative		Measured at FB	-5		5	%
Charge-Pump Output Leakage		Measured at FB	-25		25	nA
Charge-Pump Output Current Drive (Note 1)		Measured at CP	100			µA
ANALOG CONTROL INPUTS (GC1, GC2)						
Input Current	$I_{GC\_}$	$V_{GC\_}$ = 1V to 4V	-50		50	µA
BASEBAND OUTPUTS (IOUT+, IOUT-, QOUT+, QOUT-)						
Differential Output Voltage Swing		R_L = 2kΩ differential	1			Vp-p
Common-Mode Output Voltage (Note 1)			0.65		0.85	V
Offset Voltage (Note 1)			-50		50	mV

AC ELECTRICAL CHARACTERISTICS

(IC driven single-ended with RFIN- AC-terminated in 75Ω to GND, V_{CC} = +4.75V to +5.25V, $V_{IOUT\_}$ = $V_{QOUT\_}$ = 0.59Vp-p, $C_{IOUT\_}$ = $C_{QOUT\_}$ = 10pF, f_{LCLK} = 2MHz, $R_{IOUT\_}$ = $R_{QOUT\_}$ = 10kΩ, $V_{LOBUFSEL}$ = 0.5V, V_{RFBAND} = V_{INSEL} = V_{CPG1} = V_{CPG2} = +2.4V, V_{PLLIN+} = V_{MOD+} = +1.3V, V_{PLLIN-} = V_{MOD-} = +1.1V, T_A = +25°C, unless otherwise noted. Typical values are at V_{CC} = +5V.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RF FRONT END							
RFIN_ Input Frequency Range	$f_{RFIN\_}$	Inferred by quadrature gain and phase-error test		925		2175	MHz
RFIN_ Input Power for 0.59Vp-p Baseband Levels		Single carrier	V_{GC1} = V_{GC2} = +4V (min gain)	-25			dBm
			V_{GC1} = V_{GC2} = +1V (max gain)			-68	dBm
RFIN_ Input Third-Order Intercept Point (Note 3)	$IP3_{RFIN\_}$	$P_{RFIN\_}$ = -25dBm per tone	f_{LO} = 2175MHz		10.5		dBm
			f_{LO} = 1550MHz		11.5		
			f_{LO} = 950MHz		10.5		
		$P_{RFIN\_}$ = -65dBm per tone	f_{LO} = 2175MHz		-29		dBm
			f_{LO} = 1550MHz		-26		
			f_{LO} = 950MHz		-30		
RFIN_ Input Second-Order Intercept (Note 4)	$IP2_{RFIN\_}$	$P_{RFIN\_}$ = -25dBm per tone, f_{LO} = 951MHz			17		dBm
Output-Referred 1dB Compression Point (Note 5)	$P1_{dBOUT}$	$P_{RFIN\_}$ = -40dBm, signals within filter bandwidth			2		dBV
Noise Figure	NF	$f_{RFIN\_}$ = 1550MHz, V_{GC1} = 1V, V_{GC2} adjusted 0.59Vp-p baseband level	$P_{RFIN\_}$ = -65dBm		10.2		dB
			$P_{RFIN\_}$ = -25dBm		44.8		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(R_{FIN}+ IC driven single-ended with RFIN- AC-terminated in 75Ω to GND, V_{CC} = +4.75V to +5.25V, $V_{IOUT\_}$ = $V_{QOUT\_}$ = 0.59Vp-p, $C_{IOUT\_}$ = $C_{QOUT\_}$ = 10pF, f_{LCLK} = 2MHz, $R_{IOUT\_}$ = $R_{QOUT\_}$ = 10kΩ, $V_{LOBUFSEL}$ = 0.5V, V_{RFBAND} = V_{INSEL} = V_{CPG1} = V_{CPG2} = +2.4V, V_{PLLIN+} = V_{MOD+} = +1.3V, V_{PLLIN-} = V_{MOD-} = +1.1V, T_A = +25°C, unless otherwise noted. Typical values are at V_{CC} = +5V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
R_{FIN}+ Return Loss (Note 6)		$f_{RFIN\_}$ = 925MHz, Z_{SOURCE} = 75Ω		+13		dB
		$f_{RFIN\_}$ = 2175MHz, Z_{SOURCE} = 75Ω		+14		
LO 2nd Harmonic Rejection (Note 7)		Average level of $V_{IOUT\_}$, VQOUT_		32		dB
LO Half Harmonic Rejection (Note 8)		Average level of $V_{IOUT\_}$, VQOUT_		41.5		dB
LO Leakage Power (Notes 6, 9)		Measured at R_{FIN}+		-66		dBm
RFOUT PORT (LOOPTHROUGH)						
RFIN+ to RFOUT Gain (Note 10)		f = 925MHz		0.5		dB
		f = 1550MHz		1.0		
		f = 2175MHz		2.0		
RFOUT Output Third-Order Intercept Point (Note 10)		f = 925MHz		9		dBm
		f = 1550MHz		7		
		f = 2175MHz		5		
RFOUT Noise Figure (Note 10)		f = 925MHz		12.5		dB
		f = 1550MHz		11		
		f = 2175MHz		11		
RFOUT Return Loss (Notes 6, 10)		925MHz < f < 2175MHz, Z_{LOAD} = 75Ω		12		dB
BASEBAND CIRCUITS						
Output Real Impedance (Note 1)		IOUT_, QOUT_			50	Ω
Baseband Highpass -3dB Frequency (Note 1)		$C_{IDC\_}$ = $C_{QDC\_}$ = 0.22µF			750	Hz
LPF -3dB Cutoff-Frequency Range (Note 1)		Controlled by FLCLK signal	8		33	MHz
Baseband Frequency Response (Note 1)		Deviation from ideal 7th order, Butterworth, up to 0.7 × f_C	-0.5		0.5	dB
LPF -3dB Cutoff-Frequency Accuracy (Note 1)		f_{FLCLK} = 0.5MHz, f_C = 8MHz	-5.5		5.5	%
		f_{FLCLK} = 1.25MHz, f_C = 19.3MHz	-10		10	
		f_{FLCLK} = 2.0625MHz, f_C = 31.4MHz	10		10	
Ratio of In-Filter-Band to Out-of-Filter-Band Noise		f_{IN_BAND} = 100Hz to 22.5MHz, f_{OUT_BAND} = 67.5MHz to 112.5MHz		23		dB
Quadrature Gain Error		Includes effects from baseband filters, measured at 125kHz baseband			1.2	dB
Quadrature Phase Error		Includes effects from baseband filters, measured at 125kHz baseband			4	degrees

AC ELECTRICAL CHARACTERISTICS (continued)

(IC driven single-ended with RFIN- AC-terminated in 75Ω to GND, V_{CC} = +4.75V to +5.25V, $V_{IOUT\_}$ = $V_{QOUT\_}$ = 0.59Vp-p, $C_{IOUT\_}$ = $C_{QOUT\_}$ = 10pF, f_{LCLK} = 2MHz, $R_{IOUT\_}$ = $R_{QOUT\_}$ = 10kΩ, $V_{LOBUFSEL}$ = 0.5V, V_{RFBAND} = V_{INSEL} = V_{CPG1} = V_{CPG2} = +2.4V, V_{PLLIN+} = V_{MOD+} = +1.3V, V_{PLLIN-} = V_{MOD-} = +1.1V, T_A = +25°C, unless otherwise noted. Typical values are at V_{CC} = +5V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNTHESIZER						
XTLOUT Output Voltage Swing		Load = 10pF ll 10kΩ, f_{XTLOUT} = 6MHz	0.75	1	1.5	Vp-p
Crystal Frequency Range (Note 1)			4		7.26	MHz
MOD+, MOD- Setup Time (Note 1)	t_{SUM}	Figure 1	7			ns
MOD+, MOD- Hold Time (Note 1)	t_{HM}	Figure 1	0			ns
LOCAL OSCILLATOR						
LO Tuning Range (Note 11)			590		1180	MHz
LO Buffer Output Voltage (Note 1)		$V_{LOBUFSEL}$ ≥ 2.4V, f_{LO} = 925 MHz + 2175MHz	70			V_{RMS}
LO Phase Noise (Notes 6, 12)		At 1kHz offset, f_{LO} = 2175MHz		-60		dBc/Hz
		At 10kHz offset, f_{LO} = 2175MHz		-75		
		At 100kHz offset, f_{LO} = 2175MHz		-96		
RFIN+ to LO Input Isolation (Note 9)		f_{RFIN} = 2175MHz		58		dB

Note 1: Minimum and maximum values are guaranteed by design and characterization over supply voltage.
Note 2 Driving differential load of 10kΩ ll 15pF.
Note 3: Two signals are applied to RFIN_ at f_{LO} - 100MHz and f_{LO} - 199MHz. V_{GC2} = 1V, V_{GC1} is set so that the baseband outputs are at 590mVp-p. IM products are measured at baseband outputs but are referred to RF inputs.
Note 4: Two signals are applied to RFIN_ at 1200MHz and 2150MHz. V_{GC2} = 1V, V_{GC1} is set so that the baseband outputs are at 590mVp-p. IM products are measured at baseband outputs but are referred to RF inputs.
Note 5: $P_{RFIN\_}$ = -40dBm so that front-end IM contributions are minimized.
Note 6: Using L64733/L64734 demo board from LSI Logic.
Note 7: Downconverted level, in dBc, of carrier present at $f_{LO} \times 2$, f_{LO} = 1180MHz, f_{VCO} = 590MHz, V_{RFBAND} = unconnected (see histogram plots).
Note 8: Downconverted level, in dBc, of carrier present at f_O / 2, f_{LO} = 2175MHz, f_{VCO} = 1087.5MHz, V_{RFBAND} = 2.4V.
Note 9: Leakage is dominated by board parasitics.
Note 10: V_{CPG1} = V_{CPG2} = V_{RFBAND} = V_{INSEL} = 0.5V, f_{LCLK} = 0.5MHz.
Note 11: Guaranteed by design and characterization over supply and temperature.
Note 12: Measured at tuned frequency with PLL locked. PLL loop bandwidth = 3kHz. All phase noise measurements assume tank components have a Q > 50.

DBS Direct Downconverter

Pin Description

PIN	NAME	FUNCTION
1, 6, 19, 29, 39, 45	V_{CC}	V_{CC} Power-Supply Input. Connect each pin to a +5V ±5% low-noise supply. Bypass each V_{CC} pin to the nearest GND with a ceramic chip capacitor.
2	CFLT	External Bypass for Internal Bias. Bypass this pin with a 0.1µF ceramic chip capacitor to GND.
3	XTL-	Inverting Input to Crystal Oscillator. Consult crystal manufacturer for circuit loading requirements.
4	XTL+	Noninverting Input to Crystal Oscillator. Consult crystal manufacturer for circuit loading requirements.
5, 9, 10, 16, 40, 41, 46	GND	Ground. Connect each of these pins to a solid ground plane. Use multiple vias to reduce inductance where possible.
7	RFIN-	RF Inverting Input. Bypass RFIN- with 47pF capacitor in series with a 75Ω resistor to GND.
8	RFIN+	RF Noninverting Input. Connect to 75Ω source with a 47pF ceramic chip capacitor.
11	QDC-	Baseband Offset Correction. Connect a 0.22µF ceramic chip capacitor from QDC- to QDC+ (pin 12).
12	QDC+	Baseband Offset Correction. Connect a 0.22µF ceramic chip capacitor from QDC+ to QDC- (pin 11).
13	IDC-	Baseband Offset Correction. Connect a 0.22µF ceramic chip capacitor from IDC- to IDC+ (pin 14).
14	IDC+	Baseband Offset Correction. Connect a 0.22µF ceramic chip capacitor from IDC+ to IDC- (pin 13).
15	LOBUFSEL	Local Oscillator Buffer Select. Connect to GND to select DIV32/33 prescaler output; connect V_{CC} to DIV1 to select DIV2 LO buffer output.
17	RFOUT	Buffered RF Output. Enabled when INSEL is low.
18	CPG1	Charge-Pump Gain Select. High-impedance digital input. Sets the charge-pump output scaling. See *DC Electrical Characteristics* for available gain settings.
20	XTLOUT	Buffered Crystal Oscillator Output
21	CPG2	Charge-Pump Gain Select. High-impedance digital input. Sets the charge-pump output scaling. See *DC Electrical Characteristics* for available gain settings.
22	GC1	Gain Control Input for RF Front End. High-impedance analog input, with an input range of +1V to +4V. See *AC Electrical Characteristics* for transfer function.
23	GC2	Gain Control Input for Baseband Signals. High-impedance analog input, with an input range of +1V to +4V. See *AC Electrical Characteristics* for transfer function.
24	INSEL	Loopthrough Mode Enable. High-impedance digital input. Drive low to enable the RFOUT buffer and disable the LO converters. Drive high for normal tuner operation.
25	FLCLK	Baseband Filter Cutoff Adjust. Connect to a slew-rate-limited clock source. See *AC Electrical Characteristics* for transfer function.
26	RFBAND	RF Input Band Select Input. Drive high to enable 1680 MHz to 2175 MHz band. Leave unconnected to enable 1180 MHz to 1680 MHz band. Connect to GND to enable 925 MHz to 1180 MHz band.
27	QOUT-	Baseband Quadrature Output. Connect to inverting input of high-speed ADC.
28	QOUT+	Baseband Quadrature Output. Connect to noninverting input of high-speed ADC.
30	IOUT-	Baseband In-Phase Output. Connect to inverting input of high-speed ADC.
31	IOUT+	Baseband In-Phase Output. Connect to noninverting input of high-speed ADC.
32	LODIVSEL	LO Buffer Divider Ratio Input. Drive high to enable divide-by-one LO buffer output. Connect to GND to enable divide-by-two buffer output.
33	MOD+	PECL Modulus Control. A PECL high on MOD+ sets the dual-modulus prescaler to divide by 32. A PECL logic low sets the divide ratio to 33. Drive with a differential PECL signal in conjunction with MOD- (pin 34).

Pin Description (continued)

PIN	NAME	FUNCTION
34	MOD-	PECL Modulus Control. A PECL low on MOD- sets the dual-modulus prescaler to divide by 32. A PECL logic high sets the divide ratio to 33. Drive with a differential PECL signal in conjunction with MOD+ (pin 33).
35	PLLIN+	PECL Phase-Locked Loop Input. Drive with a differential PECL signal in conjunction with PLLIN- (pin 36).
36	PLLIN-	PECL Phase-Locked Loop Input. Drive with a differential PECL signal in conjunction with PLLIN+ (pin 35)
37	LOBUF+/ PSOUT+	LOBUFSEL = GND: PECL Prescaler Output. Differential output of the dual-modulus prescaler. Used in conjunction with PSOUT-. Requires PECL-compatible termination. LOBUFSEL=V_{CC}: 50Ω LO buffer noninverting output.
38	LOBUF-/ PSOUT-	LOBUFSEL = GND: PECL Prescaler Output. Differential output of the dual-modulus prescaler. Used in conjunction with PSOUT+. Requires PECL-compatible termination. LOBUFSEL = V_{CC}: 50Ω LO buffer inverting output.
42	TANK-	LO Tank Oscillator Input. Connect to an external LC tank with varactor tuning.
43	VRLO	LO Internal Regulator. Bypass with a 1000pF ceramic chip capacitor to GND.
44	TANK+	LO Tank Oscillator Input. Connect to an external LC tank with varactor tuning.
47	FB	Feedback Input for Loop Filter
48	CP	Voltage Drive Output. Control of external charge-pump transistor.

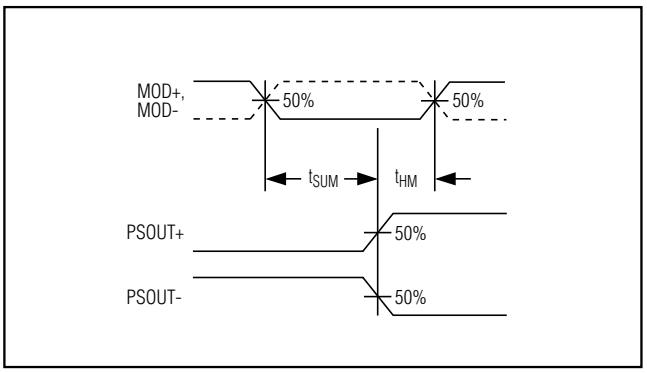
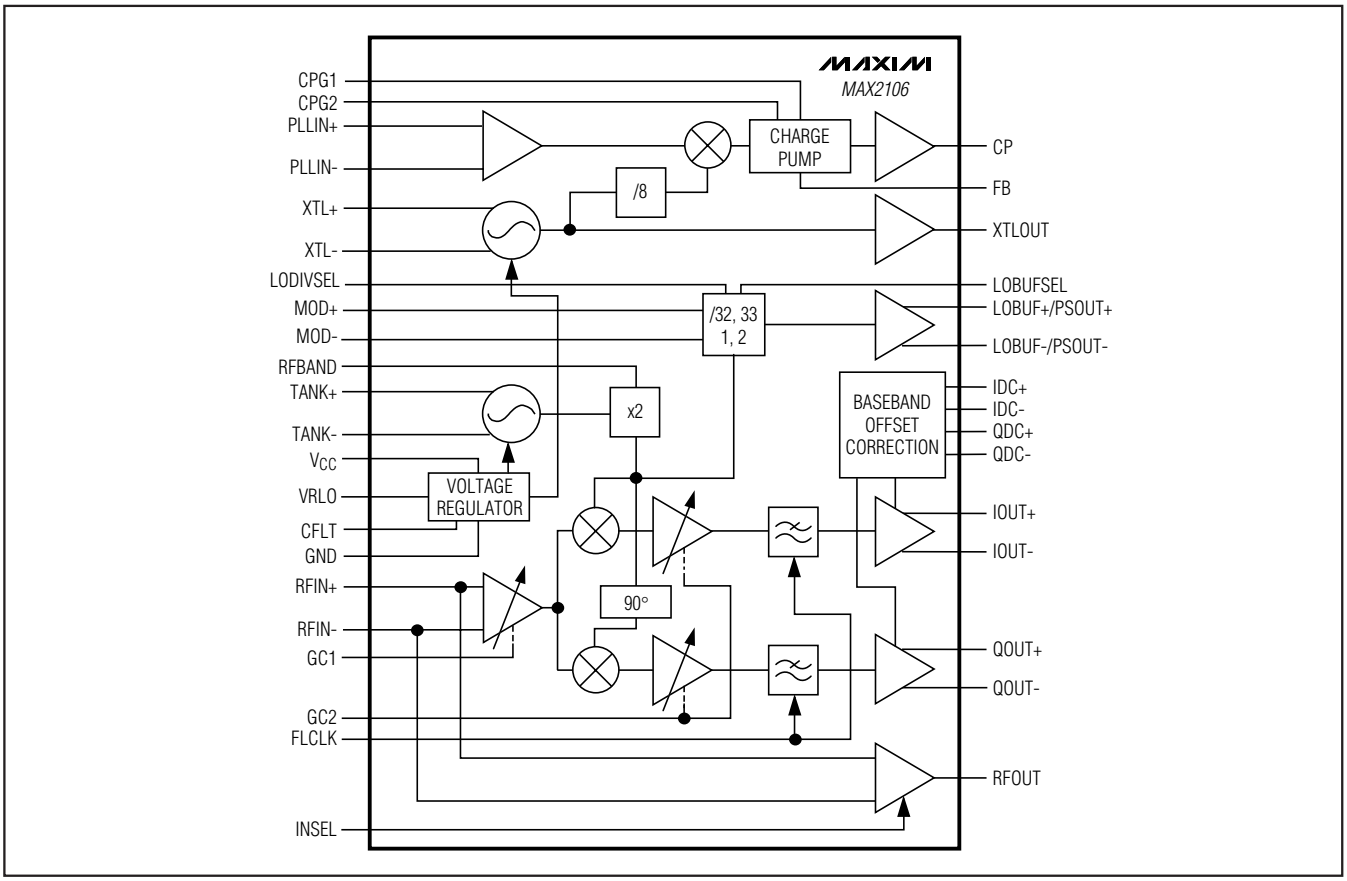


Figure 1. Modulus Control Timing Diagram

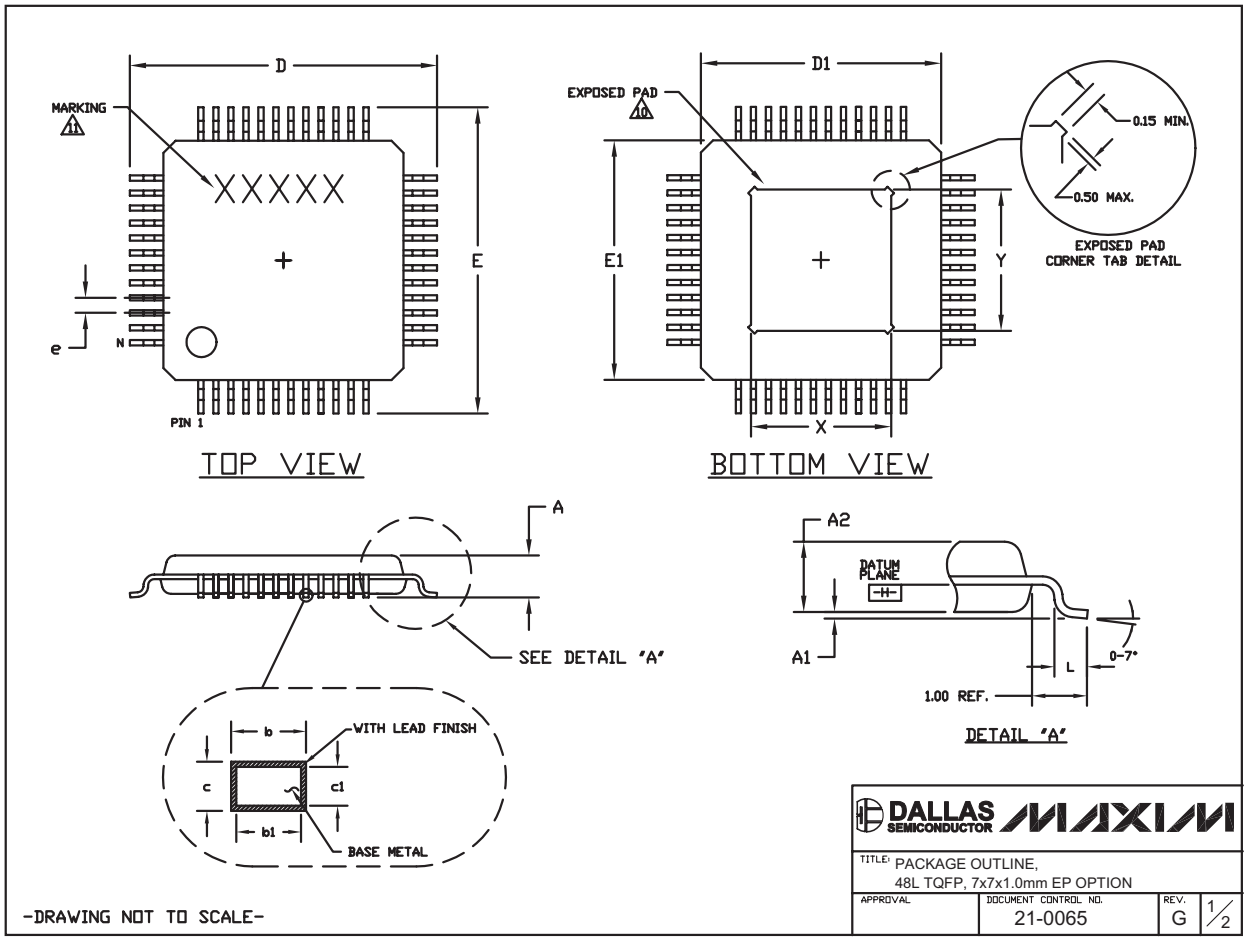
DBS Direct Downconverter

Functional Diagram



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



DBS Direct Downconverter

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE [-H-] IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATION ABA-HD.
8. LEADS SHALL BE COPLANAR WITHIN 0.08 MM.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

SYMBOL	JEDEC VARIATION ABC-HD		
	MIN.	NOM.	MAX.
A			1.20
A_1	0.05	0.10	0.15
A_2	0.95	1.00	1.05
D	8.90	9.00	9.10
D_1	6.90	7.00	7.10
E	8.90	9.00	9.10
E_1	6.90	7.00	7.10
L	0.45	0.60	0.75
N		48	
e		0.50 BSC.	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	--	0.20
c1	0.09	--	0.16

PKG. CODE	EXPOSED PAD VARIATIONS X			Y		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
C48E-7	3.70	4.00	4.30	3.70	4.00	4.30
C48E-8	4.70	5.00	5.30	4.70	5.00	5.30
C48E-10	3.70	4.00	4.30	3.70	4.00	4.30

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 48L TQFP, 7x7x1.0mm EP OPTION

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0065	G	2/2