Gate Driver Providing Galvanic isolation Series

Isolation voltage 2500Vrms
1ch Gate Driver Providing Galvanic Isolation

BM60054FV-C

General Description

The BM60054FV-C is a gate driver with isolation voltage 2500Vrms, I/O delay time of 110ns, and a minimum input pulse width of 90ns. Fault signal output function, ready signal output function, under voltage lockout (UVLO) function, short current protection (SCP) function, and switching controller function are all built-in.

Features

- Provides Galvanic Isolation
- Fault Signal Output Function
- Ready Signal Output Function
- Under Voltage Lockout Function
- Short Circuit Protection Function
- Soft Turn-Off Function for Short Circuit Protection (Adjustable Turn-OFF time)
- Thermal Protection Function
- Active Miller Clamping
- Switching Controller Function
- Output State Feedback Function
- UL1577 Recognized:File No. E356010
- AEC-Q100 Qualified(Note 1)
  (Note 1:Grade1)

Applications

- Driving IGBT Gate
- Driving MOSFET Gate

Key Specifications

- Isolation Voltage: 2500Vrms
- Maximum Gate Drive Voltage: 20V(Max)
- I/O Delay Time: 110ns(Max)
- Minimum Input Pulse Width: 90ns(Max)

Package

	W(Typ) x D(Typ) x H(Max)
SSOP-B28W	9.2 mm x 10.4 mm x 2.4 mm

Typical Application Circuit

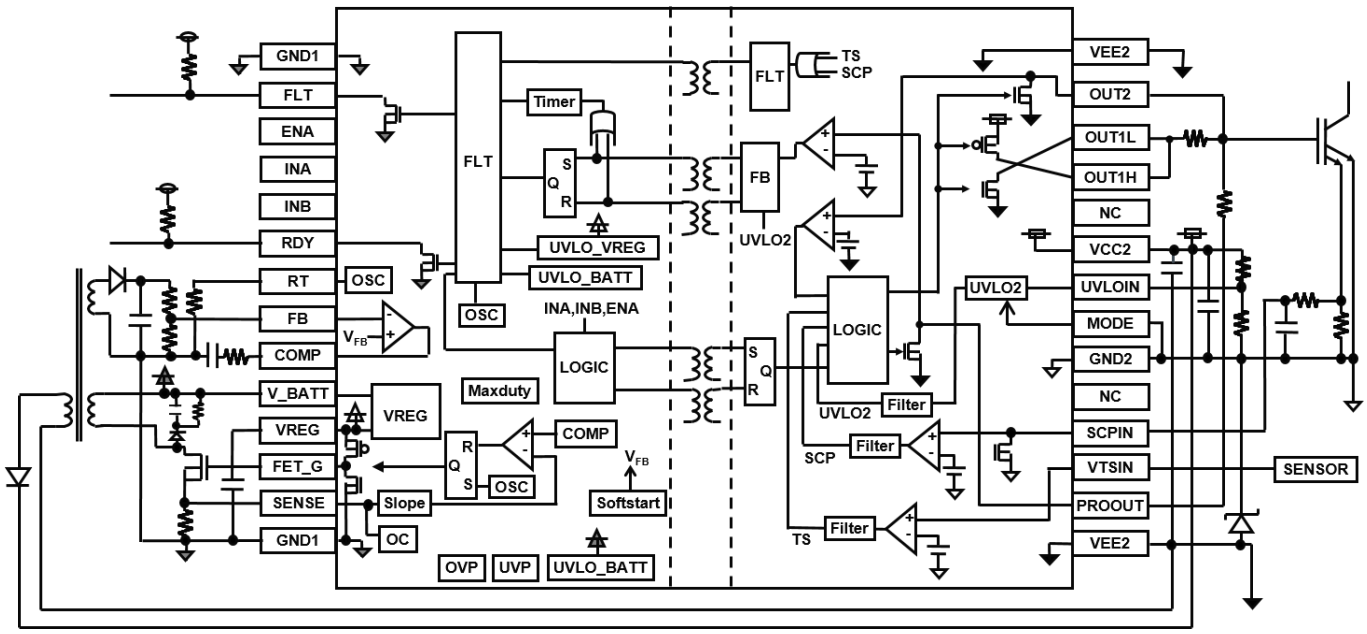


Figure 1. Typical Application Circuit

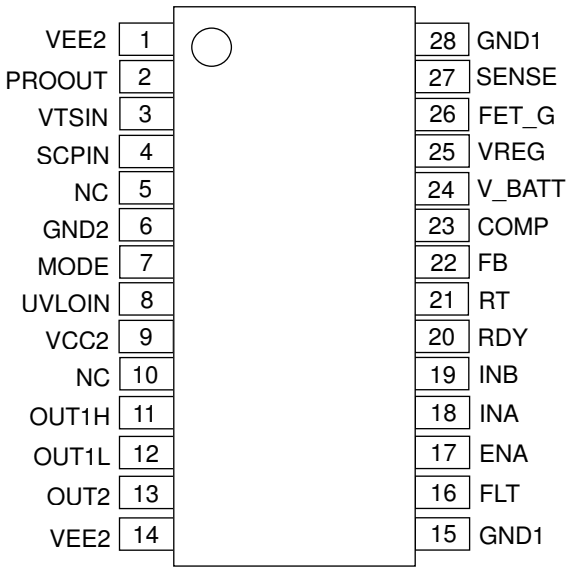
Contents

Recommended Range of External Constants

Pin Name	Symbol	Recommended Value			Unit
		Min	Typ	Max	
VREG	C_{VREG}	1.0	3.3	10.0	µF
VCC2	C_{VCC2}	0.33	-	-	µF
RT	R_{RT}	24	68	150	kΩ

Pin Configuration

(TOP VIEW)



Pin Descrlptions

	Pin Name	Pin Function
1	VEE2	Output-side negative power supply pin
2	PROOUT	Soft turn-off pin / Gate voltage input pin
3	VTSIN	Thermal detection pin
4	SCPIN	Short circuit current detection pin
5	NC	No connection
6	GND2	Output-side ground pin
7	MODE	Mode selection pin of output-side UVLO
8	UVLOIN	Output-side UVLO setting pin
9	VCC2	Output-side positive power supply pin
10	NC	No connection
11	OUT1H	Source side output pin
12	OUT1L	Sink side output pin
13	OUT2	Output pin for Miller Clamp
14	VEE2	Output-side negative power supply pin
15	GND1	Input-side ground pin
16	FLT	Fault output pin
17	ENA	Input enabling signal pin
18	INA	Control input pin A
19	INB	Control input pin B
20	RDY	Ready output pin
21	RT	Switching frequency setting pin for switching controller
22	FB	Error amplifier inverting input pin for switching controller
23	COMP	Error amplifier output pin for switching controller
24	V_BATT	Main power supply pin
25	VREG	Input-side internal power supply pin
26	FET_G	MOS FET control pin for switching controller
27	SENSE	Current detection pin for switching controller
28	GND1	Input-side ground pin

Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Main Power Supply Voltage	V_{BATT}	-0.3 to +40.0(Note 2)	V
Output-Side Positive Supply Voltage	V_{CC2}	-0.3 to +24.0(Note 3)	V
Output-Side Negative Supply Voltage	V_{EE2}	-15.0 to +0.3(Note 3)	V
Maximum Difference Between Output-Side Positive and Negative Voltages	V_{MAX2}	30.0	V
INA, INB, ENA Pin Input Voltage	V_{IN}	-0.3 to +7.0(Note 2)	V
MODE Pin Input Voltage	V_{MODE}	-0.3 to +VCC2+0.3 or +24.0(Note 3)	V
SCPIN Pin Input Voltage	V_{SCPIN}	-0.3 to +VCC2+0.3 or +24.0(Note 3)	V
VTSIN Pin Input Voltage	V_{VTS}	-0.3 to +VCC2+0.3 or +24.0(Note 3)	V
UVLOIN Pin Input Voltage	V_{UVLOIN}	-0.3 to +VCC2+0.3 or +24.0(Note 3)	V
OUT1H, OUT1L Pin Output Current (Peak 10μs)	$I_{OUT1PEAK}$	5.0(Note 4)	A
OUT2 Pin Output Current (Peak 10μs)	$I_{OUT2PEAK}$	5.0(Note 4)	A
PROOUT Pin Output Current (Peak 10μs)	$I_{PROOUTPEA}$	2.5(Note 4)	A
FLT, RDY Pin Output Current	I_{FLT}	10	mA
FET_G Pin Output Current (Peak 1μs)	I_{FET_GPEAK}	1	A
Power Dissipation	Pd	1.12(Note 5)	W
Operating Temperature Range	Topr	-40 to +125	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	+150	°C

(Note 2) Relative to GND1
(Note 3) Relative to GND2
(Note 4) Should not exceed Pd and Tj=150°C
(Note 5) Derate above Ta=25°C at a rate of 9.5mW/°C. Mounted on a glass epoxy of 70 mm × 70 mm × 1.6 mm
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Main Power Supply Voltage(Note 6)	V_{BATT}	4.0	32	V
Output-Side Positive Supply Voltage(Note 7)	V_{CC2}	10	20	V
Output-Side Negative Supply Voltage(Note 7)	V_{EE2}	-12	0	V
Maximum Difference Between Output-Side Positive and Negative Voltages	V_{MAX2}	10	28	V
Switching frequency for switching controller	f_{SWR}	100	500	kHz

(Note 6) Relative to GND1
(Note 7) Relative to GND2

Insulation Related Characteristics (UL1577)

Parameter	Symbol	Characteristic	Unit
Insulation Resistance (V_{IO}=500V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage / 1min	V_{ISO}	2500	Vrms
Insulation Test Voltage / 1sec	V_{ISO}	3000	Vrms

Electrical Characteristics

(Unless otherwise specified Ta=-40°C to +125°C, V_{BATT}=4.0V to 32V, V_{CC2}=UVLO to 20V, V_{EE2}=-12V to 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Main Power Supply Circuit Current 1	I_{BATT1}	1.1	1.6	2.1	mA	V_BATT=4.0V
Main Power Supply Circuit Current 2	I_{BATT2}	0.8	1.3	1.8	mA	V_BATT=12.0V
Main Power Supply Circuit Current 3	I_{BATT3}	0.8	1.3	1.8	mA	V_BATT=32.0V
Output Side Circuit Current 1	I_{CC21}	0.7	1.4	2.1	mA	V_{CC2}=14V, OUT1=L
Output Side Circuit Current 2	I_{CC22}	0.4	1.1	1.8	mA	V_{CC2}=14V, OUT1=H
Output Side Circuit Current 3	I_{CC23}	0.8	1.5	2.2	mA	V_{CC2}=18V, OUT1=L
Output Side Circuit Current 4	I_{CC24}	0.8	1.2	1.9	mA	V_{CC2}=18V, OUT1=H
Output Side Circuit Current 5	I_{CC25}	0.9	1.6	2.3	mA	V_{CC2}=16V, V_{EE2}=-8V, OUT1=L
Output Side Circuit Current 6	I_{CC26}	0.6	1.3	2.0	mA	V_{CC2}=16V, V_{EE2}=-8V, OUT1=H
Switching Power Supply Controller						
FET_G Output Voltage H1	V_{FETGH1}	3.8	4.0	4.2	V	4.2V<V_BATT≤32V I_{FET_G}=0A(open)
FET_G Output Voltage H2	V_{FETGH2}	-	V_BATT-0.2	V_BATT	V	V_BATT ≤ 4.2V I_{FET_G} =0A(open)
FET_G Output Voltage L	V_{FETGL}	0	-	0.3	V	I_{FET_G} =0A(open)
FET_G ON-Resistance (Source-side)	R_{ONGH}	3	6	12	Ω	10mA
FET_G ON-Resistance (Sink-side)	R_{ONGL}	0.3	0.6	1.3	Ω	10mA
Oscillation Frequency	f_{SW}	182	200	222	kHz	RT=68kΩ
Soft-start Time	t_{SS}	-	-	50	ms	
FB Pin Threshold Voltage	V_{FB}	1.47	1.50	1.53	V	
FB Pin Input Current	I_{FB}	-0.8	0	0.8	µA	
COMP Pin Sink Current	$I_{COMPSINK}$	-160	-80	-40	µA	
COMP Pin Source Current	$I_{COMPSOURCE}$	40	80	160	µA	
V_BATT UVLO ON Voltage	$V_{UVLOBATTL}$	3.20	3.40	3.60	V	
V_BATT UVLO Hysteresis	$V_{UVLOBATTHYS}$	0.07	0.1	0.13	V	
Maximum ON DUTY	D_{ONMAX}	-	48	-	%	
Over Voltage Detection Threshold	V_{OVTH}	1.60	1.65	1.70	V	
Under Voltage Detection Threshold	V_{UVTH}	1.23	1.30	1.37	V	
Over-Current Detection Threshold	V_{OCTH}	0.17	0.20	0.23	V	
Protection Holding Time	$t_{DCDCRLS}$	20	40	60	ms	
Logic Block						
Logic High Level Input Voltage	V_{INH}	2.0	-	5.5	V	INA, INB, ENA
Logic Low Level Input Voltage	V_{INL}	0	-	0.8	V	INA, INB, ENA
Logic Pull-Down Resistance	R_{IND}	25	50	100	kΩ	INA, INB, ENA
Logic Input Filtering Time	t_{INFIL}	-	-	90	ns	INA, INB
ENA Input Filtering Time	t_{ENAFIL}	-	0.5	0.8	µs	ENA
MODE Low Level Input Voltage	V_{MODEL}	0	-	$0.3\times V_{CC2}$	V	MODE, relative to GND2
MODE High Level Input Voltage	V_{MODEH}	$0.7\times V_{CC2}$	-	V_{CC2}	V	MODE,relative to GND2

Electrical Characteristics – continued

(Unless otherwise specified T_a=-40°C to +125°C, V_{BATT}=4.0V to 32V, V_{CC2}=UVLO to 20V, V_{EE2}=-12V to 0V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Output						
OUT1H ON-Resistance	R_{ONH}	0.50	0.85	1.45	Ω	I_{OUT1H}=40mA
OUT1L ON-Resistance	R_{ONL}	0.25	0.45	0.80	Ω	I_{OUT1L}=40mA
OUT1 Maximum Current	$I_{OUT1MAX}$	3.0	4.5	-	A	V_{CC2}=15V Design assurance
PROOUT ON-Resistance	R_{ONPRO}	0.45	0.85	1.55	Ω	I_{PROOUT}=40mA
Turn ON Time	t_{PONA}	45	75	105	ns	INA=PWM, INB=L
	t_{PONB}	50	80	110	ns	INA=H, INB=PWM
Turn OFF Time	t_{POFFA}	40	70	100	ns	INA=PWM, INB=L
	t_{POFFB}	35	65	95	ns	INA=H, INB=PWM
Propagation Distortion	t_{PDISTA}	-25	-5	15	ns	t_{POFFA} – t_{PONA}
	t_{PDISTB}	-35	-15	5	ns	t_{POFFB} – t_{PONB}
Rise Time	t_{RISE}	-	50	-	ns	10nF between OUT1-VEE2
Fall Time	t_{FALL}	-	50	-	ns	Design assurance
OUT2 ON-Resistance	R_{ON2}	0.25	0.45	0.80	Ω	I_{OUT2}=40mA
OUT2 ON Threshold Voltage	V_{OUT2ON}	1.8	2	2.2	V	Relative to VEE2
Common Mode Transient Immunity	CM	100	-	-	kV/μs	Design assurance
Protection Functions						
Output-side UVLO ON Threshold Voltage	$V_{UVLOINL}$	0.85	0.90	0.95	V	UVLOIN, MODE=L
Output-side UVLO Threshold Hysteresis	$V_{UVLOINHYS}$	0.10× $V_{UVLOINL}$	0.11× $V_{UVLOINL}$	0.12× $V_{UVLOINL}$	V	UVLOIN, MODE=L
Output-side UVLO ON Voltage	V_{UVLO2L}	10.9	11.5	12.1	V	VCC2, MODE=H
Output-side UVLO Hysteresis	$V_{UVLO2HYS}$	0.8	1.2	1.6	V	VCC2, MODE=H
Output-side UVLO Filtering Time	$t_{UVLO2FIL}$	0.25	1.5	3.7	μs	
DESAT Leading Edge Blanking Time	$t_{DESATleb}$	0.14	0.20	0.26	μs	Design assurance
Short Current Detection Voltage	V_{SCDET}	0.47	0.50	0.53	V	Relative to GND2
Short Current Detection Filter Time	t_{SCPFIL}	0.12	0.2	0.28	μs	
Short Current Detection Delay Time (PROOUT)	t_{SCPPRO}	0.26	0.38	0.50	μs	
SCPIN Pin Low Voltage	V_{SCPINL}	-	0.1	0.22	V	I_{SCPIN}=1mA
Output Delay Difference between PROOUT and FLT	t_{PROFLT}	0.1	0.4	0.7	μs	
Thermal Detection Voltage	V_{TSDET}	1.61	1.70	1.79	V	Relative to GND2
Thermal Detection Filter Time	t_{TSFIL}	4	10	30	μs	
Soft Turn Off Release Time	t_{STO}	30	-	110	μs	
FLT Output Low Voltage	V_{FLTL}	-	0.18	0.40	V	I_{FLT}=5mA
Gate State H Detection Threshold Voltage	V_{OSFBH}	4.5	5.0	5.5	V	Relative to GND2
Gate State L Detection Threshold Voltage	V_{OSFBL}	4.0	4.5	5.0	V	Relative to GND2
OSFB Output Filtering Time	$t_{OSFBFIL}$	1.5	2.0	2.5	μs	
RDY Output Low Voltage	V_{RDYL}	-	0.18	0.40	V	I_{RDY}=5mA

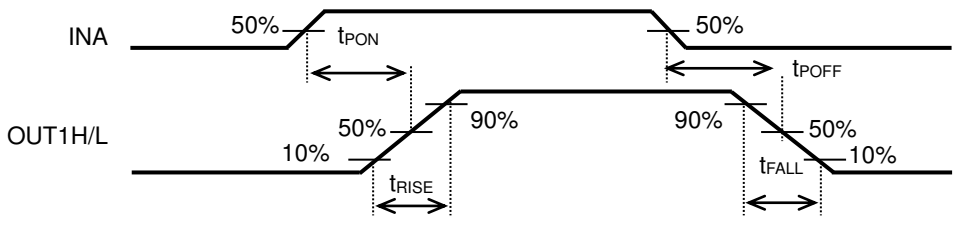


Figure 2. INA-OUT1H/L Timing Chart

UL1577 Ratings Table

Following values are described in UL Report.

Parameter	Values	Units	Conditions
Side 1 (Input Side) Circuit Current	1.3	mA	V_BATT=12V, OUT1H/L=L
Side 2 (Output Side) Circuit Current	1.6	mA	VCC2=18V, VEE2=-6V, OUT1H/L=L
Side 1 (Input Side) Consumption Power	15.6	mW	V_BATT=12V, OUT1H/L=L
Side 2 (Output Side) Consumption Power	38.4	mW	VCC2=18V, VEE2=-6V, OUT1H/L=L
Isolation Voltage	2500	Vrms	
Maximum Operating (Ambient) Temperature	125	℃	
Maximum Junction Temperature	150	℃	
Maximum Strage Temperature	150	℃	
Maximum Data Transmission Rate	5.5	MHz	

Typical Performance Curves

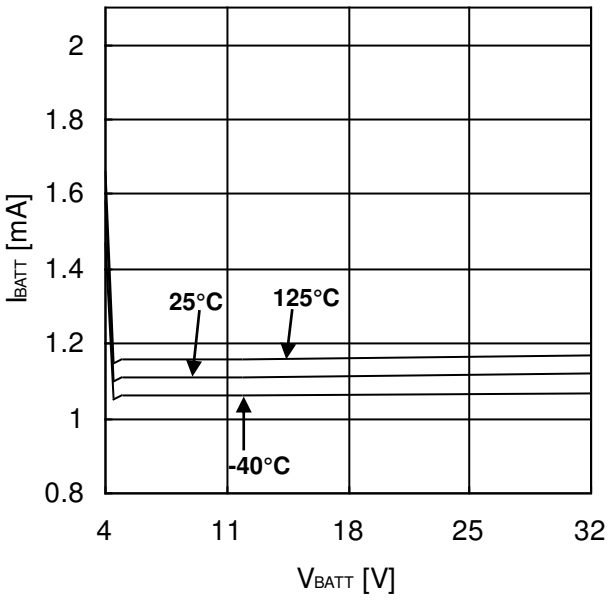


Figure 3. Main Power Supply Circuit Current

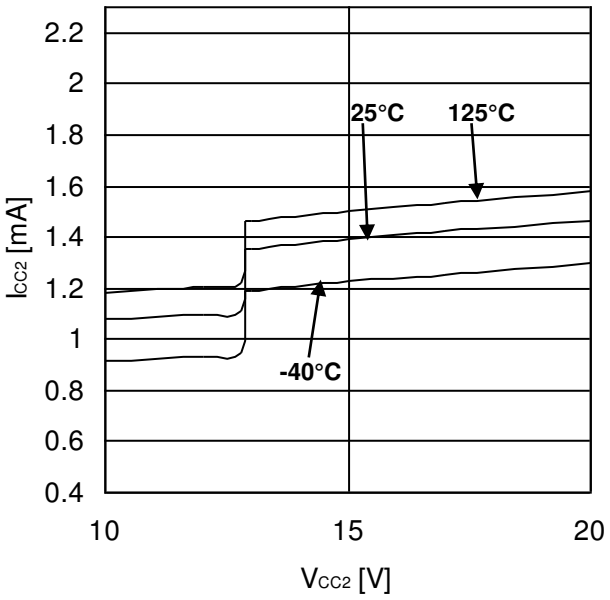


Figure 4. Output Side Circuit Current (MODE=H, VEE2=0V, OUT1=L)

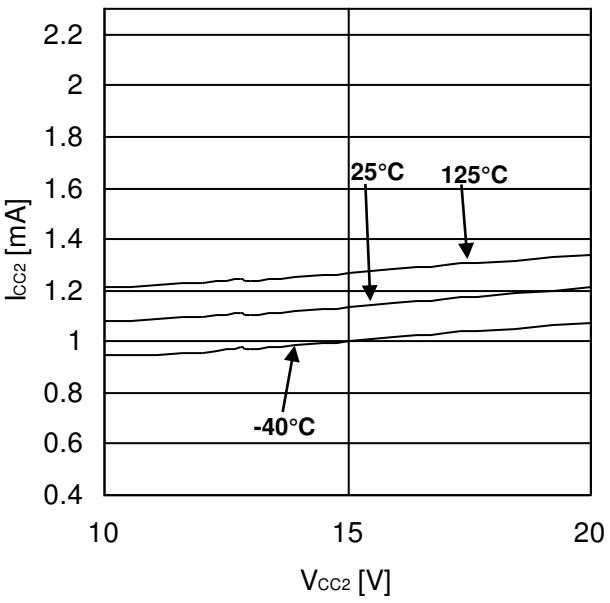


Figure 5. Output Side Circuit Current (MODE=H, VEE2=0V, OUT1=H)

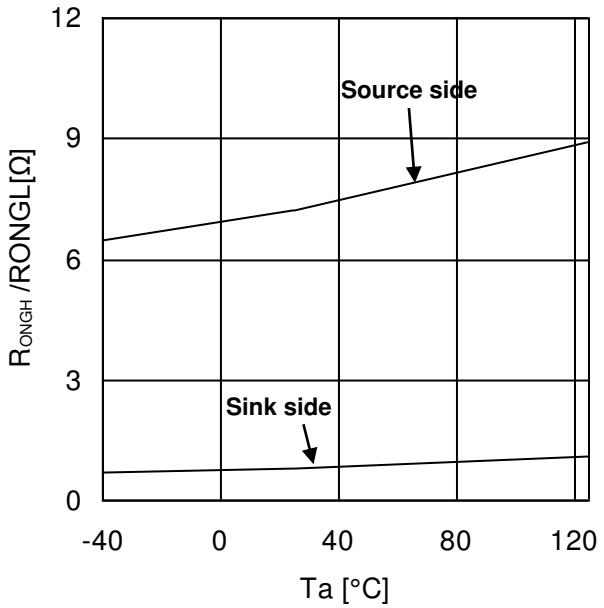


Figure 6. FET_G ON-Resistance (Source side/Sink side)

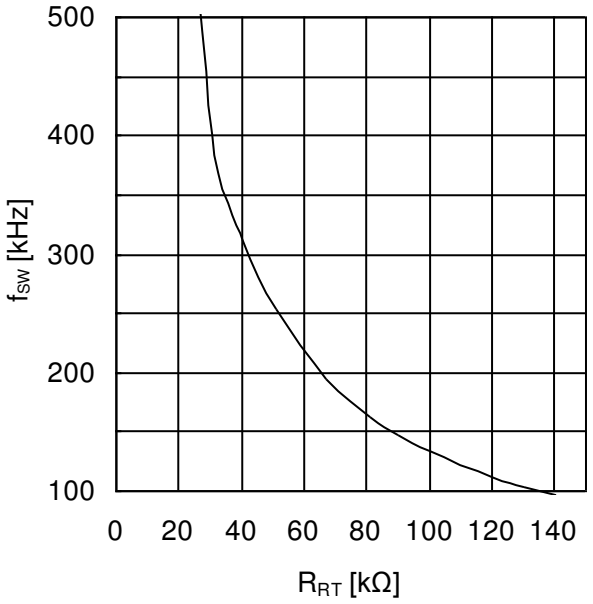


Figure 7. Oscillation Frequency

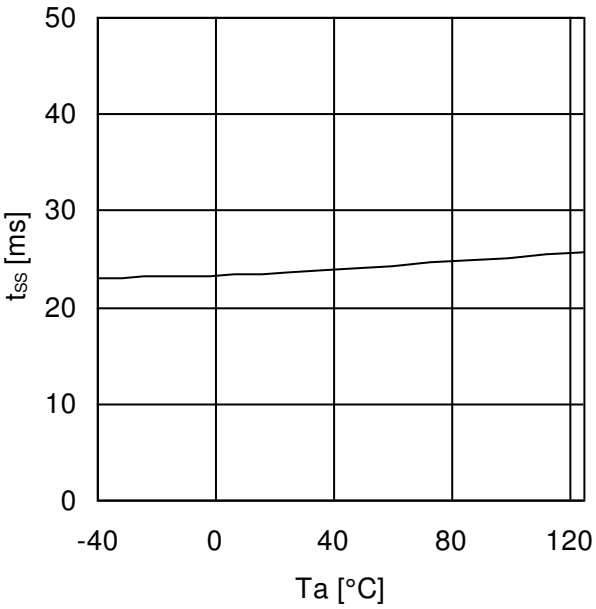


Figure 8. Soft-start Time

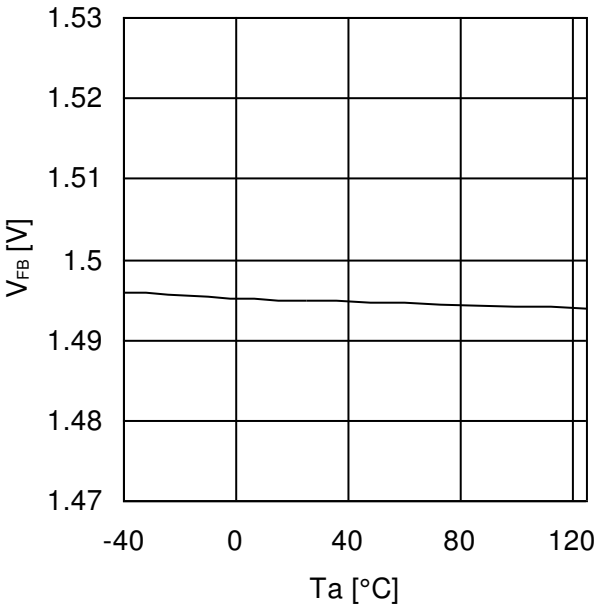


Figure 9. FB Pin Threshold Voltage

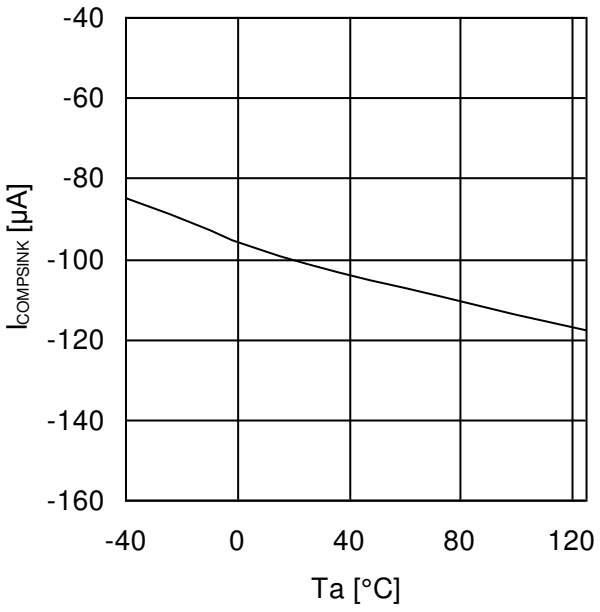


Figure 10. COMP Pin Sink Current

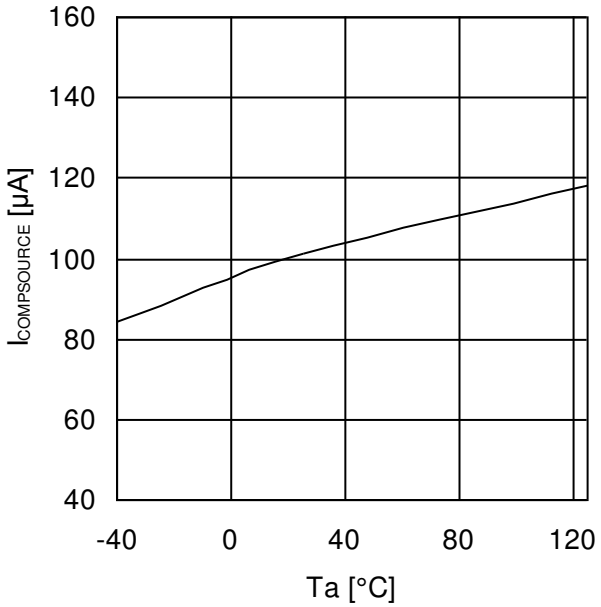


Figure 11. COMP Pin Source Current

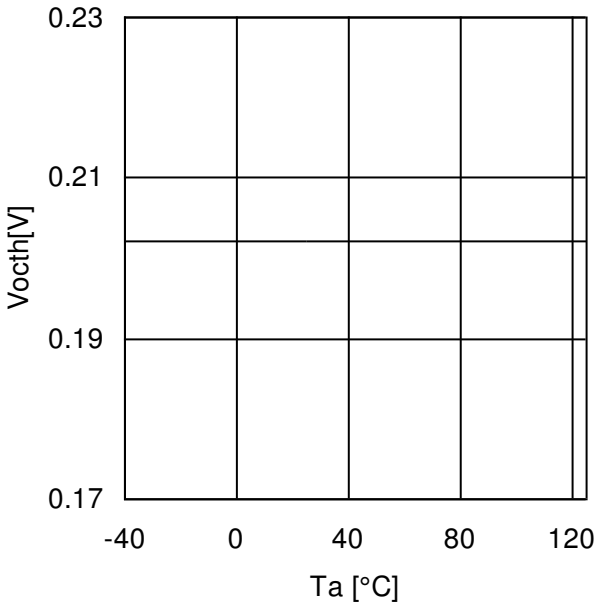


Figure 12. Over-Current Detection Threshold

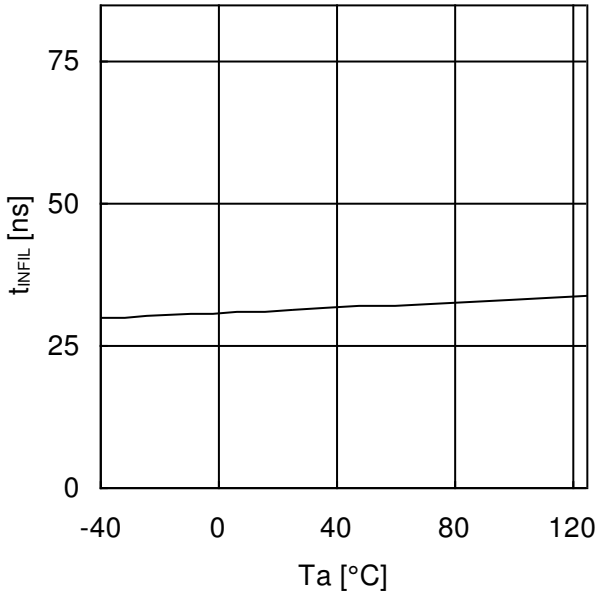


Figure 13. Logic Input Filtering Time (L pulse)

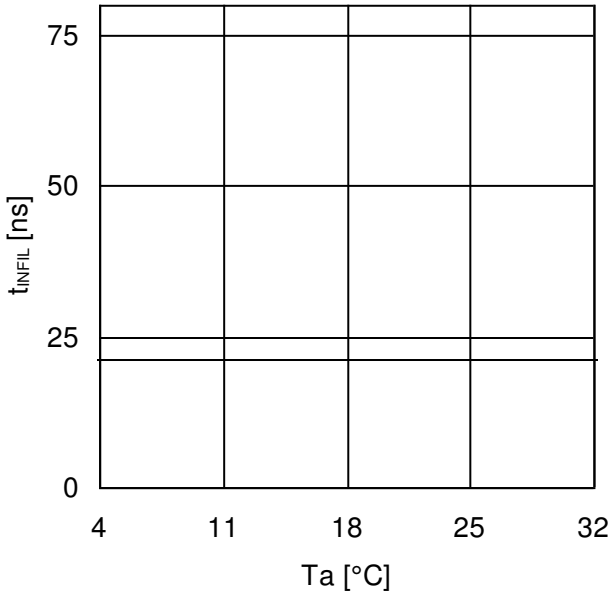


Figure 14. Logic Input Filtering Time (H pulse)

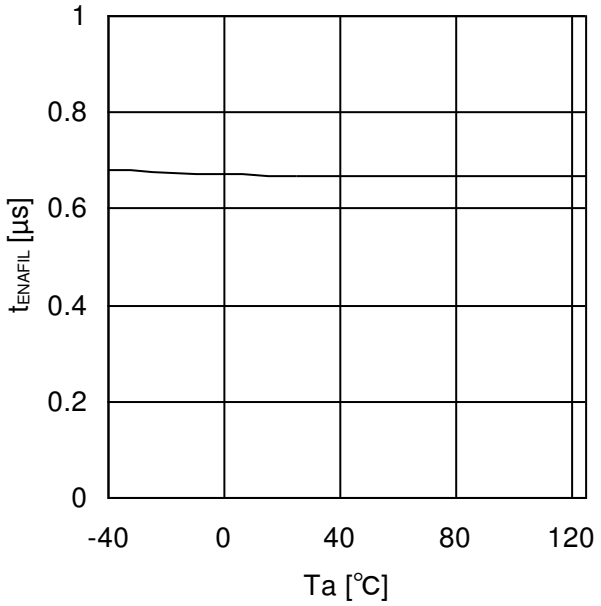


Figure 15. ENA Input Filtering Time

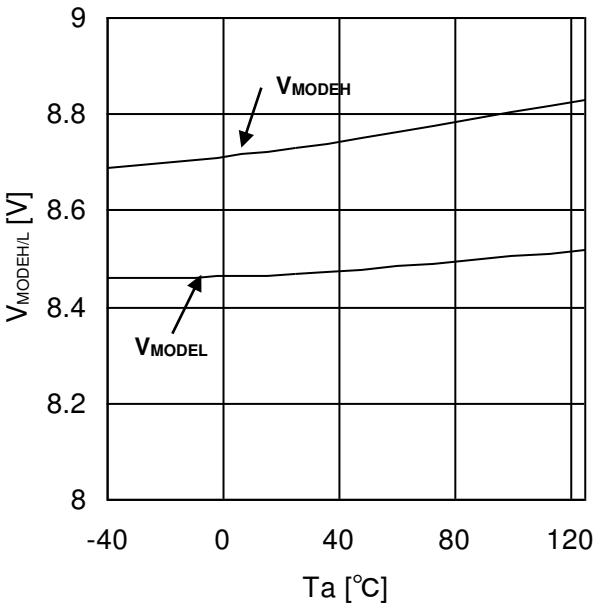


Figure 16. MODE Input Voltage H/L

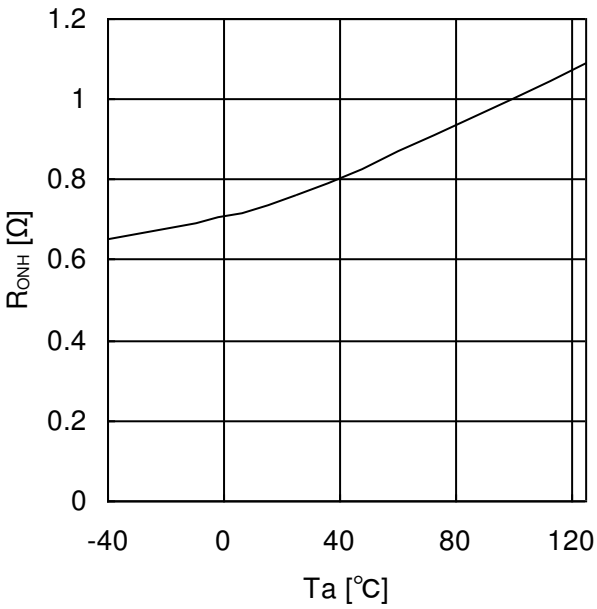


Figure 17. OUT1H ON-Resistance
(I_{OUT1}=40mA)

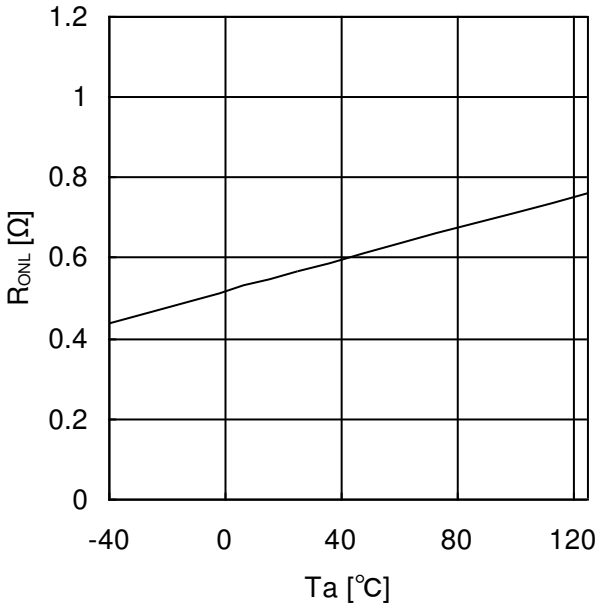


Figure 18. OUT1L ON-Resistance
(I_{OUT1}=40mA)

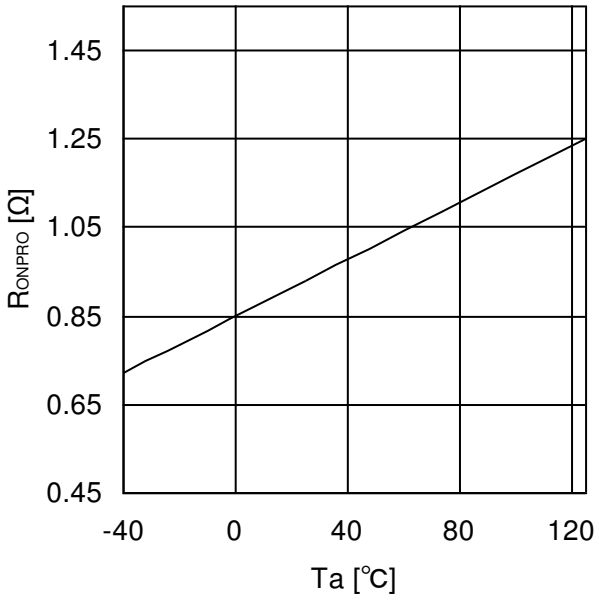


Figure 19. PROOUT ON-Resistance (IPROOUT=40mA)

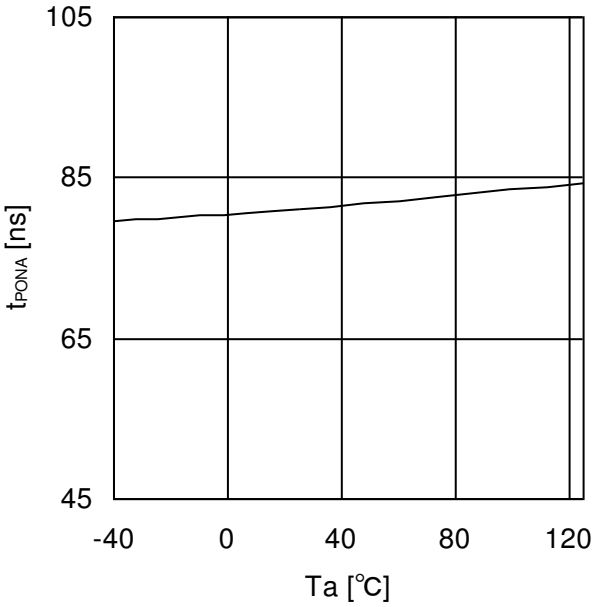


Figure 20. Turn ON time

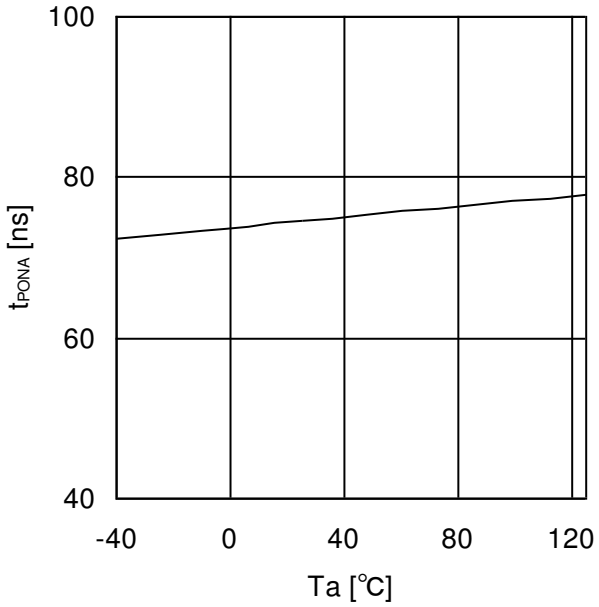


Figure 21. Turn OFF time

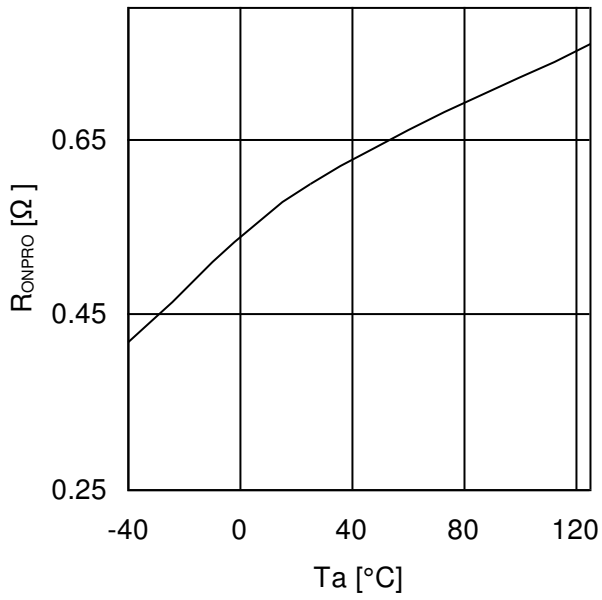


Figure 22. OUT2 ON-Resistance (IOUT2=40mA)

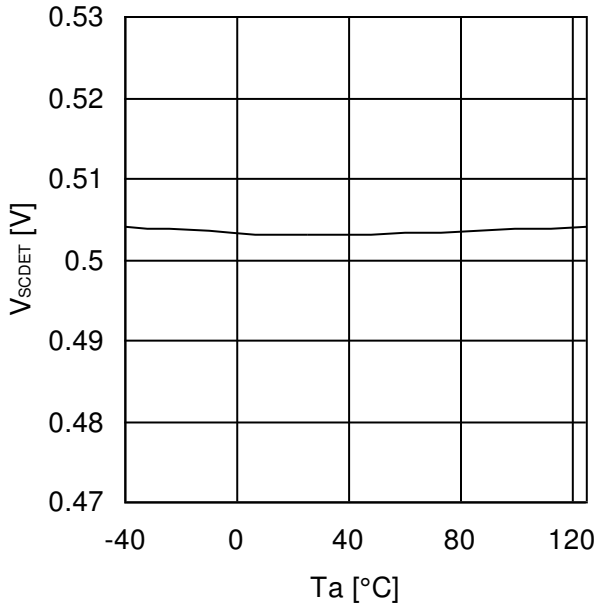


Figure 23. Short Current Detection Voltage

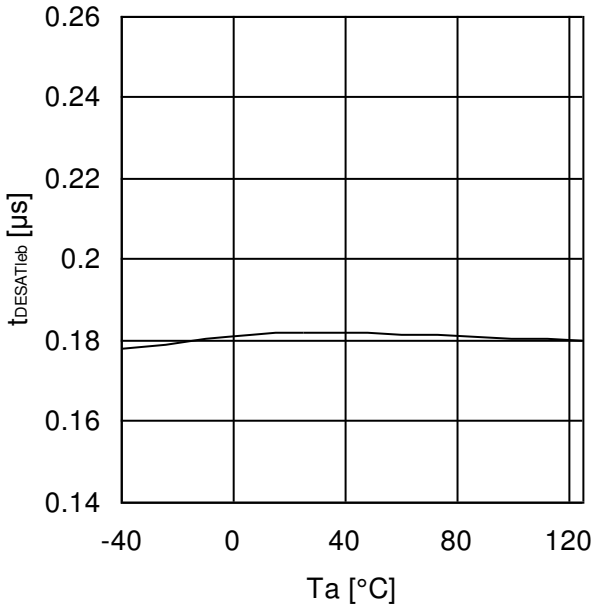


Figure 24. DESAT Leading Edge Blanking Time

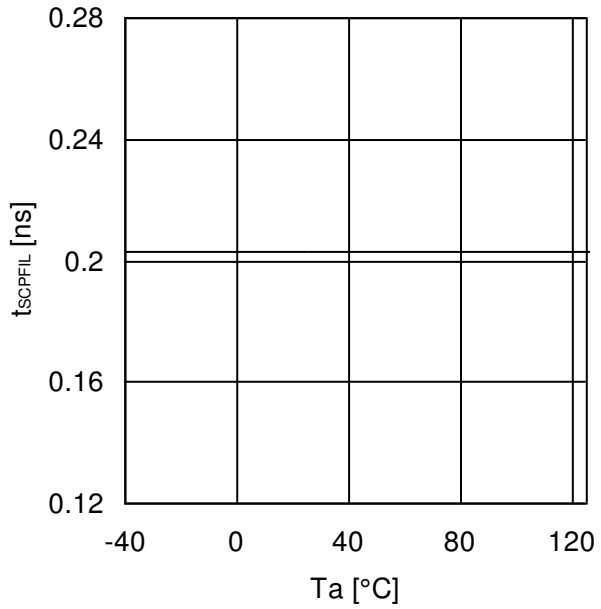


Figure 25. Short Current Detection Filter Time

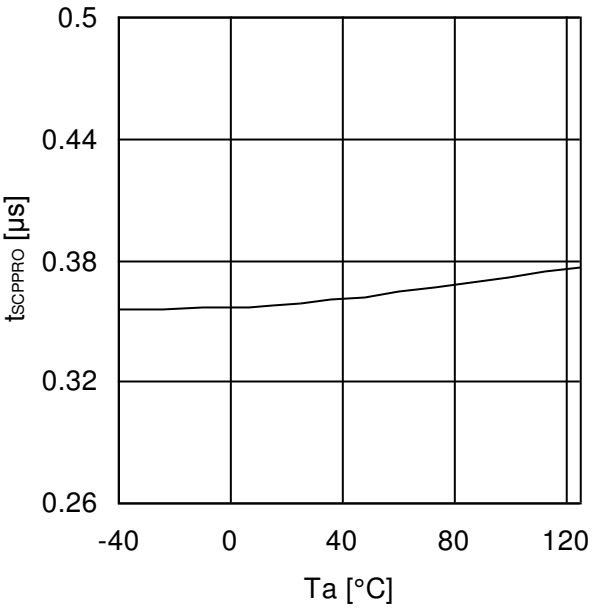


Figure 26. Short Current Detection Delay Time

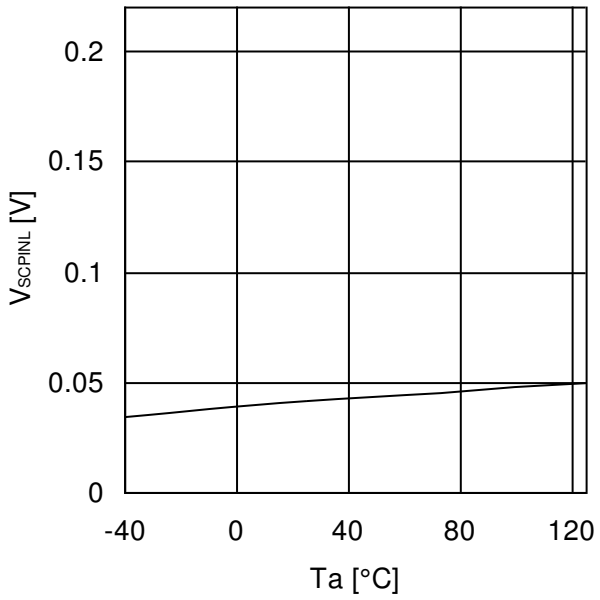


Figure 27. SCPIN Pin Low Voltage

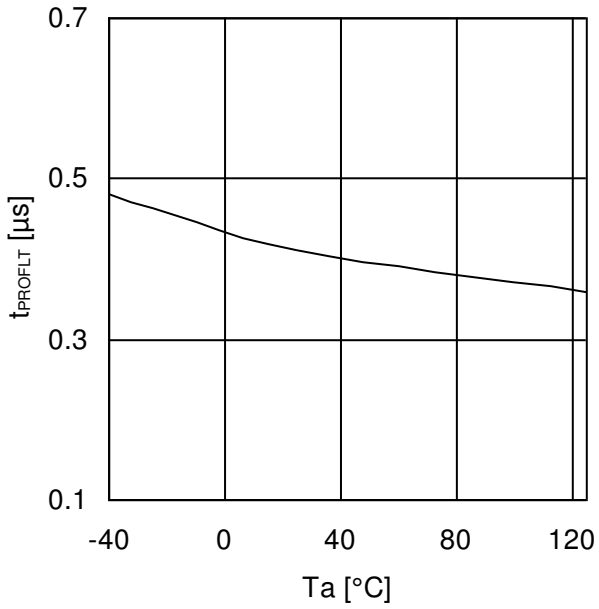


Figure 28. Output Delay Difference between PROOUT and FLT

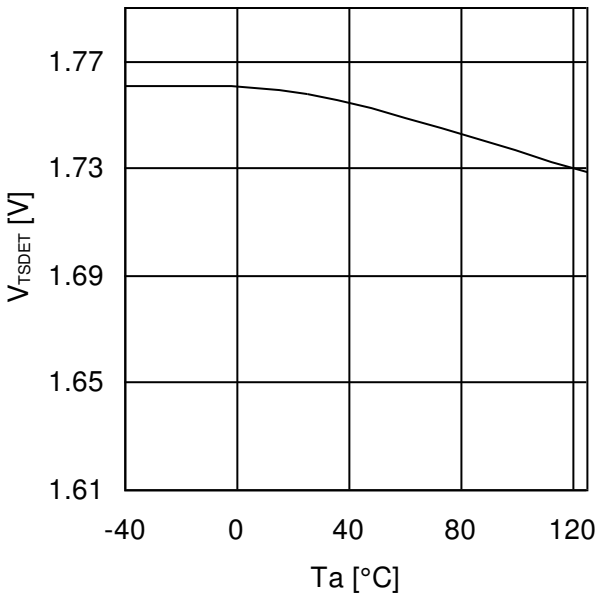


Figure 29. Thermal Detection Voltage

Application Information

1. Description of Pins and Cautions on Layout of Board

(1) V_BATT (Main Power Supply Pin)
This is the main power supply pin. Connect a bypass capacitor between V_BATT and GND1 in order to suppress voltage variations.

(2) GND1 (Input-side Ground Pin)
The GND1 pin is a ground pin on the input side.

(3) VCC2 (Output-side Positive Power Supply Pin)
The VCC2 pin is a positive power supply pin on the output side. To reduce voltage fluctuations due to OUT1H/L pin output current and due to the driving current of the internal transformers, connect a bypass capacitor between VCC2 and GND2 pins.

(4) VEE2 (Output-side Negative Power Supply Pin)
The VEE2 pin is a power supply pin on the output side. To suppress voltage fluctuations due to OUT1H/L pin output current and due to the driving current of the internal transformers, connect a bypass capacitor between the VEE2 and the GND2 pins. Connect the VEE2 pin to the GND2 pin when no negative power supply is used,

(5) GND2 (Output-side Ground Pin)
The GND2 pin is a ground pin on the output side. Connect the GND2 pin to the emitter / source of a power device.

(6) INA,INB,ENA (Control Input Terminal)
The INA,INB,ENA are pins used to determine output logic.

ENA	INB	INA	OUT1H	OUT1L
L	X	X	Hi-Z	L
H	H	X	Hi-Z	L
H	L	L	Hi-Z	L
H	L	H	H	Hi-Z

Fault state(FLT=L output) is released in rising of ENA(L→ H).

(7) FLT (Fault Output Pin)
The FLT pin is an open drain pin used to output a fault signal when short circuit protection function (SCP) or thermal protection function is activated, and will be cleared at the rising edge of ENA.

Status	FLT
While in normal operation	Hi-Z
When a fault occurs (When SCP or thermal protection is activated)	L

(8) RDY (Ready Output Pin)
The RDY pin shows the status of three internal protection features which are V_BATT UVLO, VCC2 UVLO, and output state feedback (OSFB). The term ‘output state feedback’ shows whether PROOUT pin voltage (High or Low) corresponds to input logic or not.

Status	RDY
While in normal operation	Hi-Z
V_BATT UVLO or VCC2 UVLO or Output state feedback	L

(9) MODE (Mode Selection Pin of Output-side UVLO)
The MODE pin is a pin which selects internal threshold or external setting threshold for output-side UVLO.

MODE	Output-side UVLO threshold voltage
L (=GND2)	Setting by external. (Use UVLOIN pin)
H (=VCC2)	Fixed (=V_{UVLO2L}). (Connect UVLOIN pin to VCC2 pin)

(10) UVLOIN (Output-side UVLO Setting Input Pin)
The UVLOIN pin is a pin for deciding UVLO setting value of VCC2. The threshold value of UVLO can be set by dividing the resistance voltage of VCC2 and inputting such value. UVLOIN activates only at MODE pin=L. When MODE pin=H, connect UVLOIN pin to VCC2 pin.

(11) OUT1H, OUT1L(Output Pin)
The OUT1H pin is a source side pin used to drive the gate of a power device, and the OUT1L pin is a sink side pin used to drive the gate of a power device.

(12) OUT2 (Miller Clamp Pin)
This is the miller clamp pin for preventing a rise of gate voltage due to miller current of output element connected to OUT1. It also functions as a pin for monitoring gate voltage for miller clamp and OUT2 pin voltage become not more than VOUT2ON(typ 2.0V), miller clamp function operates. OUT2 should be connect to VEE2 when miller clamp function is not used.

(13) PROOUT (Soft Turn-OFF Pin)
This is a pin for soft turn-OFF of output pin when short-circuit protection is in action. It also functions as a pin for monitoring gate voltage for output state feedback function.

(14) SCPIN(Short Circuit Current Detection Pin)
The SCPIN pin is a pin used to detect current for short circuit protection. When the SCPIN pin voltage exceeds V_{SCDET},SCP function will be activated. This may cause the IC to malfunction in an open state. To avoid such trouble, short-circuit the SCPIN pin to the GND2 pin when the short circuit protection is not used. In order to prevent the wrong detection due to noise, the noise filter time t_{SCPFIL} is set.

(15) VTSIN (Thermal Detection Pin)
The VTSIN pin is a temperature sensor voltage input pin, which can be used for thermal protection of an output device. If VTSIN pin voltage becomes V_{TSDET} or less, OUT1H/L pin is set to HiZ/L. IC may malfunction in the open status, so be sure to supply the VTSPIN more than V_{TSDET} if the thermal protection function is not used. In order to prevent the wrong detection due to noise, the noise mask time t_{TSMSK} is set. In addition, it can be used also as compulsive shutdown terminal other than a temperature sense by inputting a comparator output etc.

(16) RT (Switching Frequency Setting Pin for Switching Controller)
The RT pin is a pin used to make setting of switching frequency of switching controller. The switching frequency is determined by the resistance value connected between RT and GND1. The value of switching frequency is determined by the value of the resistor R_{RT}.

$$F_{SW}[kHz] = 1/(7.3\times10^{-8}\times R_{RT} + 2.2\times10^{-4})$$

(17) FB (Error Amplifier Inverting Input Pin for Switching Controller)
This is a voltage feedback pin of the switching controller. This pin combine with voltage monitoring at overvoltage protection function and under voltage protection function for switching controller. When overvoltage or under voltage protection is activated, switching controller will be at OFF state (FET_G pin outputs Low). When the protection holding time ($t_{DCDCRLS}$) is completed, the protection function will be released. Under voltage function is not activated during soft-start.

(18) COMP (Error Amplifier Output Pin for Switching Controller)
This is the gain control pin of the switching controller. Connect a phase compensation capacitor and resistor.

(19) VREG (Input-side internal power supply pin)
This is the input-side internal power supply pin. Be sure to connect a capacitor between VREG and GND1 even when the switching controller is not used, in order to prevent oscillation and suppress voltage variation due to FET_G output current.

(20) FET_G (MOS FET Control Pin for Switching Controller)
This is a MOSFET control pin for the switching controller transformer drive.

(21) SENSE (Connection to the Current Feedback Resistor of the Switching Controller)
This is a pin connected to the resistor of the switching controller current feedback. This pin combines with current monitoring at overcurrent protection function for switching controller. When overcurrent protection is activated, switching controller will be at OFF state (FET_G pin outputs Low). When the protection holding time ($t_{DCDCRLS}$) is completed, the over-current function will be released.

2. Description of Functions and Examples of Constant Setting

(1) Miller Clamp Function
When OUT1=L and OUT2 pin voltage < V_{OUT2ON}, internal MOS of OUT2 pin is turned ON and miller clamp function operates.

IN	OUT2 pin input voltage	OUT2
L	Not more than V_{OUT2ON}	L
H	X	Hi-Z

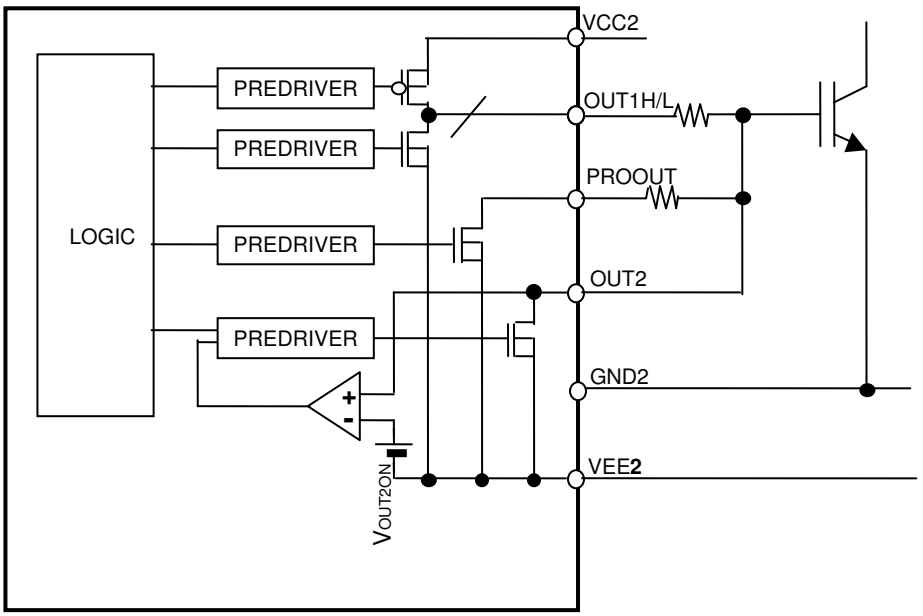


Figure 30. Block Diagram of Miller Clamp Function

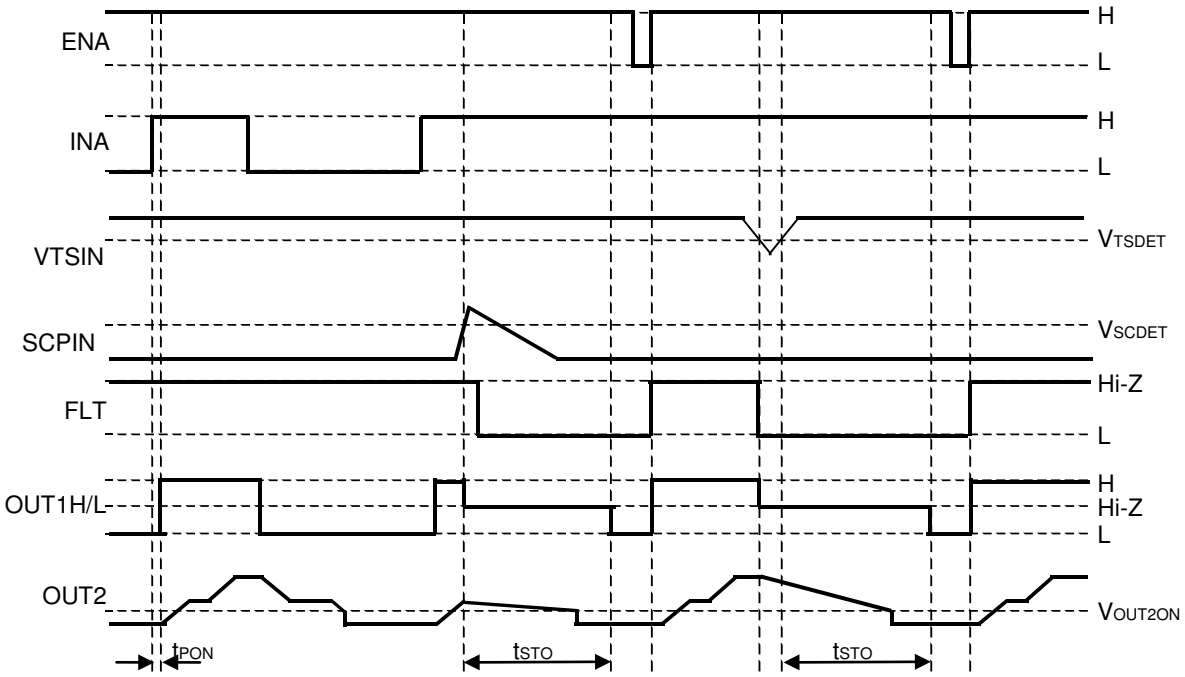


Figure 31. Timing Chart of Miller Clamp Function

(2) Under Voltage Lockout (UVLO) Function

The BM60054FV-C incorporates the under voltage lockout (UVLO) function on V_BATT and VCC2. When the power supply voltage drops to the UVLO ON voltage, the OUT1H/L pin will output the "Hi-Z / L" and the FLT pin will output the “L” signal. When the power supply voltage rises to the UVLO OFF voltage, these pins will be reset. In addition, to prevent mis-triggers due to noise, mask time $t_{UVLOBATTFIL}$ and $t_{UVLO2FIL}$ are set on both voltage sides.

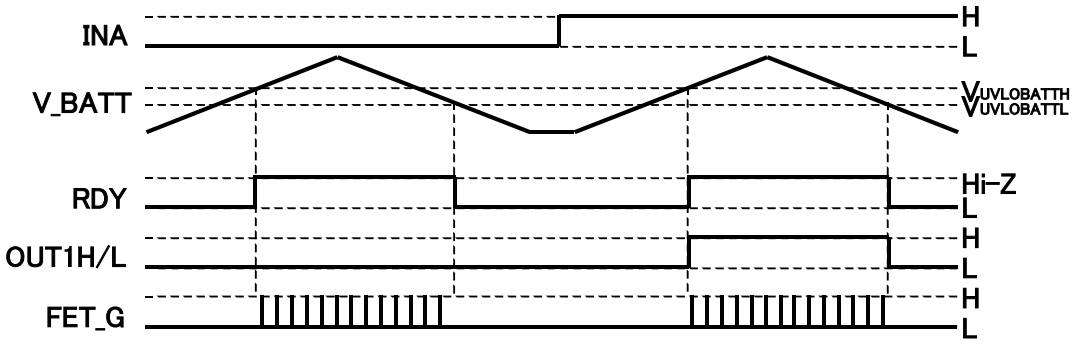


Figure 32. VBATT UVLO Function Operation Timing Chart

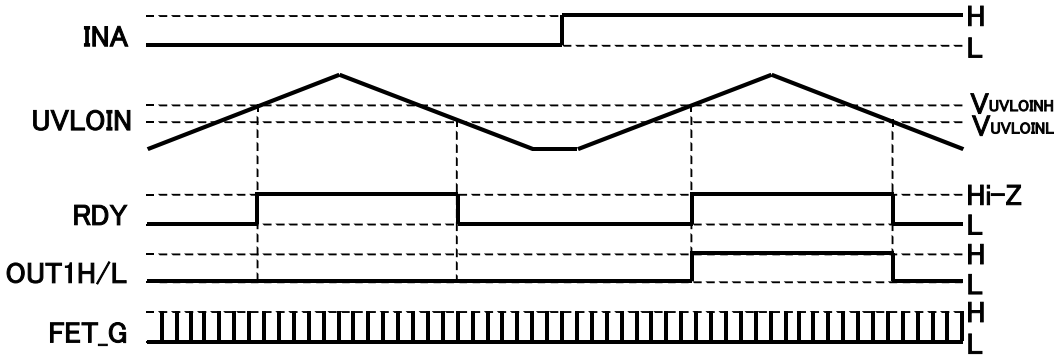


Figure 33. VCC2 UVLO Function Operation Timing Chart (MODE=L)

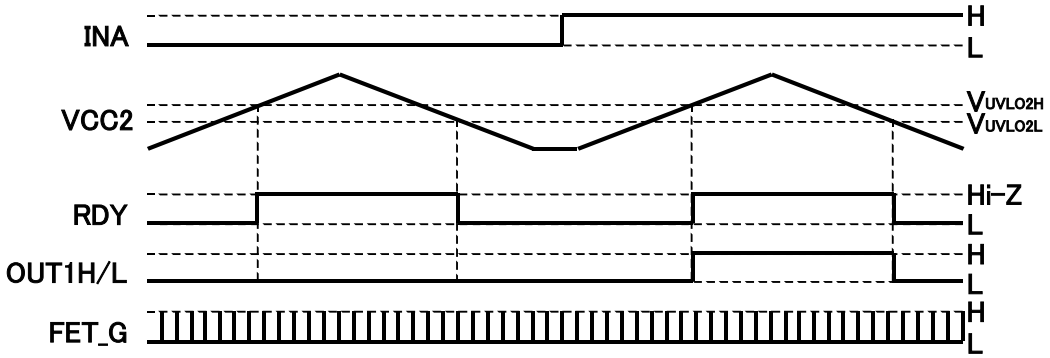


Figure 34. VCC2 UVLO Function Operation Timing Chart (MODE=H)

(3) Short Circuit Protection Function (SCP)

When the SCPIN pin voltage exceeds V_{SCDET}, the SCP function will be activated. When the SCP function is activated, the OUT1H/L pin voltage will be set to the “Hi-Z/Hi-Z” level and the PROOUT pin voltage will go to the “L” level first (soft turn-OFF). Next, After t_{STO} has passed, OUT1H/L pin become Hi-Z/L (PROOUT pin hold L). In addition, when OUT2 pin voltage < V_{OUT2ON}, miller clamp function operates.
When the rising edge is put in the ENA pin, the SCP function will be released.
When OUT1H/L=Hi-Z/L or Hi-Z/Hi-Z, internal MOSFET connected to SCPIN pin turns ON to discharge C_{BLANK} for desaturation protection function. When OUT1H/L=H/Hi-Z, internal MOSFET connected to SCPIN pin turns OFF.

$$V_{DESAT}[V] = V_{SCDET} \bullet \frac{R3+R2}{R3} - V_{F_{D1}}$$

$$V_{CC2_{MIN}}[V] > V_{SCDET} \bullet \frac{R3+R2+R1}{R3}$$

$$t_{BLANKoutemal}[s] = -\frac{R2+R1}{R3+R2+R1} \bullet R3 \bullet C_{BLANK} \bullet \ln(1 - \frac{R3+R2+R1}{R3} \bullet \frac{V_{SCDET}}{V_{CC2}}) + t_{DESATleb}$$

V_{DESAT}	設定参考値		
	R1	R2	R3
4.0V	15 kΩ	39kΩ	4.7kΩ
4.5V	15 kΩ	47kΩ	5.1kΩ
5.0V	15 kΩ	51kΩ	5.1kΩ
5.5V	15 kΩ	27kΩ	2.4kΩ
6.0V	15 kΩ	33kΩ	2.7kΩ
6.5V	15 kΩ	62kΩ	4.7kΩ
7.0V	15 kΩ	47kΩ	3.3kΩ
7.5V	15 kΩ	20kΩ	1.3kΩ
8.0V	15 kΩ	82kΩ	5.1kΩ
8.5V	15 kΩ	62kΩ	3.6kΩ
9.0V	15 kΩ	33kΩ	1.8kΩ
9.5V	15 kΩ	75kΩ	3.9kΩ
10.0V	15 kΩ	68kΩ	3.3kΩ

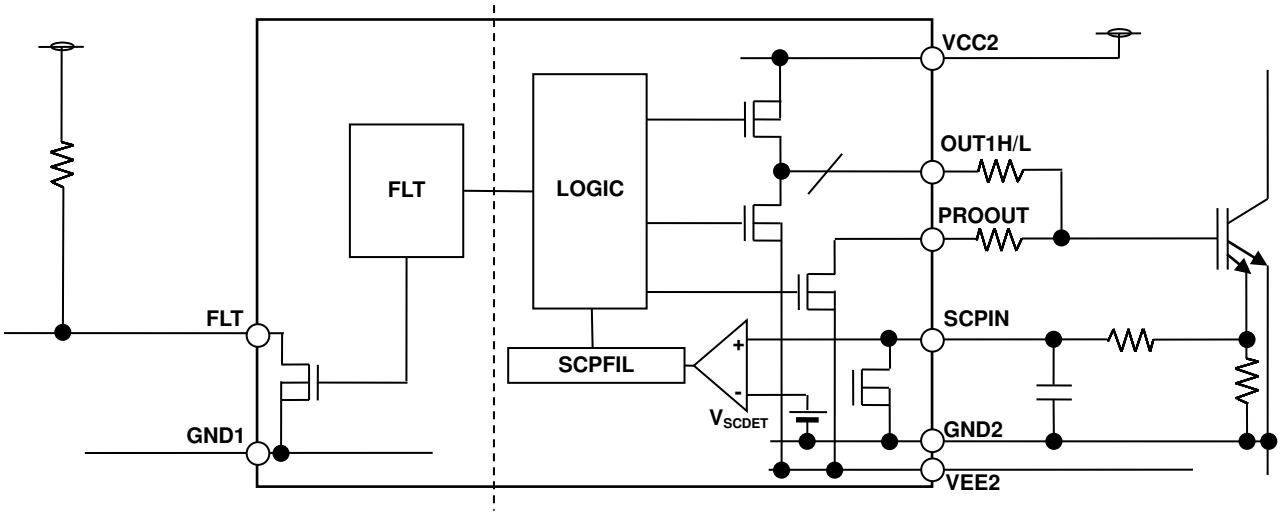


Figure 35. Block Diagram of Short Circuit Protection

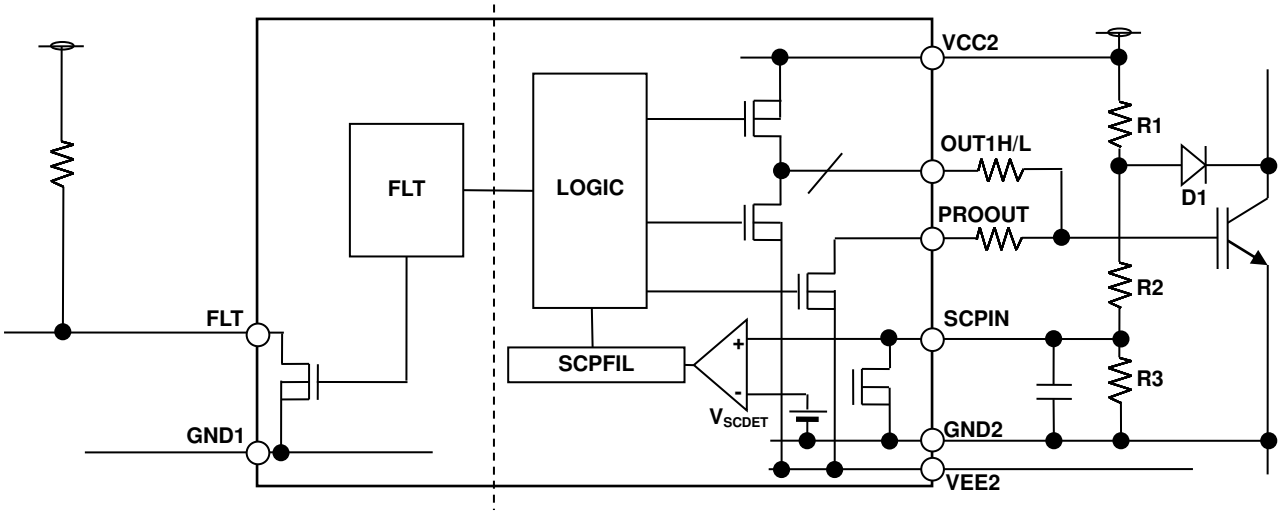


Figure 36. Block Diagram of DESAT

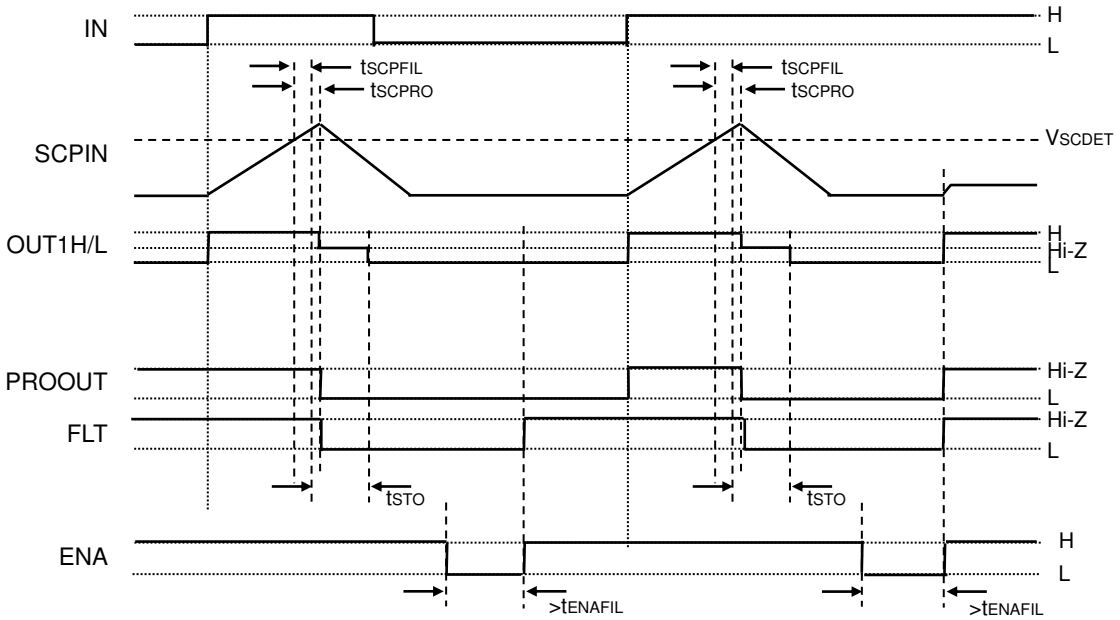


Figure 37. SCP Operation Timing Chart

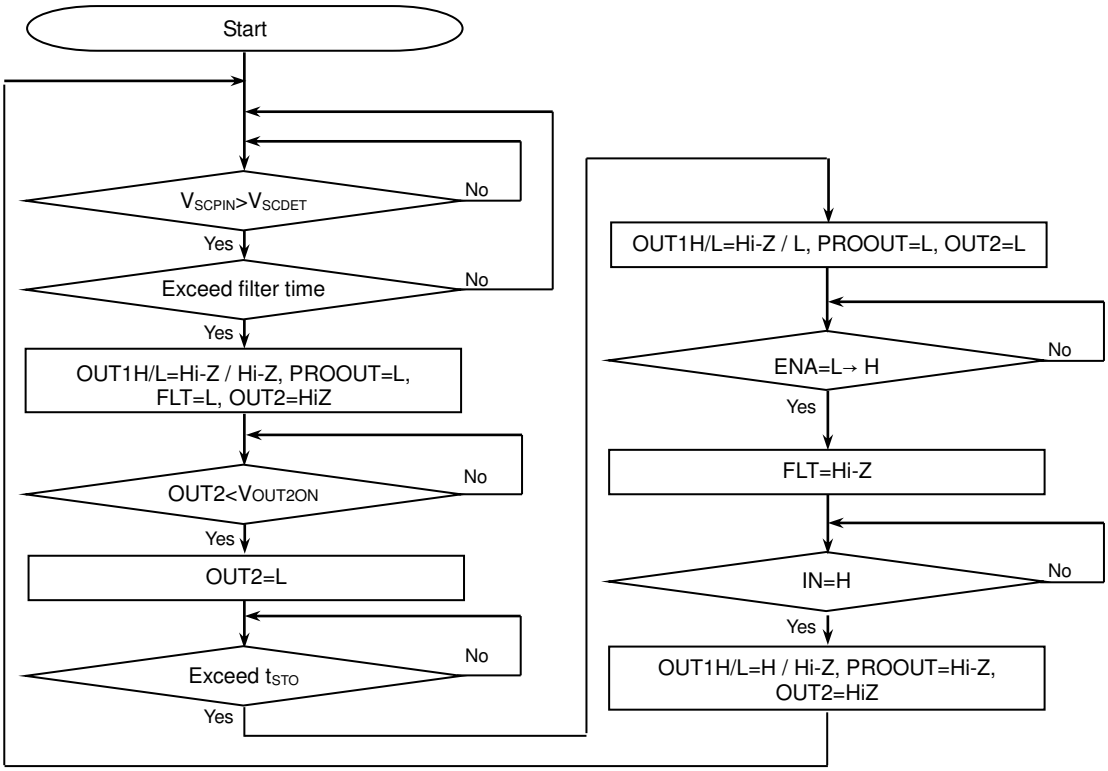


Figure 38. SCP Operation Status Transition Diagram

(4) Thermal Protection Function

When the VTSIN pin voltage becomes V_{TSDET} or less, the thermal protection function will be activated. When the thermal protection function is activated, the OUT1H/L pin voltage will be set to the “Hi-Z/Hi-Z” level and the PROOUT pin voltage will go to the “L” level first (soft turn-OFF). Next, when the VTSIN pin voltage rises to the threshold value and after t_{STO} has passed, OUT1H/L pin become Hi-Z/L (PROOUT pin hold L). In addition, when OUT2 pin voltage < V_{OUT2ON}, miller clamp function operates.

When the rising edge is put in the ENA pin, the thermal protection function will be released.

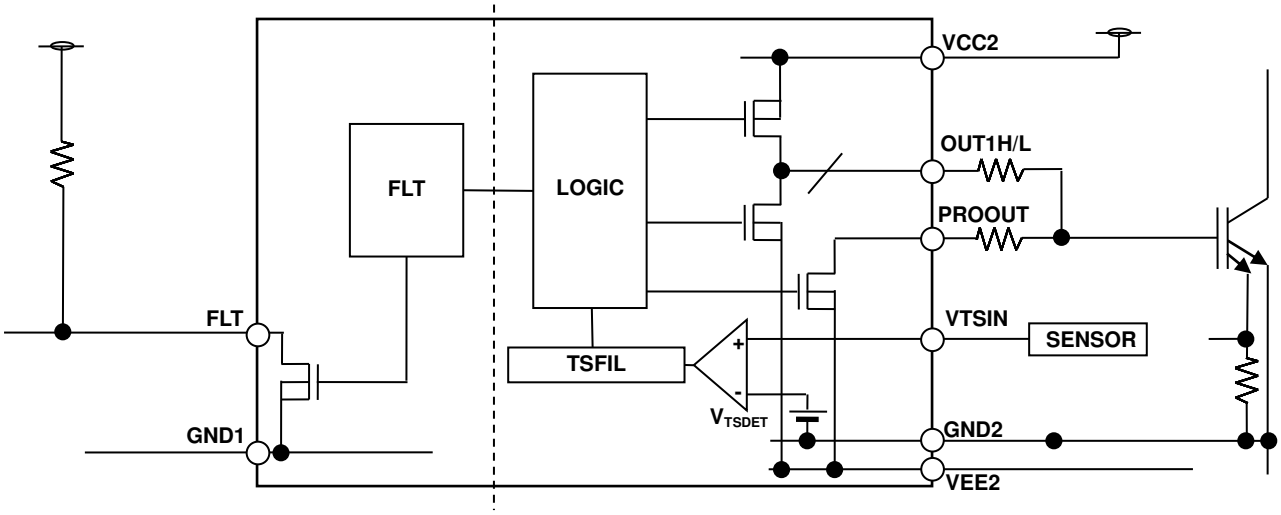


Figure 39. Block Diagram of thermal protection function

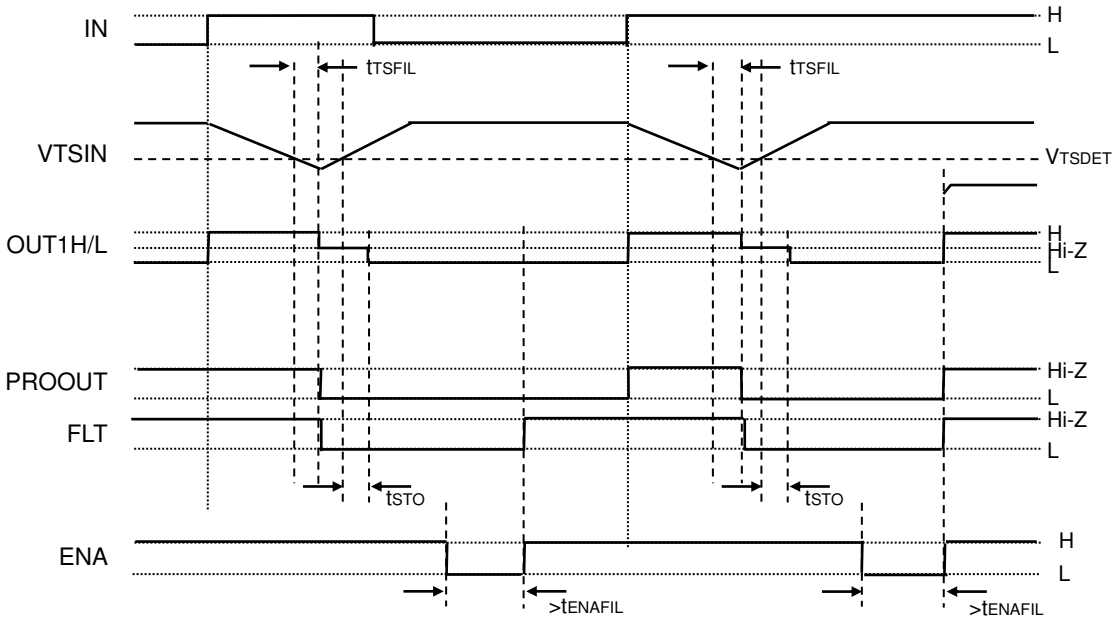


Figure 40. Thermal Protection Function Operation Timing Chart

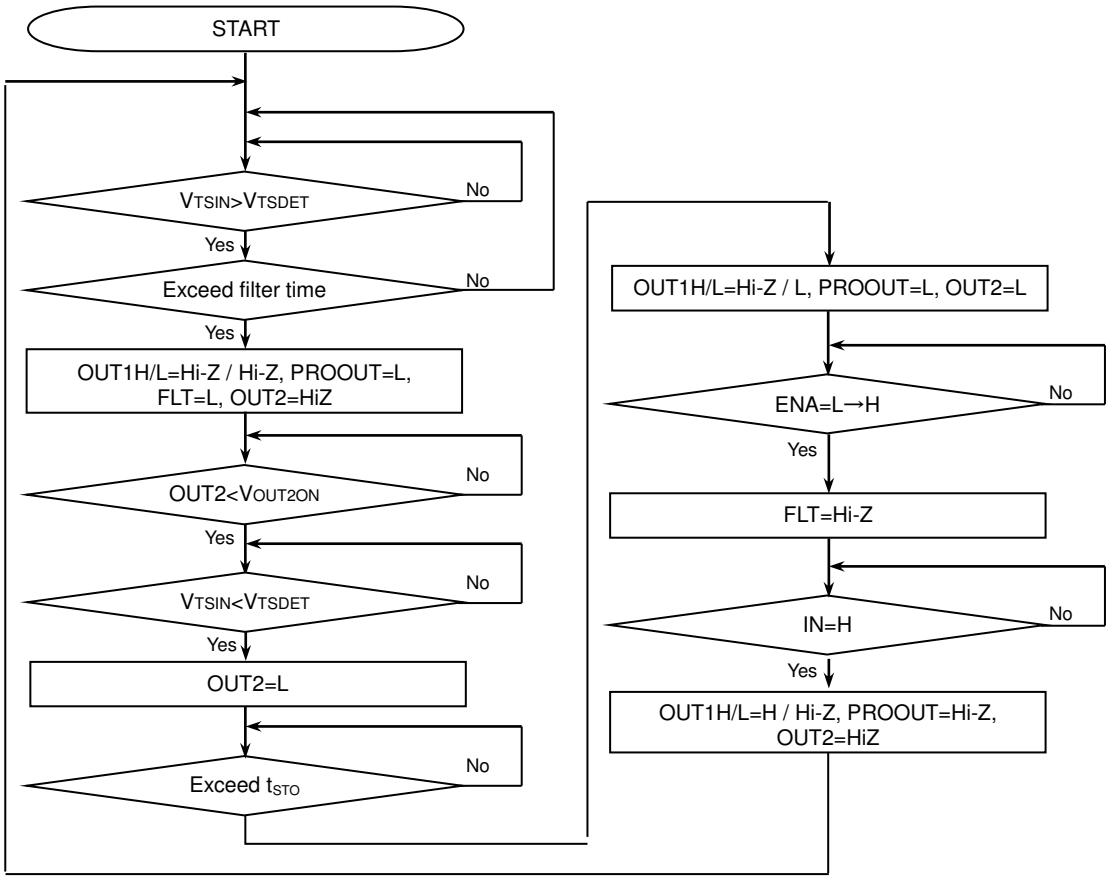


Figure 41. Thermal Protection Function Operation Status Transition Diagram

(5) Switching Controller

(a) Basic action

This IC has a built-in switching power supply controller which repeats ON/OFF synchronizing with internal clock set by RT pin. When VBATT voltage is supplied (VBATT > $V_{UVLOBATTH}$), FET_G pin starts switching by soft-start. Output voltage is determined by the following equation by external resistance and winding ratio “n” of flyback transformer (n= V_{OUT2} side winding number/V_{OUT1} side winding number)

$$V_{OUT2} = V_{FB} \times \{(R_1 + R_2)/R_2\} \times n\,[V]$$

(b) MAX DUTY

When, for example, output load is large, and voltage level of SENSE pin does not reach current detection level, output is forcibly turned OFF by Maximum On Duty (D_{ONMAX}).

(c) Protection function

The switching controller has protection function as overvoltage protection (OVP), under voltage protection (UVP), and over-current protection (OCP). OVP and UVP monitor the voltage of FB pin, OCP monitor the voltage of SENSE pin.

When the protection function is activated, switching controller will be OFF state (FET_G pin outputs Low). The protection holding time ($t_{DCDCRLS}$) is completed, the protection function will be released. Under voltage function is not activated during soft-start.

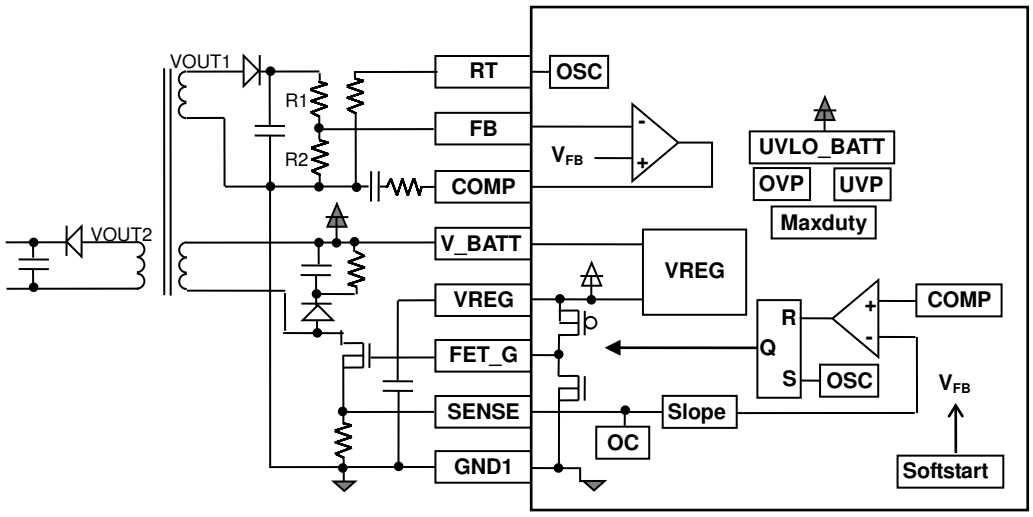


Figure 42. Block Diagram of switching controller

(d)The pin handling when not using switching controller

When not using switching controller, please do pin handling as follows.

pin no.	pin name	processing method
21	RT	pull down in gnd1 by 68kΩ
22	FB	connect to VREG
23	COMP	connect to VREG
24	V_BATT	connect power supply
25	VREG	connect capacitor
26	FET_G	open
27	SENSE	connect to VREG

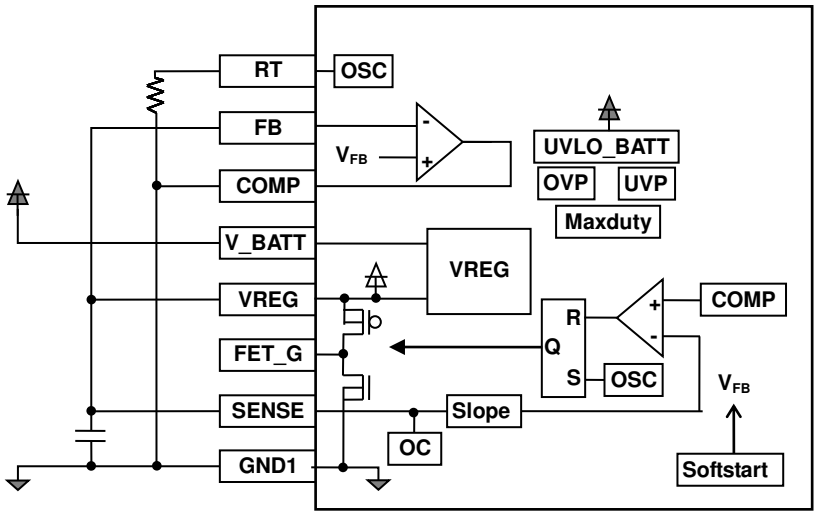


Figure 43. The pin handling when not using switching controller

(6) Gate State Monitoring Function

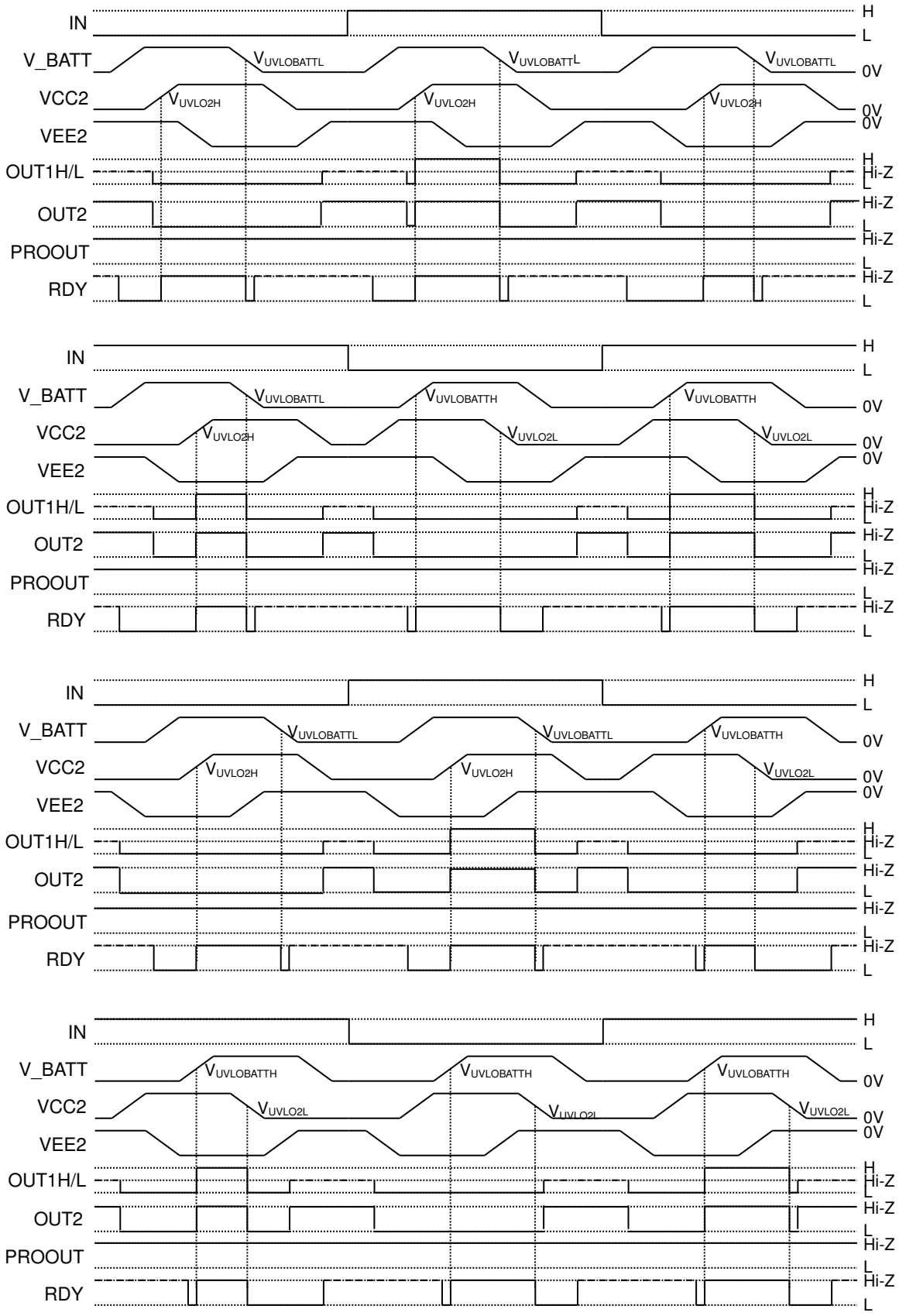
When gate logic and input logic of output device monitored with PROOUT pin are compared, a logic L is output from RDY pin when they disaccord. In order to prevent the detection error due to delay of input and output, OSFB filter time $t_{OSFBFIL}$ is provided.

(7) I/O Condition Table

No.	Status	Input									Output					
		VBATT	VCC2	SCPIN	VTSIN	ENA	INB	INA	OUT2	PROOUT	OUT1H	OUT1L	OUT2	PROOUT	FLT	RDY
1	SCP	○	○	H	H	H	L	H	H	X	Hi-Z	Hi-Z	Hi-Z	L	L	Hi-Z
2		○	○	H	H	H	L	H	L	X	Hi-Z	Hi-Z	L	L	L	Hi-Z
3	UVLO_VBATT	UVLO	○	L	H	X	X	X	H	H	Hi-Z	L	Hi-Z	Hi-Z	Hi-Z	L
4		UVLO	○	L	H	X	X	X	L	L	Hi-Z	L	L	Hi-Z	Hi-Z	L
5	UVLO_VCC2	○	UVLO	L	H	X	X	X	H	H	Hi-Z	L	Hi-Z	Hi-Z	Hi-Z	L
6		○	UVLO	L	H	X	X	X	L	L	Hi-Z	L	L	Hi-Z	Hi-Z	L
7	Thermal protection	○	○	L	L	X	X	X	H	X	Hi-Z	Hi-Z	Hi-Z	L	L	Hi-Z
8		○	○	L	L	X	X	X	L	X	Hi-Z	Hi-Z	L	L	L	Hi-Z
9	Disable	○	○	L	H	L	X	X	H	H	Hi-Z	L	Hi-Z	Hi-Z	Hi-Z	L
10		○	○	L	H	L	X	X	L	L	Hi-Z	L	L	Hi-Z	Hi-Z	Hi-Z
11	INB active	○	○	L	H	H	H	X	H	H	Hi-Z	L	Hi-Z	Hi-Z	Hi-Z	L
12		○	○	L	H	H	H	X	L	L	Hi-Z	L	L	Hi-Z	Hi-Z	Hi-Z
13	Normal Operation L Input	○	○	L	H	H	L	L	H	H	Hi-Z	L	Hi-Z	Hi-Z	Hi-Z	L
14		○	○	L	H	H	L	L	L	L	Hi-Z	L	L	Hi-Z	Hi-Z	Hi-Z
15	Normal Operation H Input	○	○	L	H	H	L	H	H	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
16		○	○	L	H	H	L	H	L	L	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	L

○ : > UVLO, X:Don't care

(8) Power Supply Startup / Shutoff Sequence



-·-·-·-·- : Since the VCC2 to VEE2 pin voltage is low and the output MOS does not turn ON, the output pins become Hi-Z conditions.

- - - - - - - : Since the VCC1 to GND1 pin voltage is low and the RDY output MOS does not turn ON, the output pins become Hi-Z conditions.

Figure 44. Power Supply Startup / Shutoff Sequence

Selection of Components Externally Connected

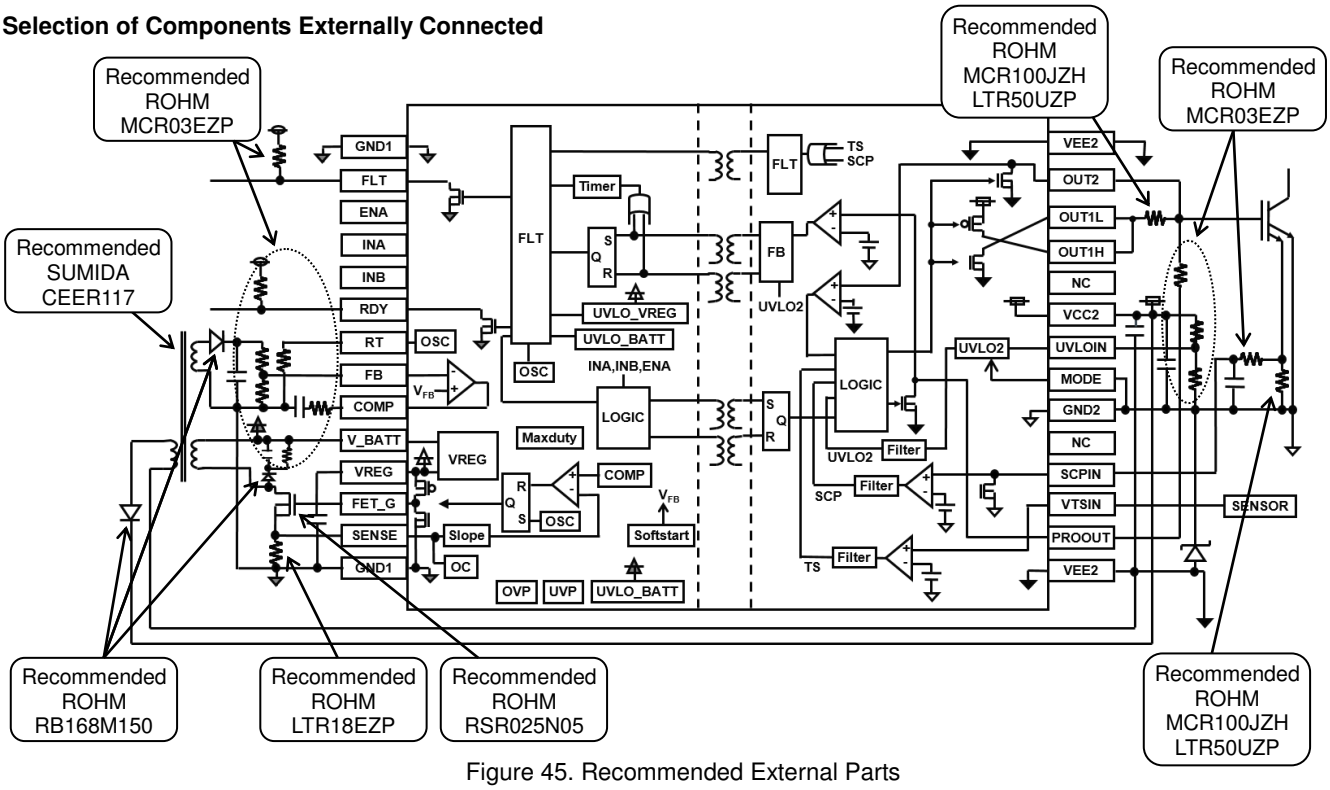


Figure 45. Recommended External Parts

Power Dissipation

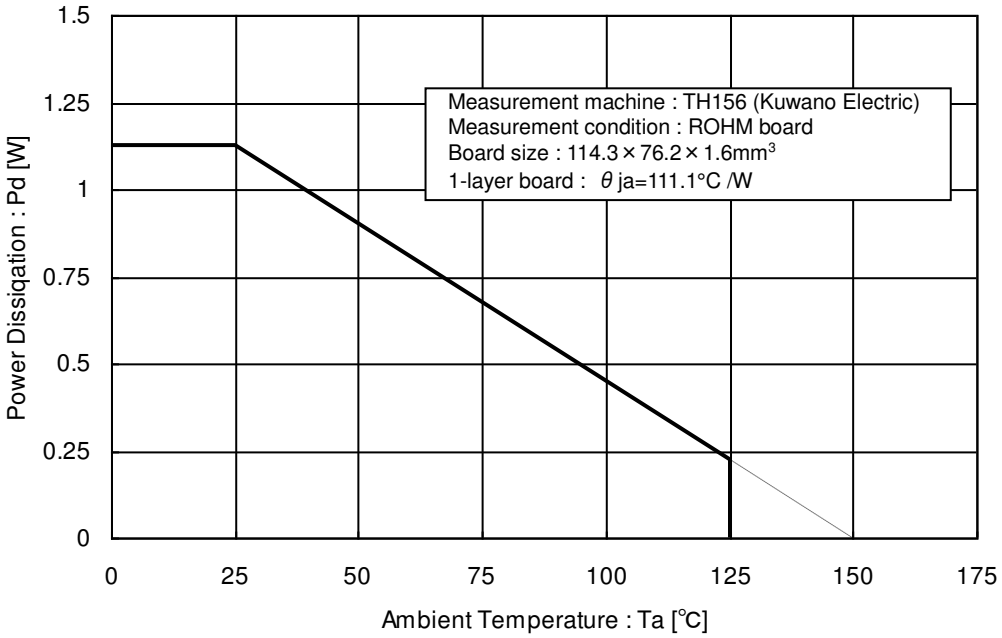
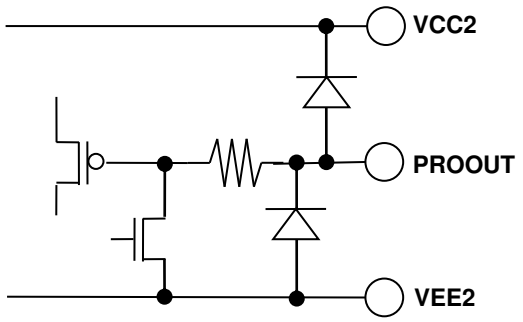
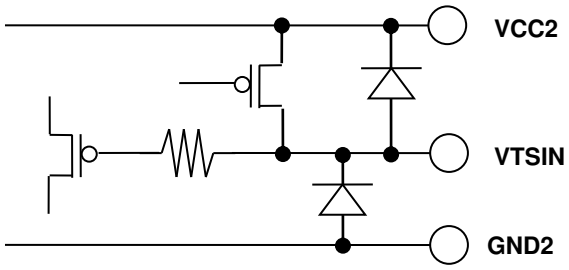
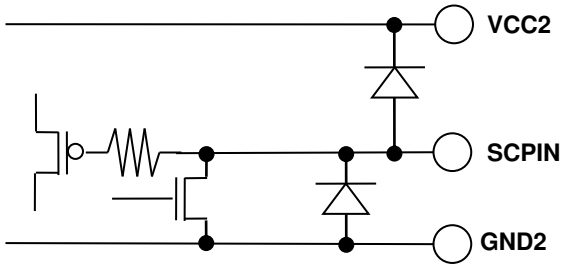
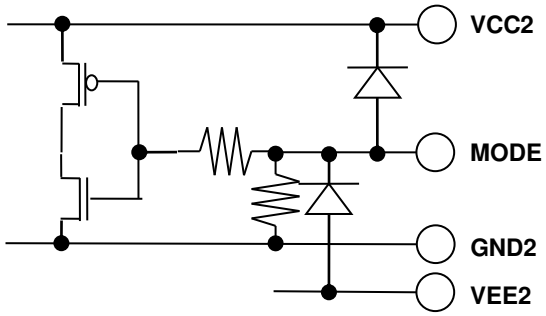
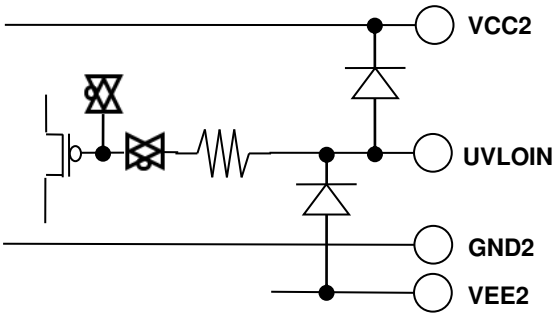


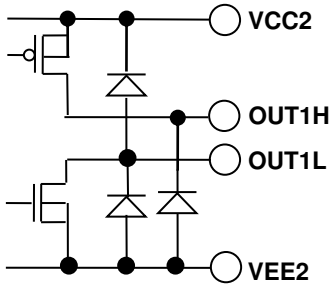
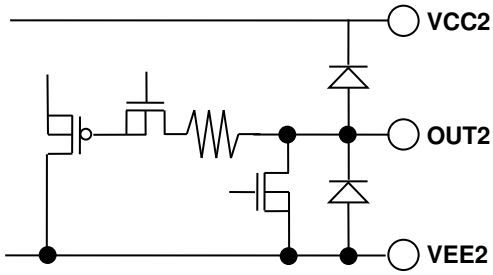
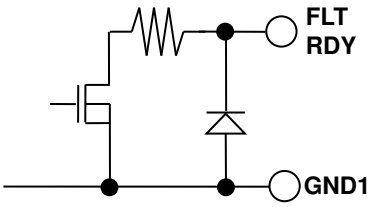
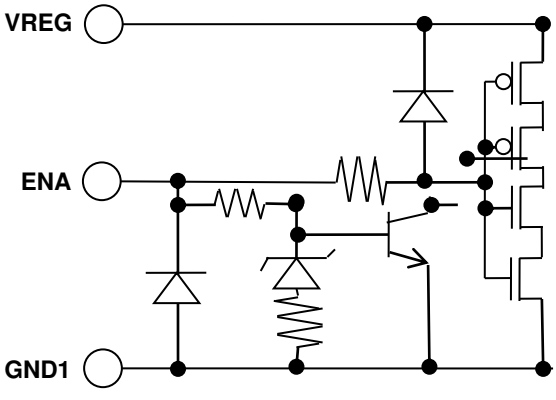
Figure 46. SSOP-B28W Derating Curve

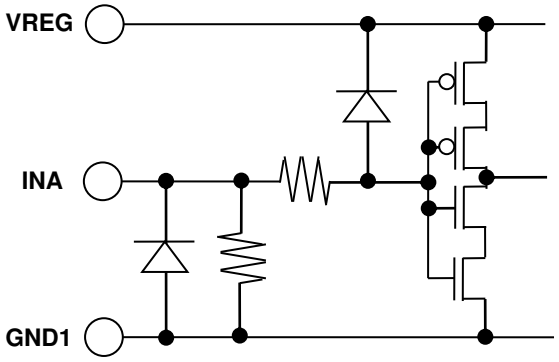
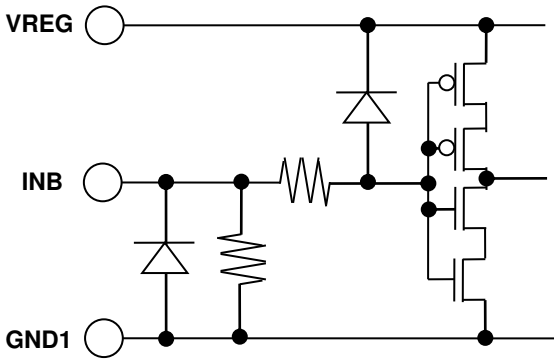
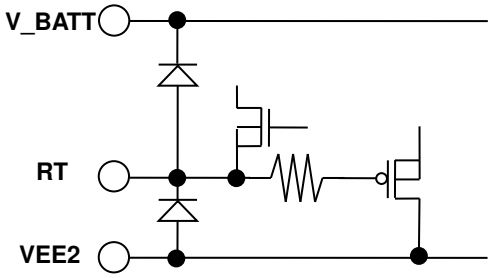
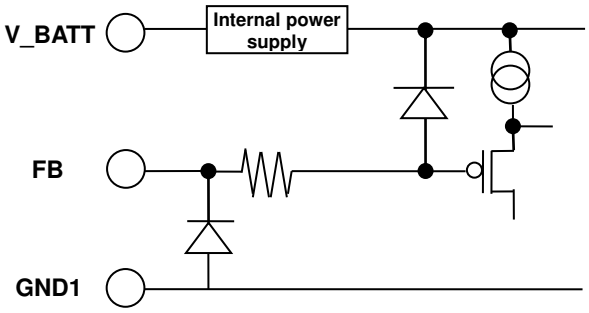
Thermal Design

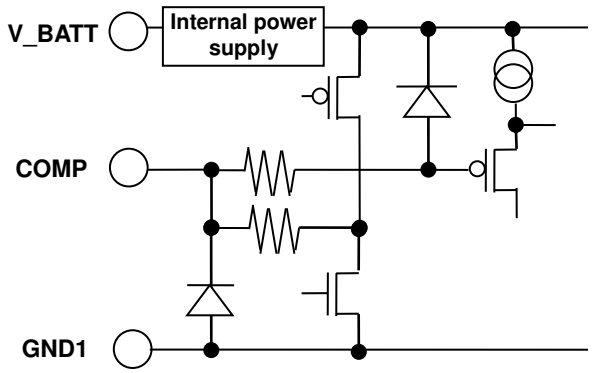
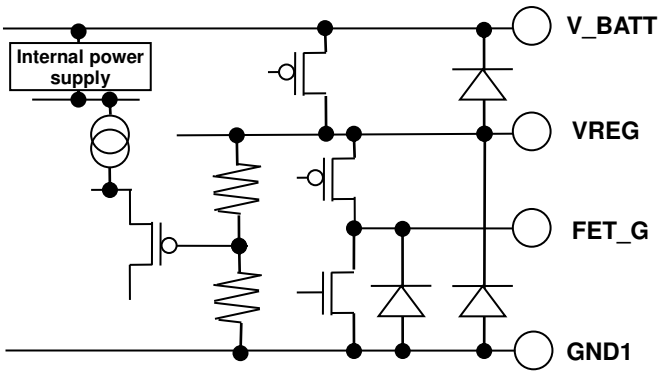
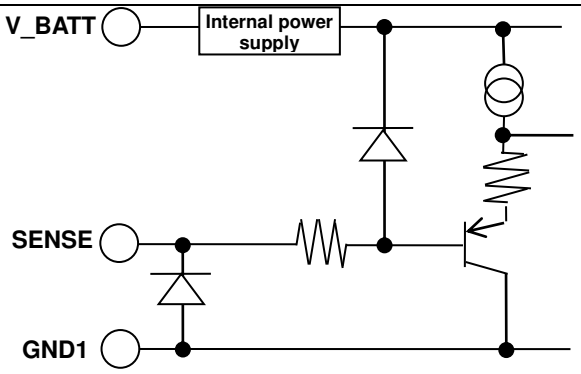
Please make sure that the IC's chip temperature Tj is not over 150°C, while considering the IC's power consumption (W), package power (Pd) and ambient temperature (Ta). When Tj=150°C is exceeded, the IC may malfunctions or some problems (ex. abnormal operation of various parasitic elements and increasing of leak current) may occur. Constant use under these circumstances leads to deterioration and eventually IC may destruct. Tjmax=150°C must be strictly obeyed under all circumstances.

I/O Equivalence Circuits

Pin No.	Pin Name / Pin Function	Input Output Equivalent Circuit Diagram
2	PROOUT Soft turn-off pin / Gate voltage input pin	
3	VTSIN Thermal detection pin	
4	SCPIN Schort circuit current detection pin	
7	MODE Mode selection pin of output-side UVLO	
8	UVLOIN Output-side UVLO setting pin	

Pin No.	Pin Name / Pin Function	Input Output Equivalent Circuit Diagram
11	OUT1H Source side output pin	
12	OUT1L Sink side output pin	
13	OUT2 Output pin for Miller Clamp	
16	FLT Fault output pin	
20	RDY Ready output pin	
17	ENA Input enabling signal pin	

Pin No.	Pin Name Pin Function	Input Output Equivalent Circuit Diagram
18	INA Control input pin A	
19	INB Control input pin B	
21	RT Switching frequency setting pin for switching controller	
22	FB Error amplifier inverting input pin for switching controller	

Pin No.	Pin Name / Pin Function	Input Output Equivalent Circuit Diagram
23	COMP Error amplifier output pin for switching controller	
25	VREG Input-side internal power supply pin	
26	FET_G MOS FET control pin for switching controller	
27	SENSE Current detection pin for switching controller	

Operational Notes

1. Reverse Connection of Power Supply
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

2. Power Supply Lines
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Terminals
    Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding Input Pins of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

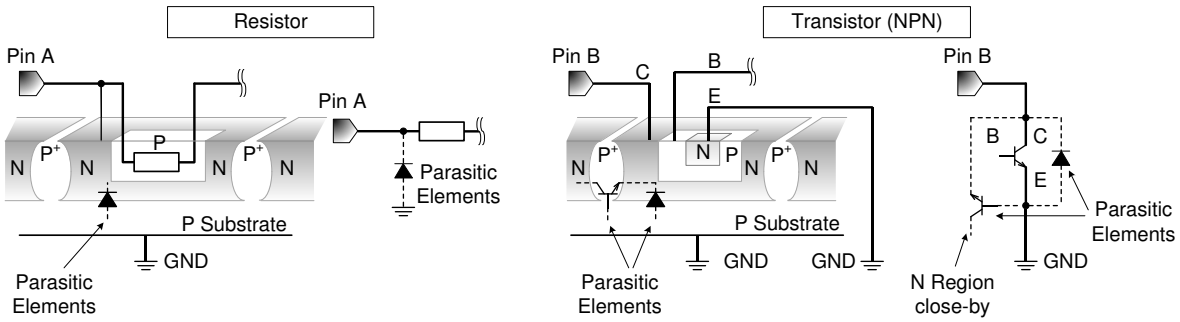
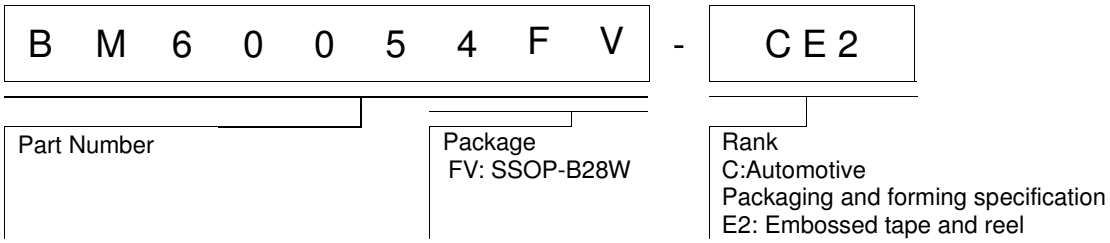


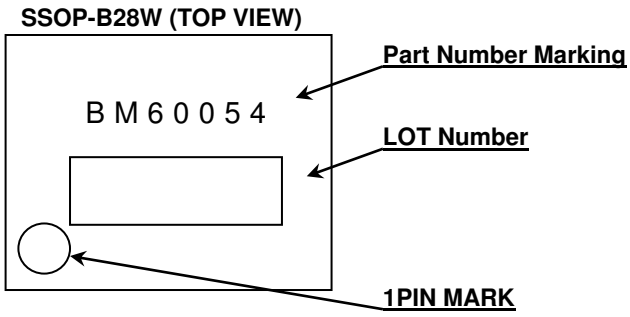
Figure 47. Example of Monolithic IC Structure

13. Ceramic Capacitor
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

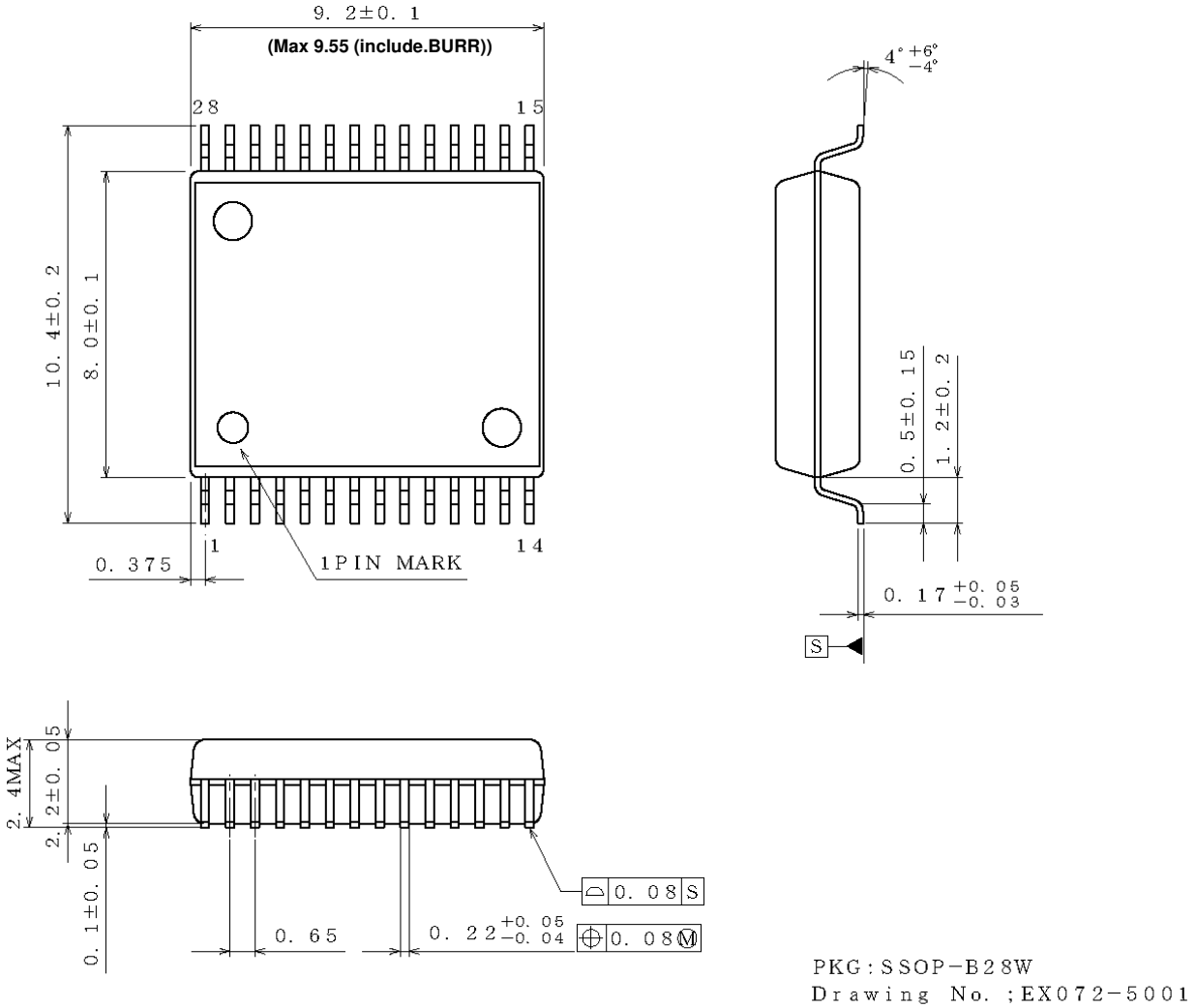


Marking Diagram



Physical Dimension, Tape and Reel Information

Package Name	SSOP-B28W

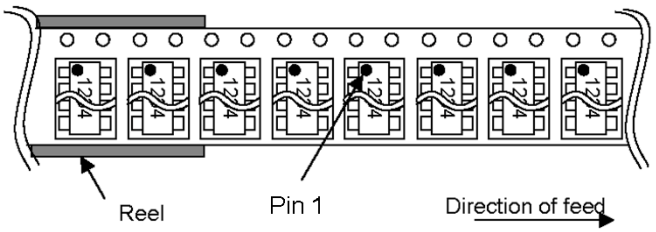


PKG : SSOP−B28W
Drawing No. ; EX072−5001

(UNIT : mm)

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
10.Apr.2015	001	New Release
25.Dec.2015	002	Page 7 Adding UL1577 Rating Table Page15 Misprint correction of Description of Pins and Cautions on Layout of Board (7)FLT Page17 Misprint correction of Description of Functions and Examples of Constant Setting (1)Miller Clamp Function

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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