LINEAR SYSTEMS

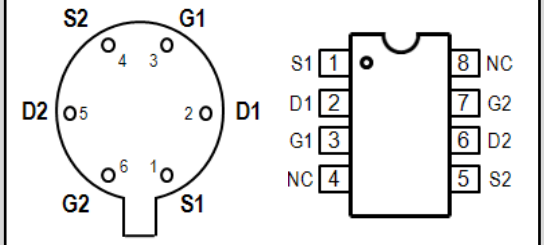
Twenty-Five Years Of Quality Through Innovation

SST/U401 – SST/U406

LOW NOISE LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
LOW DRIFT	$\lvert V_{GS1-2}/T \rvert$ = 10µV/ºC TYP.
LOW NOISE	e_n=6nV/Hz@10Hz TYP.
LOW PINCHOFF	V_P=2.5V MAX.

ABSOLUTE MAXIMUM RATINGS NOTE 1 @ 25 °C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55 to +150°C
Operating Junction Temperature		-55 to +150°C
Maximum Voltage and Current for Each Transistor NOTE 1		
$-V_{GSS}$	Gate Voltage to Drain or Source	50V
$-V_{DSO}$	Drain to Source Voltage	50V
$-I_{G(f)}$	Gate Forward Current	10mA
Maximum Power Dissipation per side NOTE 2		
Device Dissipation TA = 25°C		300mW



TO-71 Top View

SOIC Top View

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	U401	U402	U403	U404	U405	U406	UNITS	CONDITIONS
$\lvert V_{GS1-2}/T \rvert$ max.	Drift vs. Temperature	10	10	25	25	40	80	µV/ºC	V_{DG} = 10V, I_D = 200µA T_A = -55ºC to +125ºC
$\lvert V_{GS1-2} \rvert$ max.	Offset Voltage	5	10	10	15	20	40	mV	V_{DG} = 10V, I_D = 200µA

ELECTRICAL CHARACTERISTICS TA = 25ºC (unless otherwise noted) NOTE 3

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-50	-60	--	V	V_{DS}= 0 I_D= 1nA
BV_{G1G2}	Gate-to-Gate Breakdown	±50	--	--	V	I_G= ±1µA I_D= 0, I_S = 0
	TRANSCONDUCTANCE					
G_{fss}	Full Conduction	2000	--	7000	µS	V_{DG}= 10V V_{GS}= 0 f = 1kHz
G_{fs}	Typical Operation	1000	--	2000	µS	V_{DG}= 15V I_D= 200µA f = 1kHz
$\lvert G_{fs1}/G_{fs2} \rvert$	Mismatch	0.97	--	1.0		
I_{DSS}	Saturation Drain Current	0.5	--	10	mA	V_{DG}= 10V V_{GS}= 0
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Current Ratio	0.9	0.98	1.0		
	GATE VOLTAGE					
V_{GS}(off) or V_P	Pinchoff Voltage	-0.5	--	-2.5	V	V_{DS}= 15V I_D= 1nA
V_{GS}	Operating Range	--	--	-2.3	V	V_{DS}= 15V I_D= 200µA
	GATE CURRENT					
I_G	Operating	--	-4	-15	pA	V_{DG}= 15V I_D= 200µA
I_G	High Temperature	--	--	-10	nA	T_A=+125ºC
I_{GSS}	Gate Reverse Current	--	--	-100	pA	V_{GS}=-30v, V_{DS}= 0V
I_{G1G2}	Gate to Gate Isolation Current	--	--	±1.0	µA	V_{G1}-V_{G2}= ±50V, I_D= IS= 0

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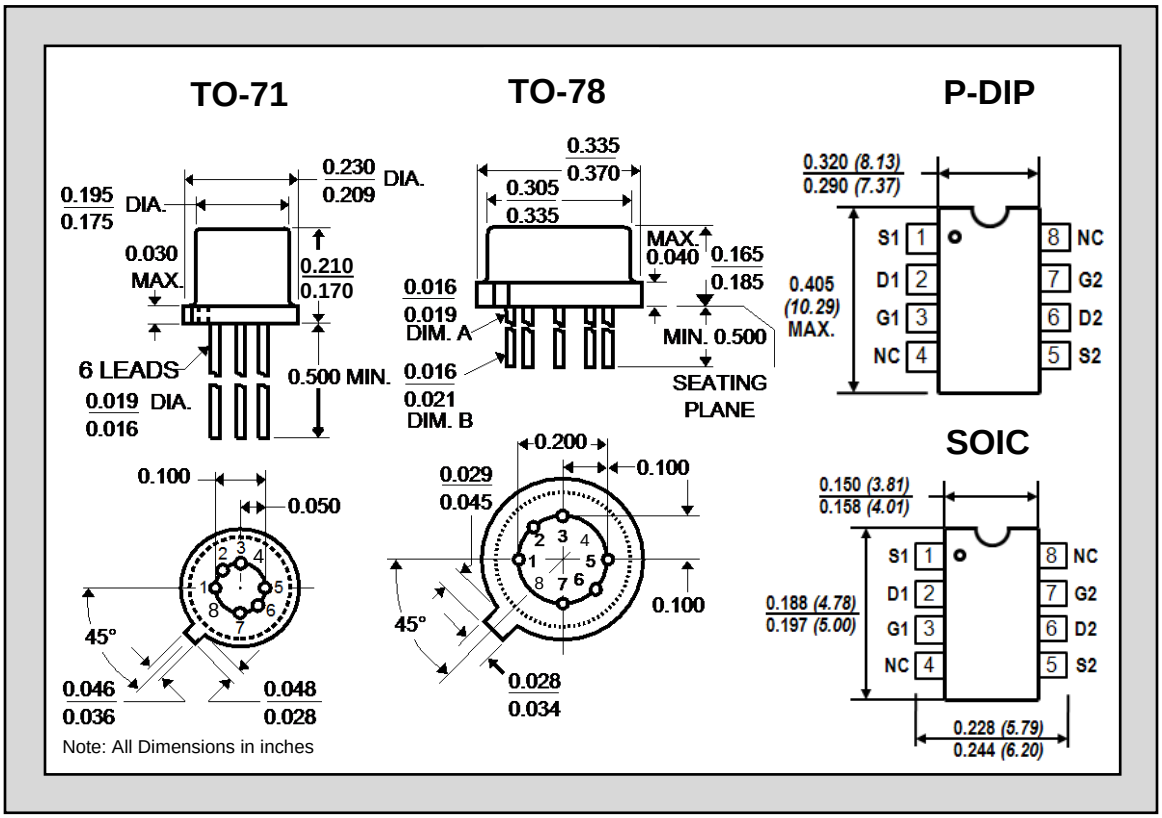
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	OUTPUT CONDUCTANCE					
G_{OSS}	Full Conduction	--	--	40	µS	V_{DS}= 10V, V_{GS}= 0V, f = 1kHz
G_{OS}	Operating	--	2	2.7	µS	V_{DS}= 15V, I_D= 200µA, f = 1kHz
	COMMON MODE REJECTION					V_{DG1}= 10V
CMRR	-20 log [(V_{GS1}-V_{GS2})/ΔV_{DG1-2}]	95	--	--	dB	V_{DG2}= 20V I_{D1}= I_{D2}=200µA
	NOISE					
NF	Figure	--	--	0.5	dB	V_{DS}= 15V V_{GS}= 0 R_G=10M f= 100Hz NBW= 6Hz
e_n	Voltage	--	6	20	nV/Hz	V_{DS}= 15V I_D= 200µA f= 10Hz NBW= 1Hz
	CAPACITANCE					
C_{ISS}	Input	--	4	8	pF	V_{DS}= 15V I_D= 200µA f= 1MHz
C_{RSS}	Reverse Transfer	--	1.5	3	pF	



Note: All Dimensions in inches

NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. Derate 2.4mW/ºC when TA is greater than 25ºC
3. All MIN/TYP/MAX limits are absolute numbers. Negative signs indicate electrical polarity only.

Linear Integrated Systems (LIS) is a 25-year-old, third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company President John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, Co-Founder and Vice President of R&D at Intersil, and Founder/President of Micro Power Systems.

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