



# CTL0322PS-R3

## P-Channel Enhancement MOSFET

### Features

- Drain-Source Breakdown Voltage  $V_{DS} -20\text{ V}$
- Drain-Source On-Resistance  
 $R_{DS(ON)} 55\text{m}\Omega$ , at  $V_{GS} = -4.5\text{V}$ ,  $I_D = -3.2\text{A}$   
 $R_{DS(ON)} 70\text{m}\Omega$ , at  $V_{GS} = -2.5\text{V}$ ,  $I_D = -2.4\text{A}$   
 $R_{DS(ON)} 100\text{m}\Omega$ , at  $V_{GS} = -1.8\text{V}$ ,  $I_D = -1.7\text{A}$
- Continuous Drain Current at  $T_A=25^\circ\text{C}$   $I_D = -3.2\text{A}$
- Advanced high cell density Trench Technology
- RoHS Compliance & Halogen Free

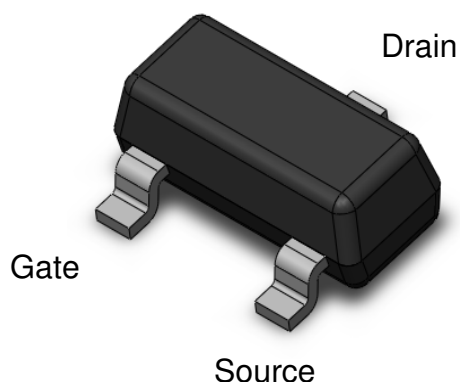
### Description

The CTL0322PS-R3 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

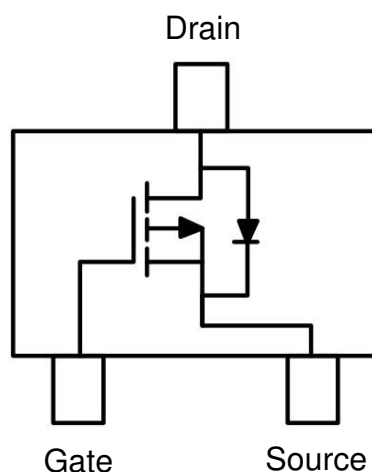
### Applications

- Power Management
- Lithium Ion Battery
- High-Side Switching

### Package Outline



### Schematic



**Absolute Maximum Rating at 25°C**

Symbol	Parameters	Test Conditions	Min	Notes
V <sub>DS</sub>	Drain-Source Voltage	-20	V	
V <sub>GS</sub>	Gate-Source Voltage	±12	V	
I <sub>D</sub>	Continuous Drain Current @T <sub>A</sub> =25°C	-3.2	A	1
I <sub>DM</sub>	Pulsed Drain Current	-10	A	1
P <sub>D</sub>	Total Power Dissipation	1.4	W	2
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C	
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C	

**Thermal Characteristics**

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
R <sub>θJA4</sub>	Thermal Resistance Junction-Ambient (t=10s)		--	65	--	°C /W	1,4

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  (unless otherwise specified)**Static Characteristics**

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$B_{V_{DS}}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-20	-	-	V	
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS} = -20V, V_{GS} = 0V$	-	-	-1	$\mu A$	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS} = \pm 12V, V_{DS} = 0V$	-	-	$\pm 100$	nA	

**On Characteristics**

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$R_{DS(ON)}$	Drain-Source On-Resistance	$V_{GS} = -4.5V, I_D = -3.2A$	-	55	75	m $\Omega$	3
		$V_{GS} = -2.5V, I_D = -2.4A$	-	70	95	m $\Omega$	
		$V_{GS} = -1.8V, I_D = -1.7A$	-	100	130	m $\Omega$	
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu A$	-0.4	-0.6	-0.9	V	3

**Dynamic Characteristics**

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$C_{ISS}$	Input Capacitance	$V_{GS} = 0V,$ $V_{DS} = -15V$ $f = 1MHz$	-	650	680	pF	
$C_{OSS}$	Output Capacitance		-	65	-		
$C_{RSS}$	Reverse Transfer Capacitance		-	16	-		

**Switching Characteristics**

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
$T_{D(ON)}$	Turn-On Delay Time	$V_{DS} = -6V,$ $V_{GS} = -4.5V,$ $R_G = 6\Omega,$ $R_L = 3.6\Omega,$	-	52	-	ns	
$T_R$	Rise Time		-	30	-		
$T_{D(OFF)}$	Turn-Off Delay Time		-	53	-		
$T_F$	Fall Time		-	10	-		
$Q_G$	Total Gate Charge	$V_{DS} = -6V,$ $V_{GS} = -4.5V,$ $I_D = -4A$	-	9.3	-	nC	
$Q_{GS}$	Gate-Source Charge		-	3	-		
$Q_{GD}$	Gate-Drain Charge		-	1.5	-		

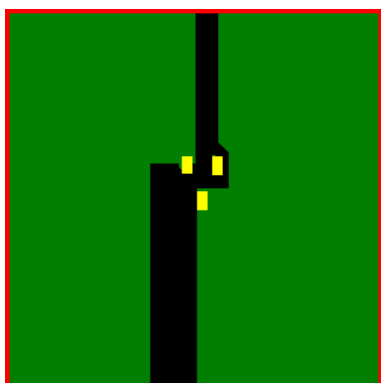


**Drain-Source Diode Characteristics**

Symbol	Parameters	Test Conditions	Min	Typ	Max	Units	Notes
V <sub>SD</sub>	Body Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = -1A	-	-0.7	-1.0	V	
I <sub>SD</sub>	Body Diode Continuous Current		-	-	-1	A	1

Note:

- 1. The power dissipation is limited by 150°C junction temperature.
- 2. Device mounted on a glass-epoxy board



FR-4  
25.4 × 25.4 mm .  
2 Oz Copper

Actual Size

- 3. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 4. Thermal Resistance follow JESD51-3.



Typical Characteristic Curves

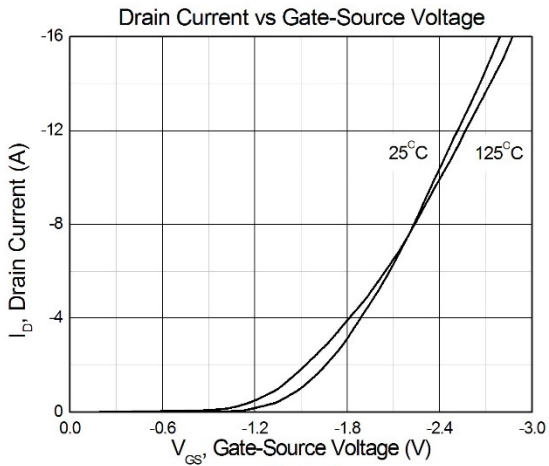


Figure 1

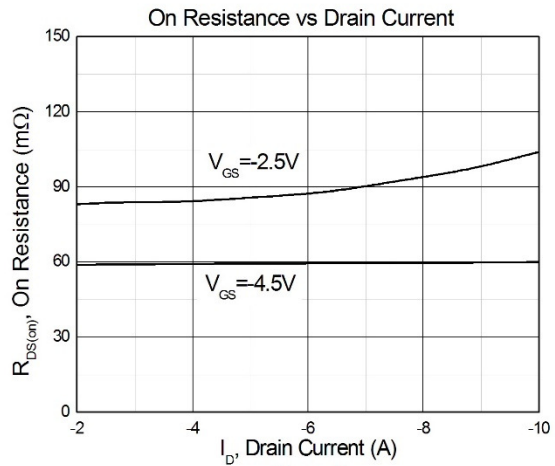


Figure 2

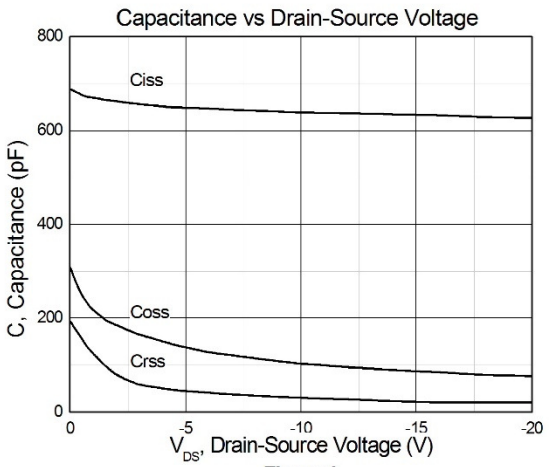


Figure 3

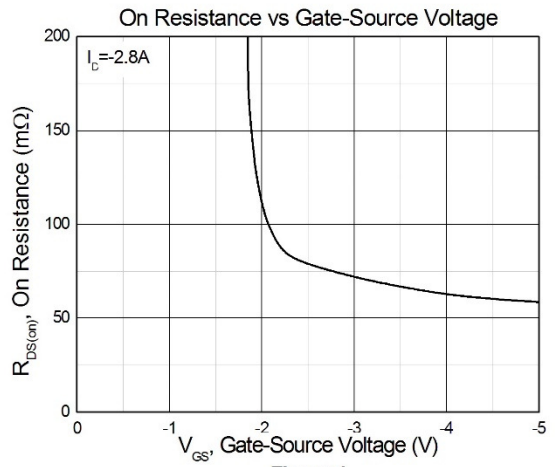


Figure 4

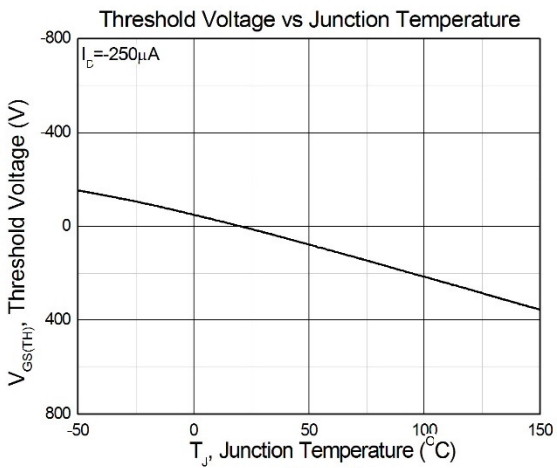


Figure 5

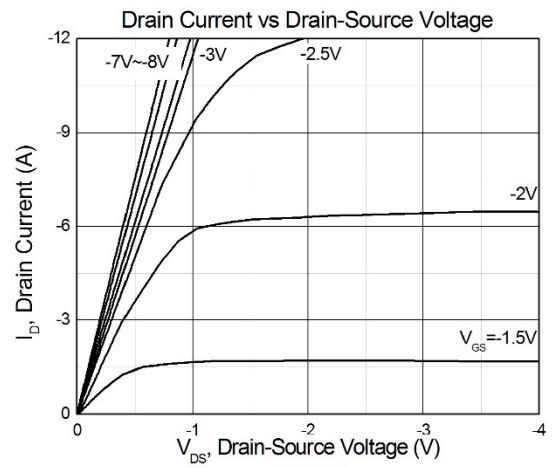
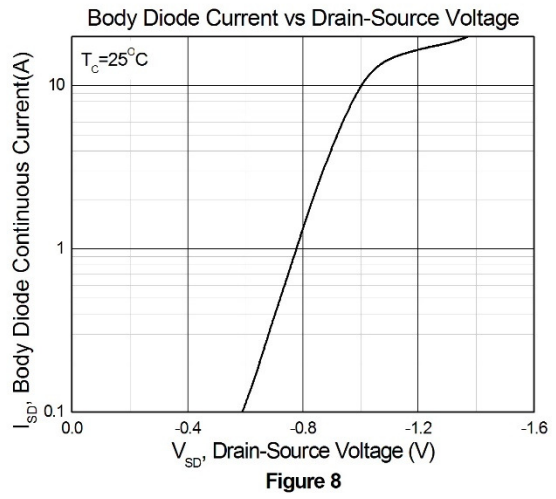
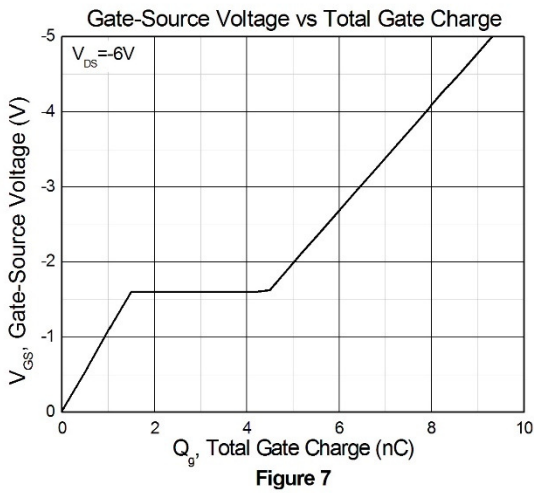


Figure 6





Test Circuits & Waveforms

Figure 9: Gate Charge Test Circuit

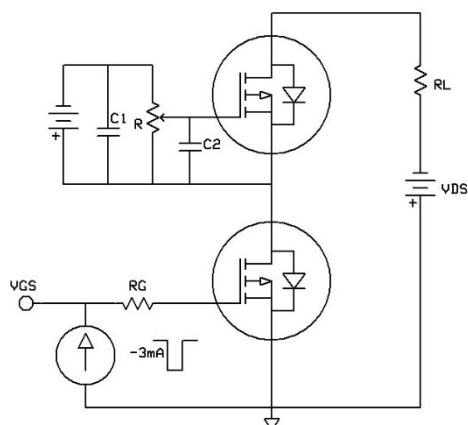


Figure 10: Gate Charge Waveform

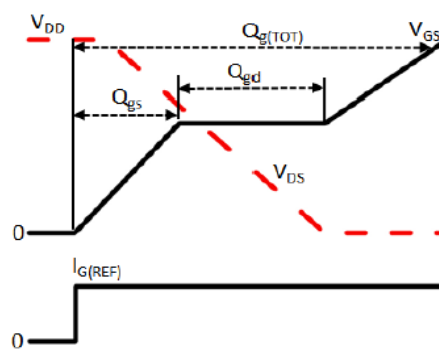


Figure 11: Switching Time Test Circuit

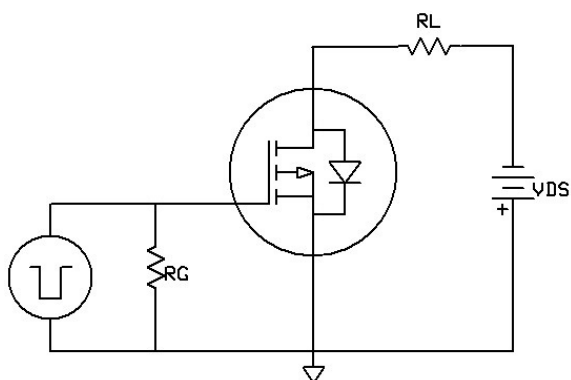
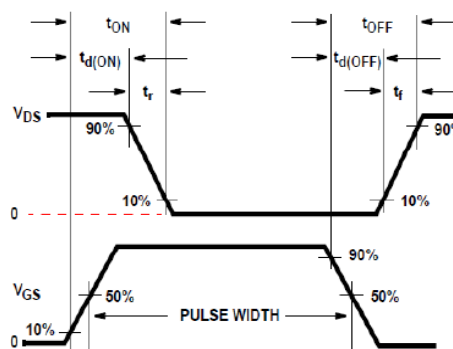
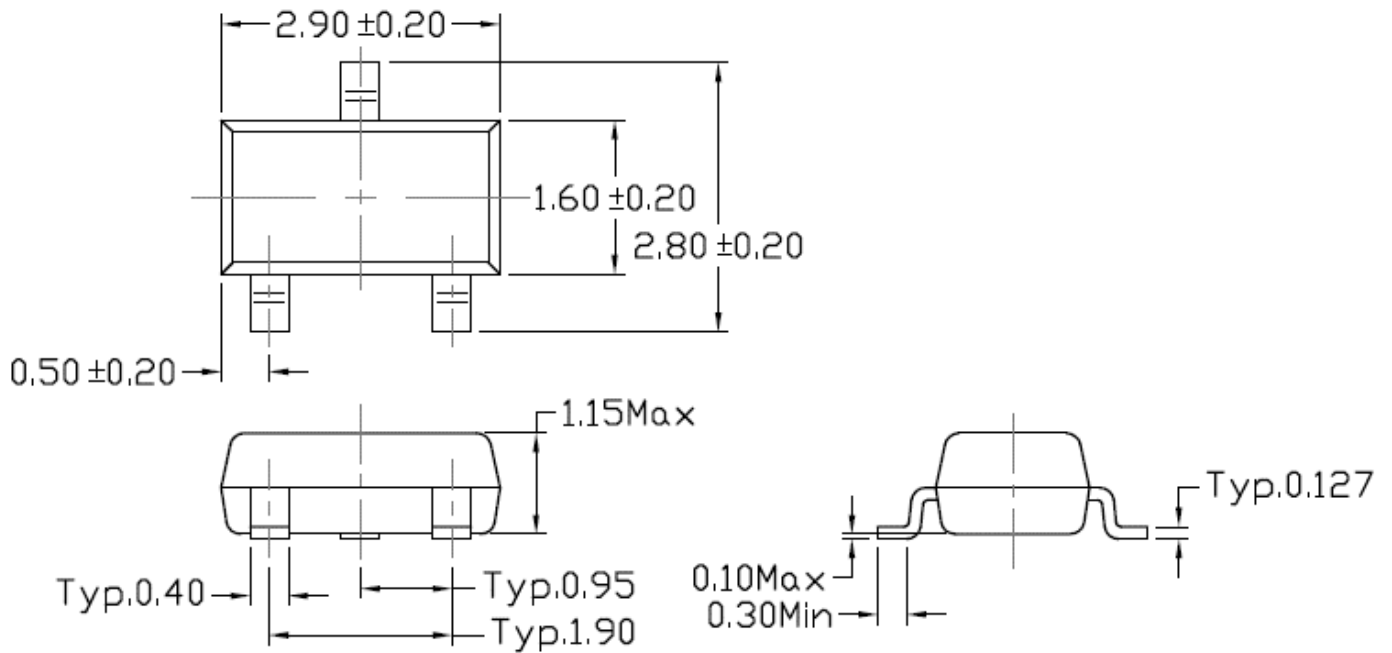


Figure 12: Switching Time Waveform



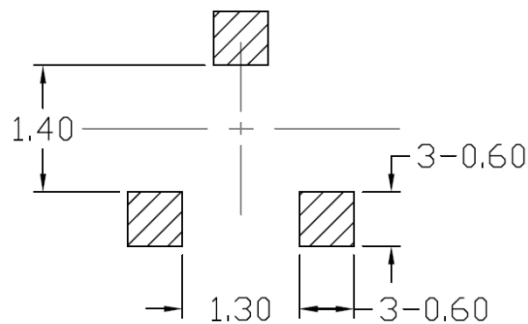


Package Dimension (SC-59)



Note: Dimensions in mm

Recommended pad layout for surface mount leadform



Note: Dimensions in mm

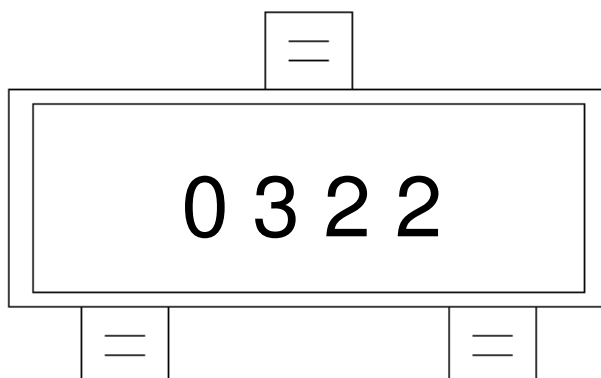




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### Marking Information



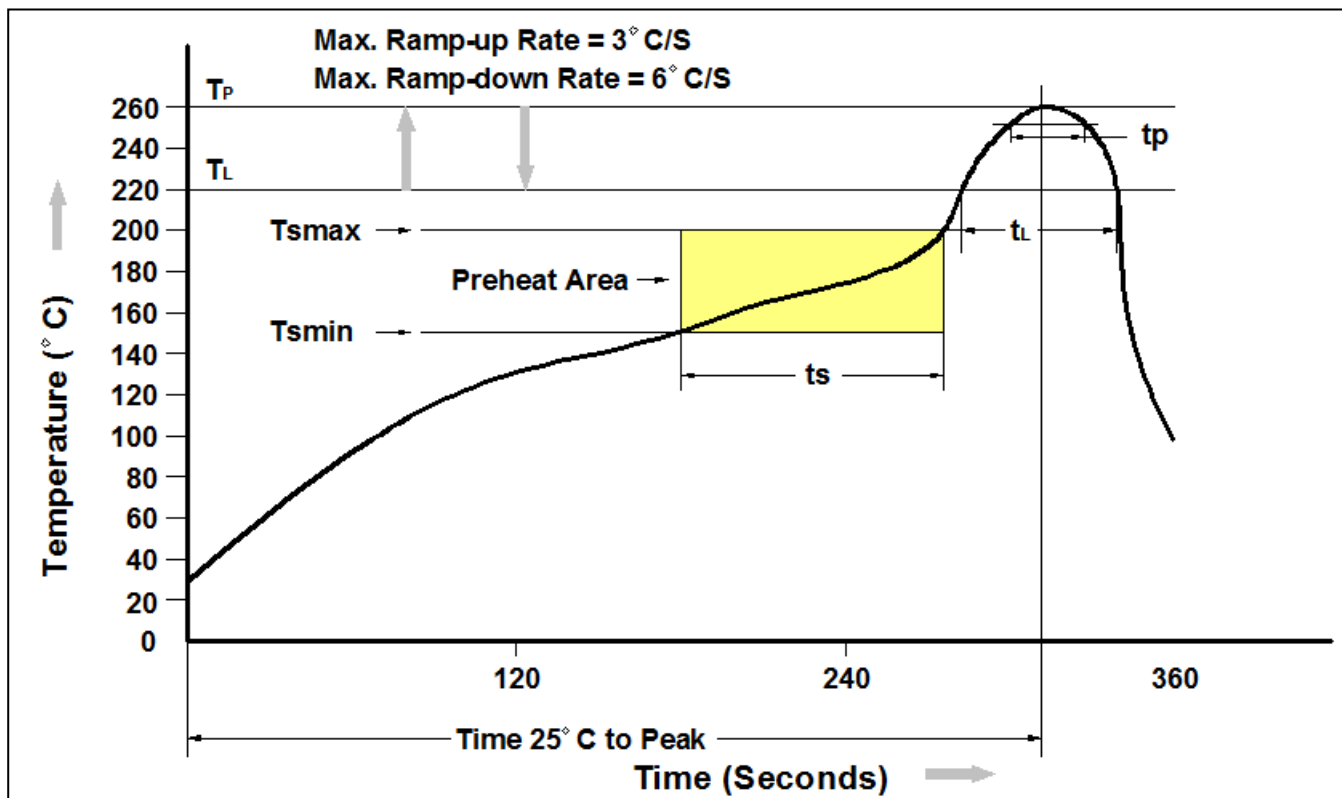
0322: Device Number

### Ordering Information

Part Number	Description	Quantity
CTL0322PS-R3	SC-59Reel	3000 pcs



Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (T <sub>smin</sub> )	150 °C
Temperature Max. (T <sub>smax</sub> )	200 °C
Time (t <sub>s</sub> ) from (T <sub>smin</sub> to T <sub>smax</sub> )	60-120 seconds
Ramp-up Rate (t <sub>L</sub> to t <sub>P</sub> )	3 °C/second max.
Liquidous Temperature (T <sub>L</sub> )	217 °C
Time (t <sub>L</sub> ) Maintained Above (T <sub>L</sub> )	60 – 150 seconds
Peak Body Package Temperature	260 °C +0 °C / -5 °C
Time (t <sub>P</sub> ) within 5 °C of 260 °C	30 seconds
Ramp-down Rate (T <sub>P</sub> to T <sub>L</sub> )	6 °C/second max
Time 25 °C to Peak Temperature	8 minutes max.



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