ADVANCE

S27KL0641, S27KS0641

HyperRAM™ Self-Refresh DRAM 3.0V/1.8V 64 Mb (8 MB)

Distinctive Characteristics

HyperBus™ Low Signal Count Interface

- 3.0V I/O, 11 bus signals
  – Single ended clock (CK)
- 1.8V I/O, 12 bus signals
  – Differential clock (CK, CK#)
- Chip Select (CS#)
- 8-bit data bus (DQ[7:0])
- Read-Write Data Strobe (RWDS)
  – Bidirectional Data Strobe / Mask
  – Output at the start of all transactions to indicate refresh latency
  – Output during read transactions as Read Data Strobe
  – Input during write transactions as Write Data Mask
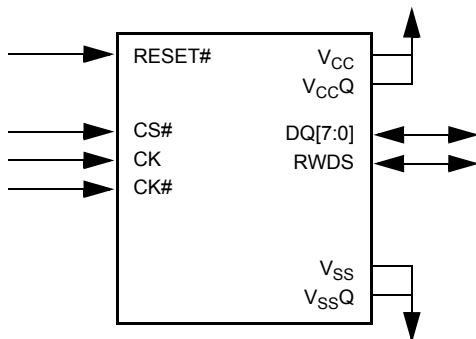
High Performance

- Up to 333MB/s
- Double-Data Rate (DDR) - two data transfers per clock
- 166-MHz clock rate (333 MB/s) at 1.8V V_{CC}
- 100-MHz clock rate (200 MB/s) at 3.0V V_{CC}
- Sequential burst transactions
- Configurable Burst Characteristics
  – Wrapped burst lengths:
    – 16 bytes (8 clocks)
    – 32 bytes (16 clocks)
    – 64 bytes (32 clocks)
    – 128 bytes (64 clocks)
  – Linear burst
  – Hybrid option - one wrapped burst followed by linear burst
  – Wrapped or linear burst type selected in each transaction
  – Configurable output drive strength
- Package and Die Options
  – 24-ball FBGA footprint

Performance Summary

Read Transaction Timings	
Maximum Clock Rate at 1.8V V_{CC}/V_{CC}Q	166 MHz
Maximum Clock Rate at 3.0V V_{CC}/V_{CC}Q	100 MHz
Maximum Access Time, (t_{ACC} at 166 MHz)	36 ns
Maximum CS# Access Time to first word at 166 MHz (excluding refresh latency)	56 ns

Maximum Current Consumption	
Burst Read or Write (linear burst at 166 MHz, 1.8V)	60 mA
Power On Reset	50 mA
Standby (CS# = High, 3V, 105 °C)	300 µA
Deep Power Down (CS# = High, 3V, 105 °C)	40 µA
Standby (CS# = High, 1.8V, 105 °C)	300 µA
Deep Power Down (CS# = High, 1.8V, 105 °C)	20 µA

Errata: For information on silicon errata, see "Errata" on page 27. Details include trigger conditions, devices affected, and proposed workaround.

Contents

1.   General Description

The Spansion HyperRAM™ family of products are high-speed CMOS, Self-refresh Dynamic RAM (DRAM) devices, with a HyperBus interface.

The Random Access Memory (RAM) array uses dynamic cells that require periodic refresh. Refresh control logic within the device manages the refresh operations on the RAM array when the memory is not being actively read or written by the HyperBus interface master (host). Since the host is not required to manage any refresh operations, the DRAM array appears to the host as though the memory uses static cells that retain data without refresh. Hence, the memory can also be described as Pseudo Static RAM (PSRAM).

Because the DRAM cells cannot be refreshed during a read or write transaction, there is a requirement that the host not perform read or write burst transfers that are long enough to block the necessary internal logic refresh operations when they are needed. The host is required to limit the duration of transactions and allow additional initial access latency, at the beginning of a new transaction, if the memory indicates a refresh operation is needed.

HyperBus is a low signal count, Double Data Rate (DDR) interface, that achieves high speed read and write throughput. The DDR protocol transfers two data bytes per clock cycle on the DQ input/output signals. A read or write transaction on HyperBus consists of a series of 16-bit wide, one clock cycle data transfers at the internal HyperRAM core with two corresponding 8-bit wide, one-half-clock-cycle data transfers on the DQ signals. All inputs and outputs are LV-CMOS compatible. Ordering Part Number (OPN) device versions are available for core (V_{CC}) and IO buffer ($V_{CC}Q$) supplies of either 1.8V or 3.0V (nominal).

Command, Address, and Data information is transferred over the eight HyperBus DQ signals. The clock is used for information capture by a HyperBus device when receiving Command-Address/Data on the DQ signals. Command-Address values are center aligned with clock edges.

The Read/Write Data Strobe (RWDS) is a bidirectional signal that indicates:

– when data will start to transfer from the memory to the host in read transactions (initial read latency),

– when data is being transferred from the memory to the host during read data transfers (source synchronous read data strobe),

– when data will start to transfer from the host to the memory in write transactions (initial write latency),

– and data masking during write data transfers.

During the command and address cycles of a read or write transaction, RWDS acts as an output from the memory to indicate whether additional initial access latency is needed to perform a dynamic memory refresh operation.

During read data transfers, RWDS is a read data strobe with data values edge aligned with the transitions of RWDS driven by the memory device.

During write data transfers, RWDS indicates whether a data byte is masked (prevented from changing the byte location in memory) or not masked (written to memory). Data masking may be used by the host to byte align write data within the memory or to enable merging of multiple non-word aligned writes in a single burst write. During write transactions, data is center aligned with the clock.
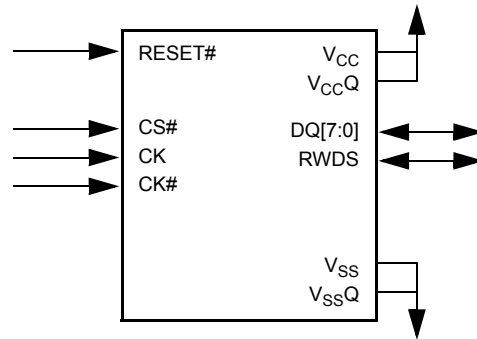
Read and write transactions are burst oriented, transferring the next sequential word during each clock cycle. Each individual read or write transaction can use either a wrapped or linear burst sequence. During wrapped transactions, accesses start at a selected location and continue to the end of a configured word group aligned boundary, then wrap to the beginning location in the group, then continue back to the starting location. Wrapped bursts are generally used for critical word first instruction or data cache line fill read accesses. During linear transactions, accesses start at a selected location and continue in a sequential manner until the transaction is terminated when CS# returns High. Linear transactions are generally used for large contiguous data transfers such as graphic image moves. Since each transaction command selects the type of burst sequence for that access, wrapped and linear burst transactions can be dynamically intermixed as needed.

For additional information on HyperBus interface operation, please refer to the HyperBus specification.

2. HyperRAM Product Overview

The HyperRAM Family consists of multiple density option, 1.8V or 3.0V core and I/O, synchronous self-refresh Dynamic RAM (DRAM) memory devices. This family provides a HyperBus slave interface to the host system. HyperBus has an 8 bit (1 byte) wide DDR data bus and uses only word-wide (16-bit data) address boundaries. Read transactions provide 16 bits of data during each clock cycle (8 bits on both clock edges). Write transactions take 16 bits of data from each clock cycle (8 bits on each clock edge).

Figure 2.1 HyperRAM Interface

Read and write transactions require two clock cycles to define the target row address and burst type, then an initial access latency of t_{ACC}. During the Command-Address (CA) part of a transaction, the memory will indicate whether an additional latency for a required refresh time (t_{RFH}) is added to the initial latency; by driving the RWDS signal to the High state. During the CA period the third clock cycle will specify the target word address within the target row. During a read (or write) transaction, after the initial data value has been output (or input), additional data can be read from (or written to) the row on subsequent clock cycles in either a wrapped or linear sequence. When configured in linear burst mode, the device will automatically fetch the next sequential row from the memory array to support a continuous linear burst. Simultaneously accessing the next row in the array while the read or write data transfer is in progress, allows for a linear sequential burst operation that can provide a sustained data rate of 333 MB/s (1 byte (8 bit data bus) * 2 *(data clock edges)* * 166 MHz = 333 MB/s).

3. HyperBus Interface

For the general description of how the HyperBus interface operates in HyperRAM memories, refer to the HyperBus specification. The following section describes HyperRAM device dependent aspects of HyperBus interface operation.

All bus transactions can be classified as either read or write. A bus transaction is started with CS# going Low with CK = Low and CK# = High. The transaction to be performed is presented to the HyperRAM device during the first three clock cycles in a DDR manner using all six clock edges. These first three clocks transfer three words of Command / Address (CA0, CA1, CA2) information to define the transaction characteristics:

- Read or write transaction

- Whether the transaction will be to the memory array or to register space.

- Whether a read transaction will use a linear or wrapped burst sequence

- The target half-page address (row and upper order column address)

- The target Word (within half-page) address (lower order column address)

Once the transaction has been defined, a number of idle clock cycles are used to satisfy initial read or write access latency requirements before data is transferred. During the Command-Address portion of all transactions, RWDS is used by the memory to indicate whether additional initial access latency will be inserted for a required refresh of the memory array.

When data transfer begins, read data is edge aligned with RWDS transitions or write data is center aligned with clock transitions. During read data transfer, RWDS serves as a source synchronous data timing strobe. During write data transfer, clock transitions provide the data timing reference and RWDS is used as a data mask. When RWDS is Low during a write data transfer, the data byte is written into memory; if RWDS is High during the transfer the byte is not written.

Data is transferred as 16-bit values with the first eight bits transferred on a High going CK (write data or CA bits) or RWDS edge (read data) and the second eight bits being transferred on the Low going CK or RWDS edge. Data transfers during read or write operations can be ended at any time by bringing CS# High when
CK = Low and CK# = High.

The clock may stop in the idle state while CS# is High.

The clock may also stop in the idle state for short periods while CS# is Low, as long as this does not cause a transaction to exceed the CS# maximum time low (t_{CSM}) limit. This is referred to as Active Clock Stop mode. In some HyperBus devices this mode is used for power reduction. However, due to the relatively short t_{CSM} period for completing each data transfer, the Active Clock Stop mode is generally not useful for power reduction but, may be used for short duration data flow control by the HyperBus master.

3.1 Command-Address Bit Assignments

Table 3.1 Command-Address Bit Definitions

CA Bit#	Bit Name	Bit Function
47	R/W#	Identifies the transaction as a read or write. R/W# = 1 indicates a Read transaction R/W# = 0 indicates a Write transaction
46	Address Space (AS)	Indicates whether the read or write transaction accesses the memory or register spaces. AS = 0 indicates memory space. AS = 1 indicates the register space. The register space is used to access device ID and Configuration registers.
45	Burst Type	Indicates whether the burst will be linear or wrapped. Burst Type = 0 indicates wrapped burst Burst Type = 1 indicates linear burst
44-35 (64 Mb)	Reserved	Reserved for future row address expansion. Reserved bits should be set to 0 by the HyperBus master.
34-22 (64 Mb)	Row Address	Row component of the target address: System word address bits A23-A9.
21-16	Upper Column Address	Upper Column component of the target address: System word address bits A8-A3.

Table 3.1 Command-Address Bit Definitions (Continued)

CA Bit#	Bit Name	Bit Function
15-3	Reserved	Reserved for future column address expansion. Reserved bits should be set to 0 by the HyperBus master.
2-0	Lower Column (word) Address	Lower Column component of the target address: System word address bits A2-0 selecting the starting word within a row.

3.2   Read Transactions

Table 3.2 Maximum Operating Frequency For Latency Code Options

Latency Code	Latency Clocks	Maximum Operating Frequency (MHz)
0000	5	133
0001	6	166
0010	Reserved	NA
0011	Reserved	NA
0100	Reserved	NA
0101	Reserved	NA
0110	Reserved	NA
0111	Reserved	NA
1000	Reserved	NA
1001	Reserved	NA
1010	Reserved	NA
1011	Reserved	NA
1100	Reserved	NA
1101	Reserved	NA
1110	3	83
1111	4	100

Note:
1. The Latency Code is the value loaded into Configuration Register bits CR0[7:4].

3.3   Write to Memory Space Transactions

When a linear burst write reaches the last address in the array, continuing the burst beyond the last address has undefined results.

4. Memory Space

When CA[46] is 0 a read or write transaction accesses the DRAM memory array.

Table 4.1 Memory Space Address Map

Unit Type	Count	System Word Address Bits	CA Bits	Notes
Rows within 64 Mb device	8192 (Rows)	A21 - A9	34 - 22	
Row	1 (row)	A8 - A3	21 - 16	512 (word addresses) 1 kbytes
Half-Page	8 (word addresses)	A2 - A0	2 - 0	16 bytes

5. Register Space

When CA[46] is 1 a read or write transaction accesses the Register Space.

Table 5.1 Register Space Address Map

Register	System Address	—	—	—	31-27	26-19	18-11	10-3	—	2-0
	CA Bits	47	46	45	44-40	39-32	31-24	23-16	15-8	7-0
Identification Register 0 (read only)	C0h or E0h				00h	00h	00h	00h	00h
Identification Register 1 (read only)	C0h or E0h				00h	00h	00h	00h	01h
Configuration Register 0 Read	C0h or E0h				00h	01h	00h	00h	00h
Configuration Register 0 Write	60h				00h	01h	00h	00h	00h
Configuration Register 1 Read	C0h or E0h				00h	01h	00h	00h	01h
Configuration Register 1 Write	60h				00h	01h	00h	00h	01h

Note:

1. CA45 may be either 0 or 1 for either wrapped or linear read. CA45 must be 1 as only linear single word register writes are supported.

5.1 Device Identification Registers

There are two read only, non-volatile, word registers, that provide information on the device selected when CS# is low. The device information fields identify:

- Manufacturer
- Type
- Density
  - Row address bit count
  - Column address bit count

Table 5.2 ID Register 0 Bit Assignments

Bits	Function	Settings (Binary)
15-14	Reserved	Reserved
13	Reserved	0 - default
12-8	Row Address Bit Count	00000 - One Row address bit ... 11111 - Thirty-two row address bits

Table 5.2 ID Register 0 Bit Assignments (Continued)

Bits	Function	Settings (Binary)
7-4	Column Address Bit Count	0000 - One column address bit ... 1111 - Sixteen column address bits
3-0	Manufacturer	0000 - Reserved 0001 - Spansion 0010 to 1111 - Reserved

Table 5.3 ID Register 1 Bit Assignments

| Bits	Function	Settings (Binary)
15-4	Reserved	0000_0000_0000b (default)
3-0	Device Type	0000 - HyperRAM 0001 to 1111 - Reserved

5.1.1   Density and Row Boundaries

The DRAM array size (density) of the device can be determined from the total number of system address bits used for the row and column addresses as indicated by the Row Address Bit Count and Column Address Bit Count fields in the ID0 register. For example: a 64 Mbit HyperRAM has 9 column address bits and 13 row address bits for a total of 22 word address bits = 2^{22} = 4 Mwords = 8 Mbytes. The 9 column address bits indicate that each row holds 2^9 = 512 words = 1 kbytes. The row address bit count indicates there are 8196 rows to be refreshed within each array refresh interval. The row count is used in calculating the refresh interval.

5.2   Register Space Access

Register default values are loaded upon power-up or hardware reset. The registers can be altered at any time while the device is in the standby state.

Loading a register is accomplished with a single 16-bit word write transaction as shown in Figure 5.1. CA[47] is zero to indicate a write transaction, CA[46] is a one to indicate a register space write, CA[45] is a one to indicate a linear write, lower order bits in the CA field indicate the register address.

Figure 5.1 Loading a Register

Host drives DQ[7:0] with Command-Address and Register Data
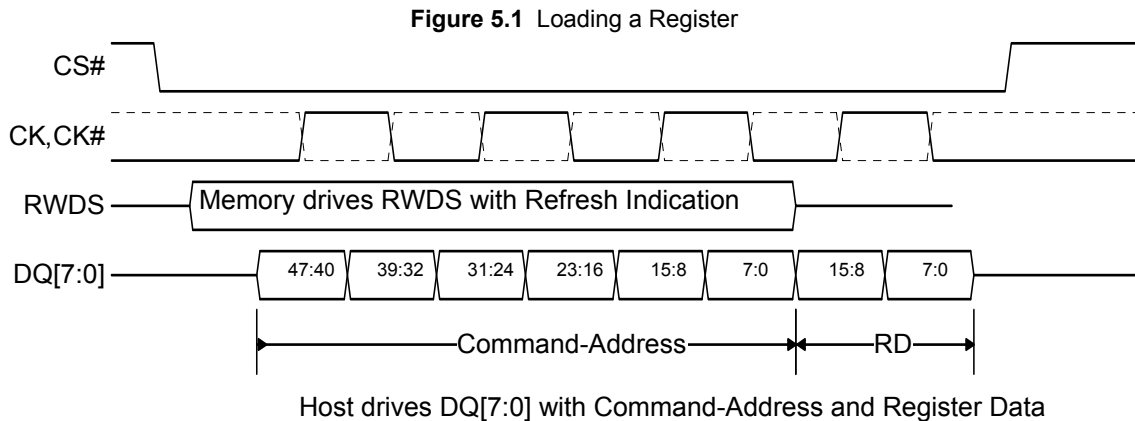
Notes:

1. The host must not drive RWDS during a write to register space.

2. The RWDS signal is driven by the memory during the Command-Address period based on whether the memory array is being refreshed. This refresh indication does not affect the writing of register data. RWDS is driven immediately after CS# goes low, before CA[47:46] are received to indicate that the transaction is a write to register space, for which the RWDS refresh indication is not relevant.

3. The register value is always provided immediately after the CA value and is not delayed by a refresh latency.

4. The the RWDS signal returns to high impedance after the Command-Address period. Register data is never masked. Both data bytes of the register data are loaded into the selected register.

Each register is written with a separate single word write transaction. Register write transactions have zero latency, the single word of data immediately follows the Command-Address. RWDS is not driven by the host during the write because RWDS is always driven by the memory during the CA cycles to indicate whether a memory array refresh is in progress. Because a register space write goes directly to a register, rather than the memory array, there is no initial write latency, related to an array refresh that may be in progress. In a register write, RWDS is also not used as a data mask because both bytes of a register are always written and never masked.

Reserved register fields must be written with their default value. Writing reserved fields with other than default values may produce undefined results.

Reading of a register is accomplished with a single 16 bit read transaction with CA[46]=1 to select register space. If more than one word is read, the same register value is repeated in each word read. The CA[45] burst type is "don't care" because only a single register value is read. The contents of the register is returned in the same manner as reading array data, with one or two latency counts, based on the state of RWDS during the Command-Address period. The latency count is defined in the Configuration Register 0 Read Latency field (CR0[7:4]).

5.2.1 Configuration Register 0

Configuration Register 0 (CR0) is used to define the power mode and access protocol operating conditions for the HyperRAM device. Configurable characteristics include:

- Wrapped Burst Length (16, 32, 64, or 128-byte aligned and length data group)
- Wrapped Burst Type
– Legacy wrap (sequential access with wrap around within a selected length and aligned group)
– Hybrid wrap (Legacy wrap once then linear burst at start of the next sequential group)
- Initial Latency
- Variable Latency
– Whether an array read or write transaction will use fixed or variable latency. If fixed latency is selected the memory will always indicate a refresh latency and delay the read data transfer accordingly. If variable latency is selected, latency for a refresh is only added when a refresh is required at the same time a new transaction is starting.
- Output Drive Strength
- Deep Power Down Mode

Table 5.4 Configuration Register 0 Bit Assignments

CR0 Bit	Function	Settings (Binary)
15	Deep Power Down Enable	1 - Normal operation (default) 0 - Writing 0 to CR[15] causes the device to enter Deep Power Down
14-12	Drive Strength	000 - 34 ohms (default) 001 - 115 ohms 010 - 67 ohms 011 - 46 ohms 100 - 34 ohms 101 - 27 ohms 110 - 22 ohms 111 - 19 ohms
11-8	Reserved	1 - Reserved (default) Reserved for Future Use. When writing this register, these bits should be set to 1 for future compatibility.

Table 5.4 Configuration Register 0 Bit Assignments (Continued)

CR0 Bit	Function	Settings (Binary)
7-4	Initial Latency	0000 - 5 Clock Latency 0001 - 6 Clock Latency (default) 0010 - Reserved 0011 - Reserved 0100 - Reserved ... 1101 - Reserved 1110 - 3 Clock Latency 1111 - 4 Clock Latency
3	Fixed Latency Enable	0 - Variable Latency - 1 or 2 times Initial Latency depending on RWDS during CA cycles. 1 - Fixed 2 times Initial Latency (default)
2	Hybrid Burst Enable	0: Wrapped burst sequences to follow hybrid burst sequencing 1: Wrapped burst sequences in legacy wrapped burst manner (default)
1-0	Burst Length	00 - 128 bytes 01 - 64 bytes 10- 16 bytes 11 - 32 bytes (default)

5.2.1.1 Wrapped Burst

A wrapped burst transaction accesses memory within a group of words aligned on a word boundary matching the length of the configured group. Wrapped access groups can be configured as 16, 32, 64, or 128 bytes alignment and length. During wrapped transactions, access starts at the Command-Address selected location within the group, continues to the end of the configured word group aligned boundary, then wraps around to the beginning location in the group, then continues back to the starting location. Wrapped bursts are generally used for critical word first instruction or data cache line fill read accesses.

5.2.1.2 Hybrid Burst

The beginning of a hybrid burst will wrap within the target address wrapped burst group length before continuing to the next half-page of data beyond the end of the wrap group. Continued access is in linear burst order until the transfer is ended by returning CS# high. This hybrid of a wrapped burst followed by a linear burst starting at the beginning of the next burst group, allows multiple sequential address cache lines to be filled in a single access. The first cache line is filled starting at the critical word. Then the next sequential line in memory can be read in to the cache while the first line is being processed.

Table 5.5 CR0[2] Control of Wrapped Burst Sequence

Bit	Default Value	Name
2	1	Hybrid Burst Enable CR[2]= 0: Wrapped burst sequences to follow hybrid burst sequencing CR[2]= 1: Wrapped burst sequences in legacy wrapped burst manner

.

Table 5.6 Example Wrapped Burst Sequences

Burst Selection		Burst Type	Wrap Boundary (bytes)	Start Address (Hex)	Address Sequence (Hex) (Words)
CA[45]	CR0[2:0]				
0	000	Hybrid 128	128 Wrap once then Linear	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02 (wrap complete, now linear beyond the end of the initial 128 byte wrap group) 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 4A, 4B, 4C, 4D, 4E, 4F, 50, 51, ...
0	001	Hybrid 64	64 Wrap once then Linear	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, (wrap complete, now linear beyond the end of the initial 64 byte wrap group) 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, ...
0	001	Hybrid 64	64 Wrap once then Linear	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, (wrap complete, now linear beyond the end of the initial 64 byte wrap group) 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 4A, 4B, 4C, 4D, 4E, 4F, 50, 51, ...
0	010	Hybrid 16	16 Wrap once then Linear	XXXXXX02	02, 03, 04, 05, 06, 07, 00, 01, (wrap complete, now linear beyond the end of the initial 16 byte wrap group) 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, ...
0	010	Hybrid 16	16 Wrap once then Linear	XXXXXX0C	0C, 0D, 0E, 0F, 08, 09, 0A, 0B, (wrap complete, now linear beyond the end of the initial 16 byte wrap group) 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, ...
0	011	Hybrid 32	32 Wrap once then Linear	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, ...
0	011	Hybrid 32	32 Wrap once then Linear	XXXXXX1E	1E, 1F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, ...
0	100	Wrap 128	128	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02, ...
0	101	Wrap 64	64	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, ...
0	101	Wrap 64	64	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, ...
0	110	Wrap 16	16	XXXXXX02	02, 03, 04, 05, 06, 07, 00, 01, ...
0	110	Wrap 16	16	XXXXXX0C	0C, 0D, 0E, 0F, 08, 09, 0A, 0B, ...
0	111	Wrap 32	32	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, ...

Table 5.6 Example Wrapped Burst Sequences (Continued)

Burst Selection		Burst Type	Wrap Boundary (bytes)	Start Address (Hex)	Address Sequence (Hex) (Words)
CA[45]	CR0[2:0]				
0	111	Wrap 32	32	XXXXXX1E	1E, 1F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, ...
1	XXX	Linear	Linear Burst	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, ...

5.2.1.3   Initial Latency

Memory Space read and write transactions or Register Space read transactions require some initial latency to open the row selected by the Command-Address. This initial latency is t_{ACC}. The number of latency clocks needed to satisfy t_{ACC} depends on the HyperBus frequency and can vary from 3 to 6 clocks. The value in CR0[7:4] selects the number of clocks for initial latency. The default value is 6 clocks, allowing for operation up to a maximum frequency of 166MHz prior to the host system setting a lower initial latency value that may be more optimal for the system.

In the event a distributed refresh is required at the time a Memory Space read or write transaction or Register Space read transaction begins, the RWDS signal goes high during the Command-Address to indicate that an additional initial latency is being inserted to allow a refresh operation to complete before opening the selected row.

Register Space write transactions always have zero initial latency. RWDS may be High or Low during the Command-Address period. The level of RWDS during the Command-Address period does not affect the placement of register data immediately after the Command-Address, as there is no initial latency needed to capture the register data. A refresh operation may be performed in the memory array in parallel with the capture of register data.

5.2.1.4   Fixed Latency

A configuration register option bit CR0[3] is provided to make all Memory Space read and write transactions or Register Space read transactions require the same initial latency by always driving RWDS high during the Command-Address to indicate that two initial latency periods are required. This fixed initial latency is independent of any need for a distributed refresh, it simply provides a fixed (deterministic) initial latency for all of these transaction types. The fixed latency option may simplify the design of some HyperBus memory controllers or ensure deterministic transaction performance. Fixed latency is the default POR or reset configuration. The system may clear this configuration bit to disable fixed latency and allow variable initial latency with RWDS driven high only when additional latency for a refresh is required.

5.2.1.5   Drive Strength

DQ signal line loading, length, and impedance vary depending on each system design. Configuration register bits CR0[14:12] provide a means to adjust the DQ[7:0] signal output impedance to customize the DQ signal impedance to the system conditions to minimize high speed signal behaviors such as overshoot, undershoot, and ringing. The default POR or reset configuration value is 000b to select the mid point of the available output impedance options.

The impedance values shown are typical for both pull-up and pull-down drivers at typical silicon process conditions, nominal operating voltage (1.8Vor 3V) and 50°C. The impedance values may vary by up to ±80% from the typical values depending on the Process, Voltage, and Temperature (PVT) conditions. Impedance will increase with slower process, lower voltage, or higher temperature. Impedance will decrease with faster process, higher voltage, or lower temperature.

Each system design should evaluate the data signal integrity across the operating voltage and temperature ranges to select the best drive strength settings for the operating conditions.

5.2.1.6 Deep Power Down

When the HyperRAM device is not needed for system operation, it may be placed in a very low power consuming mode called Deep Power Down (DPD), by writing 0 to CR0[15]. When CR0[15] is cleared to 0, the device enters the DPD mode within t_{DPDIN} time and all refresh operations stop. The data in RAM is lost, (becomes invalid without refresh) during DPD mode. The next access to the device driving CS# Low then High, POR, or a reset will cause the device to exit DPD mode. Returning to Standby mode requires t_{DPDOUT} time. For additional details see Section 6.1.3, Deep Power Down on page 15.

5.2.2 Configuration Register 1

Configuration Register 1 (CR1) is used to define the distributed refresh interval for this HyperRAM device. The core DRAM array requires periodic refresh of all bits in the array. This can be done by the host system by reading or writing a location in each row within a specified time limit. The read or write access copies a row of bits to an internal buffer. At the end of the access the bits in the buffer are written back to the row in memory, thereby recharging (refreshing) the bits in the row of DRAM memory cells.

However, the host system generally has better things to do than to periodically read every row in memory and keep track that each row is visited within the required refresh interval for the entire memory array. The HyperRAM family devices include self-refresh logic that will refresh rows automatically so that the host system is relieved of the need to refresh the memory. The automatic refresh of a row can only be done when the memory is not being actively read or written by the host system. The refresh logic waits for the end of any active read or write before doing a refresh, if a refresh is needed at that time. If a new read or write begins before the refresh is completed, the memory will drive RWDS high during the Command-Address period to indicate that an additional initial latency time is required at the start of the new access in order to allow the refresh operation to complete before starting the new access.

The required refresh interval for the entire memory array varies with temperature as shown in Table 5.7, Array Refresh Interval per Temperature on page 13. This is the time within which all rows must be refreshed. Refresh of all rows could be done as a single batch of accesses at the beginning of each interval, in groups (burst refresh) of several rows at a time, spread throughout each interval, or as single row refreshes evenly distributed throughout the interval. The self-refresh logic distributes single row refresh operations throughout the interval so that the memory is not busy doing a burst of refresh operations for a long period, such that the burst refresh would delay host access for a long period.

Table 5.7 Array Refresh Interval per Temperature

Device Temperature (°C)	Array Refresh Interval (ms)	Array Rows	Recommended t_{CMS} (µs)
85	64	8192	4
105	16	8192	1

Table 5.8 Configuration Register 1 Bit Assignments

CR1 Bit	Function	Settings (Binary)
15-2	Reserved	000000h — Reserved (default) Reserved for Future Use. When writing this register, these bits should be cleared to 0 for future compatibility.

1-0	Distributed Refresh Interval	10b — default
		    4 µs for Industrial temperature range devices
		    1 µs for Industrial Plus temperature range devices
		11b — 1.5 times default
		00b — 2 times default
		01b — 4 times default

The distributed refresh method requires that the host does not do burst transactions that are so long as to prevent the memory from doing the distributed refreshes when they are needed. This sets an upper limit on the length of read and write transactions so that the refresh logic can insert a refresh between transactions. This limit is called the CS# low maximum time (t_{CMS}). The t_{CMS} value is determined by the array refresh interval divided by the number of rows in the array, then reducing this calculation by half to ensure that a distributed refresh interval cannot be entirely missed by a maximum length host access starting immediately before a distributed refresh is needed. Because t_{CMS} is set to half the required distributed refresh interval, any series of maximum length host accesses that delay refresh operations will be catching up on refresh operations at twice the rate required by the refresh interval divided by the number of rows.

The host system is required to respect the t_{CMS} value by ending each transaction before violating t_{CMS}. This can be done by host memory controller logic splitting long transactions when reaching the t_{CMS} limit, or by host system hardware or software not performing a single read or write transaction that would be longer than t_{CMS}.

As noted in Table 5.7, Array Refresh Interval per Temperature on page 13 the array refresh interval is longer at lower temperatures such that t_{CMS} could be increased to allow longer transactions. The host system can either use the t_{CMS} value from the table for the maximum operating temperature or, may determine the current operating temperature from a temperature sensor in the system in order to set a longer distributed refresh interval.

The host system may also effectively increase the t_{CMS} value by explicitly taking responsibility for performing all refresh and doing burst refresh reading of multiple sequential rows in order to catch up on distributed refreshes missed by longer transactions.

HyperRAM Hardware Interface

For the general description of the HyperBus hardware interface of HyperFlash memories refer to the HyperBus Specification. The following section describes HyperRAM device dependent aspects of hardware interface.

6.   Interface States

6.1   Power Conservation Modes

6.1.1   Interface Standby

Standby is the default, low power, state for the interface while the device is not selected by the host for data transfer (CS#= High). All inputs, and outputs other than CS# and RESET# are ignored in this state.

6.1.2   Active Clock Stop

The Active Clock Stop mode reduces device interface energy consumption to the I_{CC6} level during the data transfer portion of a read or write operation. The device automatically enables this mode when clock remains stable for t_{ACC} + 30 ns. While in Active Clock Stop mode, read data is latched and always driven onto the data bus. I_{CC6} shown in Section 7.4, DC Characteristics on page 18.

Active Clock Stop mode helps reduce current consumption when the host system clock has stopped to pause the data transfer. Even though CS# may be Low throughout these extended data transfer cycles, the memory device host interface will go into the Active Clock Stop current level at t_{ACC} + 30 ns. This allows the device to transition into a lower current mode if the data transfer is stalled. Active read or write current will resume once the data transfer is restarted with a toggling clock. The Active Clock Stop mode must not be used in violation of the t_{CSM} limit. CS# must go high before t_{CSM} is violated.

6.1.3   Deep Power Down

In the Deep Power Down (DPD) mode, current consumption is driven to the lowest possible level (i_{DPD}). DPD mode is entered by writing a 0 to CR0[15]. The device reduces power within t_{DPDIN} time and all refresh operations stop. The data in Memory Space is lost, (becomes invalid without refresh) during DPD mode. The next access to the device, driving CS# Low then High, will cause the device to exit DPD mode. A read or write transaction used to drive CS# Low then High to exit DPD mode is a dummy transaction that is ignored by the device. Also, POR, or a hardware reset will cause the device to exit DPD mode. Only the CS# and RESET# signals are monitored during DPD mode. Returning to Standby mode following a dummy transaction or reset requires t_{DPDOUT} time. Returning to Standby mode following a POR requires t_{VCS} time, as with any other POR. Following the exit from DPD due to any of these events, the device is in the same state as following POR.

Table 6.1 Deep Power Down Timing Parameters

Parameter	Description	Min	Max	Unit
t_{DPDIN}	Deep Power Down CR0[15]=0 register write to DPD power level	10	–	µs
t_{DPDCSL}	Length of CS# Low period to cause an exit from Deep Power Down	200	–	ns
t_{DPDOUT}	CS# Low then High to Standby wakeup time	–	150	µs

Figure 6.1 Deep Power Down Entry Timing
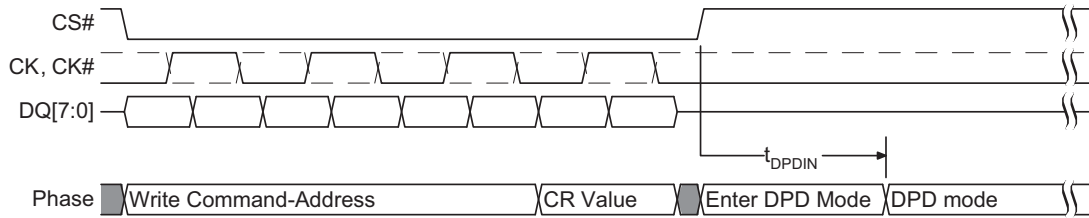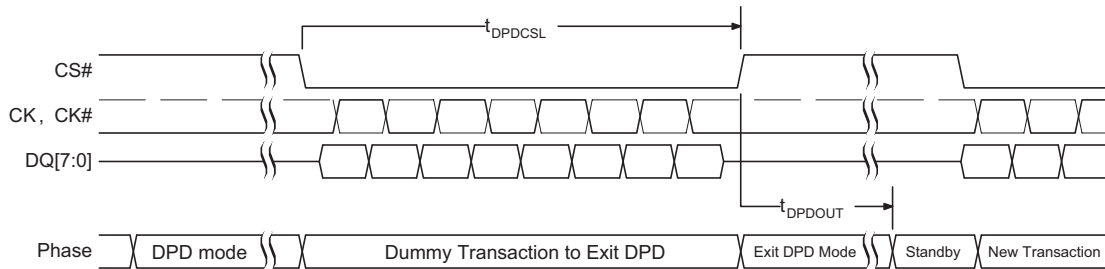

Figure 6.2 Deep Power Down CS# Exit Timing

7. Electrical Specifications

7.1 Absolute Maximum Ratings

Storage Temperature Plastic Packages	−65 °C to +150 °C
Ambient Temperature with Power Applied	−65°C to +115 °C
Voltage with Respect to Ground	
All signals (1)	−0.5V to +(V$_{CC}$ + 0.5V)
Output Short Circuit Current (2)	100 mA
V$_{CC}$	−0.5V to +4.0V

Notes:

1. Minimum DC voltage on input or I/O signal is −1.0V. During voltage transitions, input or I/O signals may undershoot V$_{SS}$ to -1.0V for periods of up to 20 ns. See Figure 7.1. Maximum DC voltage on input or I/O signals is V$_{CC}$ +1.0V. During voltage transitions, input or I/O signals may overshoot to V$_{CC}$ +1.0V for periods up to 20 ns. See Figure 7.2.

2. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

3. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

7.1.1 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between V$_{SS}$ and V$_{DD}$. During voltage transitions, inputs or I/Os may overshoot V$_{SS}$ to −1.0V or overshoot to V$_{DD}$ +1.0V, for periods up to 20 ns.

Figure 7.1 Maximum Negative Overshoot Waveform
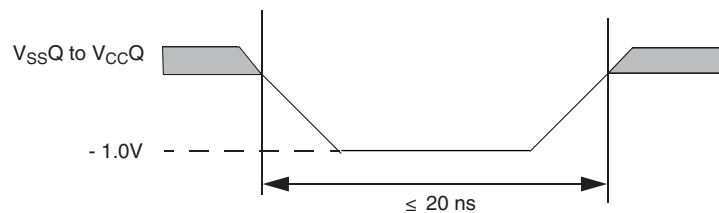
Figure 7.2 Maximum Positive Overshoot Waveform
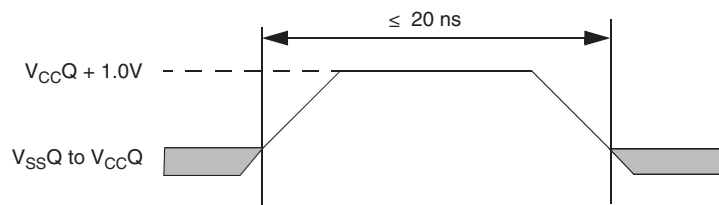
7.2   Latchup Characteristics

Table 7.1 Latchup Specification

Description	Min	Max	Unit
Input voltage with respect to $V_{SS}Q$ on all input only connections	−1.0	V_{CCQ} + 1.0	V
Input voltage with respect to $V_{SS}Q$ on all I/O connections	−1.0	V_{CCQ} + 1.0	V
V_{CCQ} Current	−100	+100	mA

Note:
1. Excludes power supplies V_{CC}/V_{CCQ}. Test conditions: V_{CC} = V_{CCQ} = 1.8 V, one connection at a time tested, connections not being tested are at V_{SS}.

7.3   Operating Ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

7.3.1   Temperature Ranges

Ambient Temperature (T_A)

Industrial	−40 °C to +85 °C
Industrial Plus	−40 °C to +105 °C

7.3.2   1.8V Power Supply Voltages

V_{CC} and V_{CCQ} 1.7V to 1.95V

7.3.3   3.0V Power Supply Voltages

V_{CC} and V_{CCQ} 2.7V to 3.6V

7.4   DC Characteristics

Table 7.2 DC Characteristics (CMOS Compatible)

Parameter	Description	Test Conditions	Min	Typ (1)	Max	Unit
I_{LI}	Input Leakage Current 3V Device Reset Signal High Only	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max	–	–	−0.1	µA
I_{LI}	Input Leakage Current 1.8V Device Reset Signal High Only	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max	–	–	−0.1	µA
I_{LI}	Input Leakage Current 3V Device Reset Signal Low Only (2)	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max	–	–	+20.0	µA
I_{LI}	Input Leakage Current 1.8V Device Reset Signal Low Only (2)	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} max	–	–	+20.0	µA
I_{CC1}	V_{CC} Active Read Current	CS# = V_{IL}, @166 MHz, V_{CC} = 1.9V	– / –	20	60	mA
		CS# = V_{IL}, @100 MHz, V_{CC} = 3.6V	–	20	35	mA
I_{CC2}	V_{CC} Active Write Current	CS# = V_{IL}, @166 MHz, V_{CC} = 1.9V	– / –	15	60	mA
		CS# = V_{IL}, @100 MHz, V_{CC} = 3.6V	–	15	35	mA

Table 7.2 DC Characteristics (CMOS Compatible) (Continued)

Parameter	Description	Test Conditions	Min	Typ (1)	Max	Unit
I_{CC4I}	V_{CC} Standby Current for Industrial (−40 °C to +85 °C)	CS#, V_{CC} = V_{CC} max,	–	135	200	µA
I_{CC4IP}	V_{CC} Standby Current for Industrial Plus (−40 °C to +105 °C)	CS#, V_{CC} = V_{CC} max	–	135	300	µA
I_{CC5}	Reset Current	CS# = V_{IH}, RESET# = V_{IL}, V_{CC} = V_{CC} max	–	10	20	mA
I_{CC6I}	Active Clock Stop Current for Industrial (−40 °C to +85 °C)	CS# = V_{IL}, RESET# = V_{IH}, V_{CC} = V_{CC} max	–	5.3	8	mA
I_{CC6IP}	Active Clock Stop Current for Industrial Plus(−40 °C to +105 °C)	CS# = V_{IL}, RESET# = V_{IH}, V_{CC} = V_{CC} max	–	5.3	12	mA
I_{CC7}	V_{CC} Current during power up (1)	CS#, = H, V_{CC} = V_{CC} max, V_{CC} = V_{CC}Q = *1.95V or 3.6V* (Note 7.4.1)	–	–	35	mA
I_{DPD}	Deep Power Down Current 3V 85°C	CS#, V_{CC} = 3.6V, T_A = 85 °C	–	–	20	µA
I_{DPD}	Deep Power Down Current 1.8V 85°C	CS#, V_{CC} = 1.9V, T_A = 85 °C	–	–	10	µA
I_{DPD}	Deep Power Down Current 3V 105°C	CS#, V_{CC} = 3.6V, T_A = 105 °C	–	–	40	µA
I_{DPD}	Deep Power Down Current 1.8V 105°C	CS#, V_{CC} = 1.9V, T_A = 105 °C	–	–	20	µA

Note:

1. Not 100% tested.

2. RESET# low initiates exits from DPD mode and initiates the draw of I_{CC5} reset current, making I_{LI} during Reset# Low insignificant.

7.4.1 Capacitance Characteristics

Table 7.3 1.8V Capacitive Characteristics

Description	Parameter	Min	Max	Unit
Input Capacitance (CK, CK#, CS#)	CI	3	4.5	pF
Delta Input Capacitance (CK, CK#)	CID	–	0.25	pF
Output Capacitance (RWDS)	CO	3	4	pF
IO Capacitance (DQx)	CIO	3	4	pF
IO Capacitance Delta (DQx)	CIOD	–	0.5	pF

Notes:

1. These values are guaranteed by design and are tested on a sample basis only.

2. Contact capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. $V_{CC,}$ V_{CC}Q are applied and all other signals (except the signal under test) floating. DQ's should be in the high impedance state.

3. Note that the capacitance values for the CK, CK#, RWDS and DQx signals must have similar capacitance values to allow for signal propagation time matching in the system. The capacitance value for CS# is not as critical because there are no critical timings between CS# going active (Low) and data being presented on the DQs bus.

Table 7.4 3.0V Capacitive Characteristics

Description	Parameter	Min	Max	Unit
Input Capacitance (CK, CS#)	CI	3	4.5	pF
Output Capacitance (RWDS)	CO	3	4	pF
IO Capacitance (DQx)	CIO	3	4	pF
IO Capacitance Delta (DQx)	CIOD	–	0.5	pF

Notes:

1. These values are guaranteed by design and are tested on a sample basis only.
2. Contact capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. V_{CC}, $V_{CC}Q$ are applied and all other signals (except the signal under test) floating. DQ's should be in the high impedance state.
3. Note that the capacitance values for the CK, RWDS and DQx signals must have similar capacitance values to allow for signal propagation time matching in the system. The capacitance value for CS# is not as critical because there are no critical timings between CS# going active (Low) and data being presented on the DQs bus.

7.5   Power-Up Initialization

HyperRAM Family products include an on-chip voltage sensor used to launch the power-up initialization process. V_{CC} and $V_{CC}Q$ must be applied simultaneously. When the power supply reaches a stable level at or above V_{CC}(min), the device will require t_{VCS} time to complete its self-initialization process.

The device must not be selected during power-up. CS# must follow the voltage applied on $V_{CC}Q$ until V_{CC} (min) is reached during power-up, and then CS# must remain high for a further delay of t_{VCS}. A simple pull-up resistor from $V_{CC}Q$ to Chip Select (CS#) can be used to insure safe and proper power-up.

If RESET# is Low during power up, the device delays start of the t_{VCS} period until RESET# is High. The t_{VCS} period is used primarily to perform refresh operations on the DRAM array to initialize it.

When initialization is complete, the device is ready for normal operation.

Figure 7.3 Power-up with RESET# High

Figure 7.4 Power-up with RESET# Low
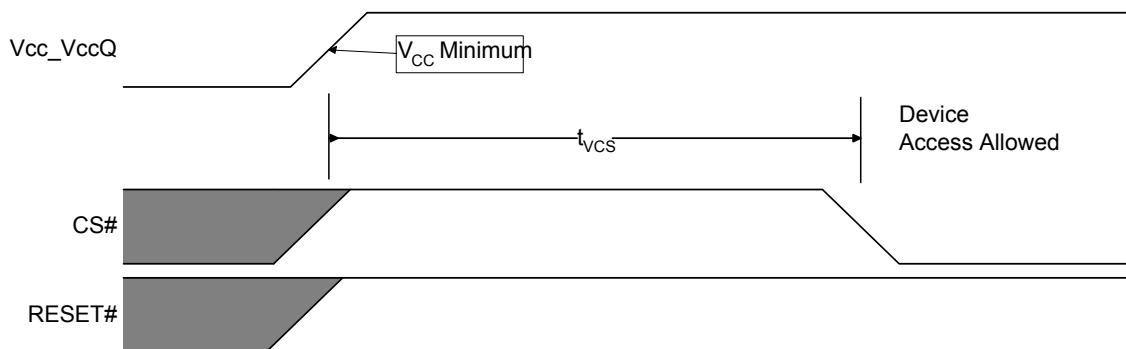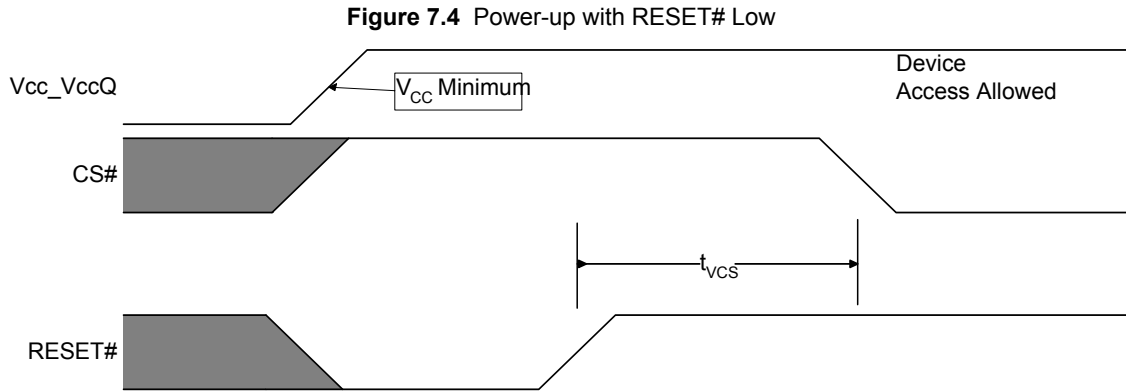
Table 7.5 Power Up and Reset Parameters

Parameter	Description	Min	Max	Unit
V_{CC}	1.8V V_{CC} Power Supply	1.7	1.95	V
V_{CC}	3V V_{CC} Power Supply	2.7	3.6	V
t_{VCS}	V_{CC} and $V_{CC}Q \geq$ minimum and RESET# High to first access	–	150	µs

Notes:

1. Bus transactions (read and write) are not allowed during the power-up reset time (t_{VCS}).

2. $V_{CC}Q$ must be the same voltage as V_{CC}.

3. V_{CC} ramp rate may be non-linear.

7.6   Power Down

For the general description of the HyperBus interface power down specifications refer to the HyperBus Specification. The following section describes HyperRAM device dependent aspects of power down specifications.

Table 7.6 1.8V Power-Down Voltage and Timing

Symbol	Parameter	Min	Max	Unit
V_{CC}	V_{CC} Power Supply	1.7	1.95	V
V_{LKO}	V_{CC} Lock-out below which re-initialization is required	1.7	–	V
V_{RST}	V_{CC} Low Voltage needed to ensure initialization will occur	0.8	–	V
t_{PD}	Duration of $V_{CC} \leq V_{RST}$	30	–	µs

Note:

1. V_{CC} ramp rate can be non-linear.

Table 7.7 3.0V Power-Down Voltage and Timing

Symbol	Parameter	Min	Max	Unit
V_{CC}	V_{CC} Power Supply	2.7	3.6	V
V_{LKO}	V_{CC} Lock-out below which re-initialization is required	2.7	–	V
V_{RST}	V_{CC} Low Voltage needed to ensure initialization will occur	0.8	–	V
t_{PD}	Duration of $V_{CC} \leq V_{RST}$	50	–	µs

Note:

1. V_{CC} ramp rate can be non-linear.

7.7 Hardware Reset

The RESET# input provides a hardware method of returning the device to the standby state.

During t_{RPH} the device will draw I_{CC5} current. If RESET# continues to be held Low beyond t_{RPH}, the device draws CMOS standby current (I_{CC4}). While RESET# is Low (during t_{RP}), and during t_{RPH}, bus transactions are not allowed.

A hardware reset will:

- cause the configuration registers to return to their default values,
- halt self-refresh operation while RESET# is low,
- and force the device to exit the Deep Power Down state.

After RESET# returns High, the self-refresh operation will resume. Because self-refresh operation is stopped during RESET# Low, and the self-refresh row counter is reset to its default value, some rows may not be refreshed within the required array refresh interval per Table 5.7, Array Refresh Interval per Temperature on page 13. This may result in the loss of DRAM array data during or immediately following a hardware reset. The host system should assume DRAM array data is lost after a hardware reset and reload any required data.

Figure 7.5 Hardware Reset Timing Diagram
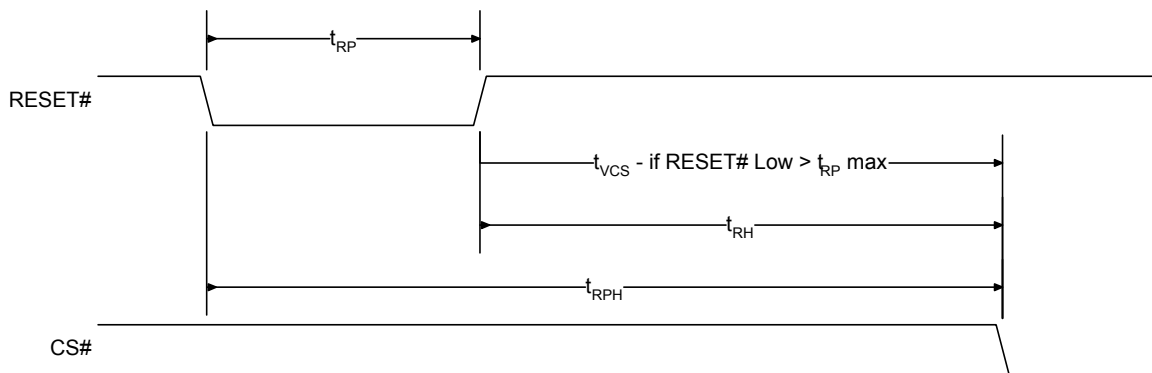
Table 7.8 Power Up and Reset Parameters

Parameter	Description	Min	Max	Unit
t_{RP}	RESET# Pulse Width	200	–	ns
t_{RH}	Time between RESET# (high) and CS# (low)	200	–	ns
t_{RPH}	RESET# Low to CS# Low	400	–	ns

8. Timing Specifications

For the general description of the HyperBus interface timing specifications refer to the HyperBus Specification. The following section describes HyperRAM device dependent aspects of timing specifications.

8.1 AC Characteristics

8.1.1 Read Transactions

Table 8.1 HyperRAM Specific 1.8V Read Timing Parameters

Parameter	Symbol	166 MHz		133 MHz		100 MHz (1)		Unit
		Min	Max	Min	Max	Min	Max	
Read-Write Recovery Time	t_{RWR}	36	–	37.5	–	40	–	ns
Refresh Time	t_{RFH}	36	–	37.5	–	40	–	ns
Access Time	t_{ACC}	36	–	37.5	–	40	–	ns
Chip Select Maximum Low Time – Industrial Temperature	t_{CSM}	–	4.0	–	4.0	–	4.0	µs
Chip Select Maximum Low Time – Industrial Plus Temperature		–	1.0	–	1.0	–	1.0	µs

Note:
1. Sampled, not 100% tested.

Table 8.2 HyperRAM Specific 3.0V Read Timing Parameters

Parameter	Symbol	100 MHz		Unit
		Min	Max	
Read-Write Recovery Time	t_{RWR}	40	–	ns
Refresh Time	t_{RFH}	40	–	ns
Access Time	t_{ACC}	40	–	ns
Chip Select Maximum Low Time — Industrial Temperature	t_{CSM}	–	4.0	µs
Chip Select Maximum Low Time — Industrial Plus Temperature		–	1.0	µs

Note:
1. Sampled, not 100% tested.

8.1.2 Write Transactions

Table 8.3 1.8V Write Timing Parameters

Parameter	Symbol	166 MHz		133 MHz		100 MHz (1)		Unit
		Min	Max	Min	Max	Min	Max	
Read-Write Recovery Time	t_{RWR}	36	–	37.5	–	40	–	ns
Access Time	t_{ACC}	36	–	37.5	–	40	–	ns
Refresh Time	t_{RFH}	36	–	37.5	–	40	–	ns
Chip Select Maximum Low Time – Industrial Temperature	t_{CSM}	–	4.0	–	4.0	–	4.0	µs
Chip Select Maximum Low Time – Industrial Plus Temperature		–	1.0	–	1.0	–	1.0	µs

Note:
1. Sampled, not 100% tested.

Table 8.4 3.0V Write Timing Parameters

Parameter	Symbol	100 MHz		Unit
		Min	Max	
Read-Write Recovery Time	t_{RWR}	40	–	ns
Access Time	t_{ACC}	40	–	ns
Refresh Time	t_{RFH}	40	–	ns
Chip Select Maximum Low Time – Industrial Temperature	t_{CSM}	–	4.0	µs
Chip Select Maximum Low Time – Industrial Plus Temperature		–	1.0	µs

Note:

1. Sampled, not 100% tested.

9. Physical Interface

See the HyperBus Specification for footprint and the 6 × 8 × 1mm (VAA024) physical package diagram.

10. Ordering Information

10.1 Ordering Part Number

The ordering part number is formed by a valid combination of the following:

S27KS 064 1 DP B H I 02 0

Packing Type
0 = Tray
3 = 13" Tape and Reel

Model Number (Additional Ordering Options)
02 = Standard 6 × 8 × 1.0 mm package (VAA024)

Temperature Range
I = Industrial (–40 °C to + 85 °C)
V = Industrial Plus (–40 °C to + 105 °C)

Package Materials
H = Low-Halogen, Lead (Pb)-free

Package Type
B = 24-ball FBGA, 1.00 mm pitch (5x5 ball footprint)

Speed
DA = 100 MHz
DP = 166 MHz

Device Technology
1 = 0.063 μm DRAM Process Technology

Density
064 = 64 Mb

Device Family
S27KS
Cypress Memory 1.8V-only, HyperRAM Self-refresh DRAM
S27KL
Cypress Memory 3.0V-only, HyperRAM Self-refresh DRAM

10.2   Valid Combinations

The Recommended Combinations table lists configurations planned to be available in volume. The table below will be updated as new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Device Family	Density	Technology	Speed	Package, Material and Temperature	Model Number	Packing Type	Ordering Part Number	Package Marking
S27KL	064	1	DA	BHI	02	0	S27KL0641DABHI020	7KL0641DAHI02
S27KL	064	1	DA	BHI	02	3	S27KL0641DABHI023	7KL0641DAHI02
S27KL	064	1	DA	BHV	02	0	S27KL0641DABHV020	7KL0641DAHV02
S27KL	064	1	DA	BHV	02	3	S27KL0641DABHV023	7KL0641DAHV02
S27KS	064	1	DP	BHI	02	0	S27KS0641DPBHI020	7KS0641DPHI02
S27KS	064	1	DP	BHI	02	3	S27KS0641DPBHI023	7KS0641DPHI02
S27KS	064	1	DP	BHV	02	0	S27KS0641DPBHV020	7KS0641DPHV02
S27KS	064	1	DP	BHV	02	3	S27KS0641DPBHV023	7KS0641DPHV02

11. Errata

This section describes the errata for the S27KL0641 and S27KS0641 Family. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Number	Device Characteristics
S27KL0641, S27KS0641	HyperRAM Self-Refresh DRAM

S27KL0641 and S27KS0641 Qualification Status

Product Status: Sampling

S27KL0641, S27KS0641 Errata Summary

The following table defines the errata applicability to available S27KL0641 and S27KS0641S family devices.

Items	Part Number	Silicon Revision	Fix Status
[1]. Variable Latency Mode Does Not Function	S27KL0641 S27KS0641	*B	Will be fixed in production silicon

1. Variable Latency Mode Does Not Function

 ■ **Problem Definition**

   The RWDS signal may not correctly indicate when additional initial latency is being inserted when the device is configured for variable initial latency.

 ■ **Parameters Affected**

   Initial latency count.

 ■ **Trigger Condition**

   Use of variable latency configuration by setting configuration register 0 bit 3 to 0.

 ■ **Scope of Impact**

   Intermittent failure of read data to start transferring on the bus when expected, based on the latency count indicated by RWDS during the command-address cycles.

 ■ **Workaround**

   Use the default fixed latency configuration or use RWDS transitions as the indication for when to capture the first and following read data transfers.

 ■ **Fix Status**

   Will be fixed in production silicon.

12. Revision History

Document History Page

| Document Title: S27KL0641, S27KS0641, HyperRAM™ Self-Refresh DRAM 3.0V/1.8V 64 Mb (8 MB) |
| Document Number: 001-97964 |

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	–	MAMC	05/01/2015	Initial release
*A	–	MAMC	06/05/2015	Read Transactions: Maximum Operating Frequency For Latency Code Options table: updated 'Latency Code' 0010 values Device Identification Registers: Updated 'ID Register 1 Bit Assignments' table Electrical Specifications: Updated Ambient Temperature with Power Applied HyperRAM Hardware Interface: Updated the following: Power-On Reset: removed section Power Down: removed section DC Characteristics (CMOS Compatible) table: updated I_{CC5}, I_{CC6I}, and I_{CC6IP} Test Conditions Electrical Specifications/Power Down: 1.8V Power-Down Voltage and Timing table: changed V_{RST} and T_{PD} MIn 3.0V Power-Down Voltage and Timing table: changed V_{RST} and T_{PD} MIn Key to Switching Waveforms: removed section AC Test Conditions: removed section AC Characteristics: updated section HyperBus Specification: Removed section. Refer to the HyperBus specification for all non-device specific information on the HyperBus interface.
*B	–	MAMC	07/10/2015	Physical Interface: Updated section. Ordering Information: Updated Valid Combinations table.
*C	4854266	MAMC	07/29/2015	Updated to Cypress template
*D	5041839	MAMC	12/08/2015	Updated DC Characteristics: Added I_{DPD} for T_A = 105°C Updated I_{LI} for the RESET# input.
*E	5155616	RYSU	03/01/2016	Added Errata.

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